S-7760A Series

PROGRAMMABLE PORT CONTROLLER (PORT EXPANDER WITH BUILT-IN E²PROM CIRCUIT)

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Rev.2.0_01

The S-7760A is a programmable port controller IC comprised of an E²PROM, a control circuit for data output, a circuit to prevent malfunction caused by low power supply voltage and others.
This IC operates at 400 kHz and interfaces with exteriors via I²C-bus, controls an 8ch digital output with a serial signal.
Among the digital output ports of 8 channels, the lower 4 channels have a timer function so that at each port, users are able to set the default value and inverted delay time. In the higher 4 channels, setting the fixed output is available at each port. The default value is maintained despite power-off because this IC has an E²PROM.
The S-7760A is able to be used to control ON/OFF for the chips surrounding MPU and to output the default data that devices fundamentally have.

■ Features

- Operating voltage range: 2.3 to 4.5 V
- 8ch digital output: Higher 4 channels; fixed output/lower 4 channels; timer action
- Operating frequency of I²C-bus interface: 400 kHz
- Low current consumption at standby: 3.0 μA Max. (V_{CCH} = 4.5 V CMOS input type)
  10.0 μA Max. (V_{CCH} = 4.5 V low voltage input type)
- Built-in E²PROM circuit: 6-byte
- E²PROM endurance: 10^5 cycles / word*1 (at −40 to +85 °C)
- E²PROM data retention: 10 years (after rewriting 10^5 cycles / word)
- Function to protect write in E²PROM
- Function to prevent malfunction during low power supply voltage operation
- Lead-free, halogen-free*2

***1.** For each address (Word: 8 bits)
***2.** Refer to "■ **Product Name Structure**" for details.

■ Application

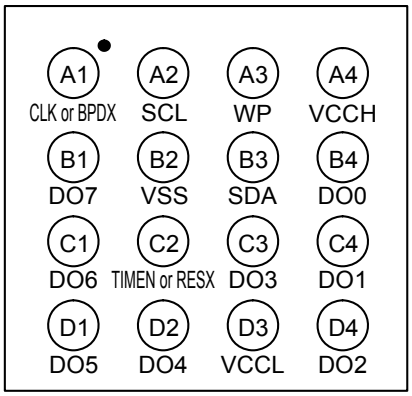
- Mobile phone
- Portable communication device
- Digital still camera
- Digital video camera

■ Package

- WLP-16A
- 16-Pin TSSOP (Under development)

■ Pin Configuration

WLP-16
Bottom View



（1.93 × 2.07 × 0.6 max.）

Figure 1

16-Pin TSSOP*1
Top View

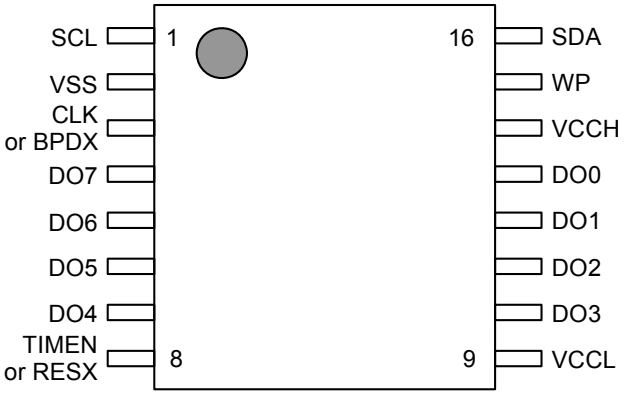


Figure 2

1. Under development

■ List of Pin

Table 1 WLP-16A List of Pin

Pin No.	Pin name	Description
A1*1	CLK	Input for external clock
	BPDX	Input for bus pull-down bar
A2	SCL	Input for serial clock
A3	WP	Input for Write protect
A4	VCCH	Power supply
B1	DO7	Output port 7
B2	VSS	GND
B3	SDA	Serial data I/O
B4	DO0	Output port 0
C1	DO6	Output port 6
C2*2	TIMEN	Input for timer enable
	RESX	Input for reset bar
C3	DO3	Output port 3
C4	DO1	Output port 1
D1	DO5	Output port 5
D2	DO4	Output port 4
D3	VCCL	Power supply for output port
D4	DO2	Output port 2

Table 2 16-Pin TSSOP List of Pin

Pin No.	Pin name	Description
1	SCL	Input for serial clock
2	VSS	GND
3*1	CLK	Input for external clock
	BPDX	Input for bus pull-down bar
4	DO7	Output port 7
5	DO6	Output port 6
6	DO5	Output port 5
7	DO4	Output port 4
8*2	TIMEN	Input for timer enable
	RESX	Input for reset bar
9	VCCL	Power supply for output port
10	DO3	Output port 3
11	DO2	Output port 2
12	DO1	Output port 1
13	DO0	Output port 0
14	VCCH	Power supply
15	WP	Input for Write protect
16	SDA	Serial data I/O

1. Whether to set A1 in CLK or BPDX is selectable by option (Pin number is 3 for 16-Pin TSSOP).
2. Whether to set C2 in TIMEN or RESX is selectable by option (Pin number is 8 for 16-Pin TSSOP).

■ Block Diagram

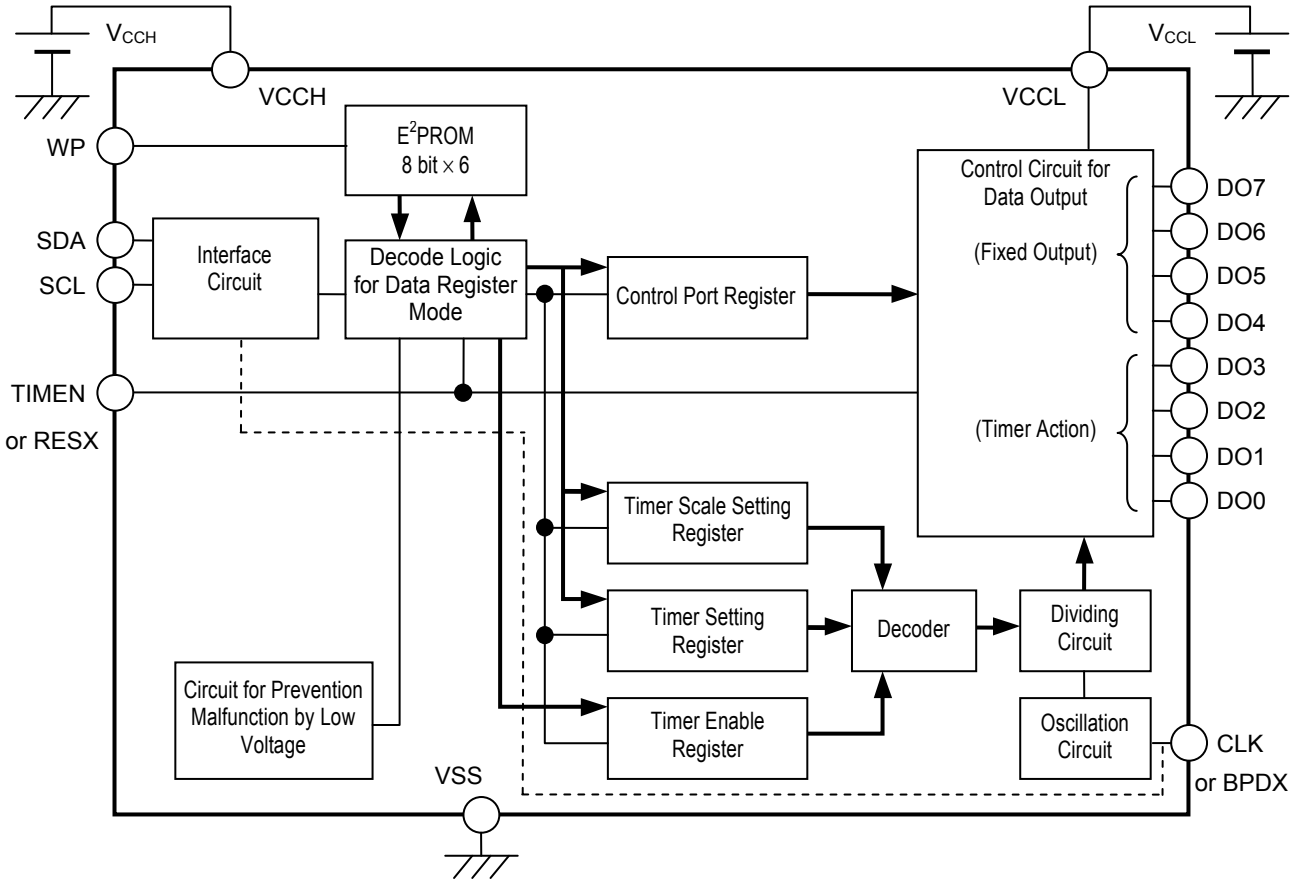


Figure 3

■ General Description of Pin Function

1. SDA (Serial data I/O) pin

The SDA pin transmits serial data bi-directionally, is comprised of a signal input pin and a pin with Nch transistor open drain output. In use, generally, connect the SDA line to any other device which has the open-drain or open-collector output with Wired-OR connection by pulling up to V_{CCH} by a resistor.

2. SCL (Input for serial clock) pin

The SCL pin is an input pin for serial clock, processes a signal at a rising/falling edge of SCL clock. Pay attention fully to the rising/falling time and comply with specifications.

3. WP (Input for Write protect) pin

This pin performs Write Protect to E²PROM (This pin does not have a function for Write protect to the register).
Set the WP pin in V_{CCH} when using the Write Protect function. If not, set the WP pin to GND.

4. TIMEN (Input for timer enable)/RESX (Input for reset bar) pin

Select TIMEN or RESX by option.
The TIMEN pin controls enable (“H”)/disable (“L”)/Start (“L”→”H”) in the timer action (inversion of digital output due to elapsed period). Refer to the description of related register in “■ **Command**” and “■ **Condition to Start Timer**” regarding details of timer action.
The RESX pin has the negative logic, is a pin to reset. This pin initializes the circuit with “L” input, and performs its regular action (the status of reset release) by inputting “H”. This pin goes in its reload action immediately after releasing reset, thus by initializing, the value of related register is reloaded to the data that E²PROM has. If a user selects the RESX pin, the TIMEN pin’s function will be invalid so that the internal signal of TIMEN is fixed in “L”.

5. CLK (Clock input)/BPDX (Input for bus pull-down bar) pin

As for primary clock for circuits, users can select either from the internal oscillation circuit or input it externally by option. In case of using an external clock input, this pin works as the CLK pin to input clock by itself. In case of using an internal oscillation circuit, users can set this pin as the BPDX pin by option. With “L” input from the BPDX pin, SDA and SCL in I²C-bus interface are forcibly pulled-down. This pin performs its regular action by inputting “H”. Users also can select the setting which does not have an internal oscillation circuit or bus pull-down for this pin.

6. DO0, DO1, DO2, DO3 (Digital output) pin

These are lower 4 channels in the digital output ports. Their default values are equal to the ones of a control port register during output. These lower 4 channels are for timer action. Its output inverts after; the timer starts and delay time has elapsed.

7. DO4, DO5, DO6, DO7 (Digital output) pin

These are the higher 4 channels in the digital output ports. Their default values are equal to the ones of a control port register during output. These higher 4 channels have fixed output. The elapsed period does not make outputs inverted.

8. VSS pin

Connect to GND.

9. VCCH pin

Except for the output ports, the power supply is applied to the entire circuit via this pin. Regarding the voltage’s value to be applied to this pin, refer to “■ **Recommended Operating Conditions**”.

10. VCCL pin

This pin is to apply the power supply for the output ports. Regarding the voltage’s value to be applied to this pin, refer to “■ **Recommended Operating Conditions**”.

■ Equivalent Circuit of I/O Pin

This IC's I/O pin does not have an element of pull-up or pull-down. The SDA line has an open drain output. The followings are equivalent circuits.

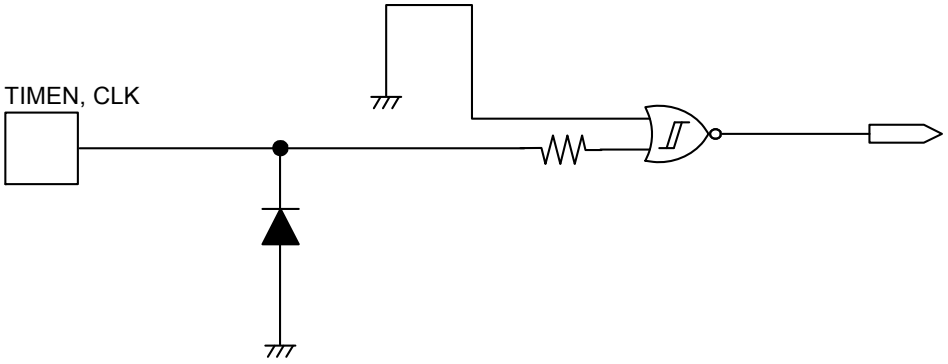


Figure 4 TIMEN, CLK Pin

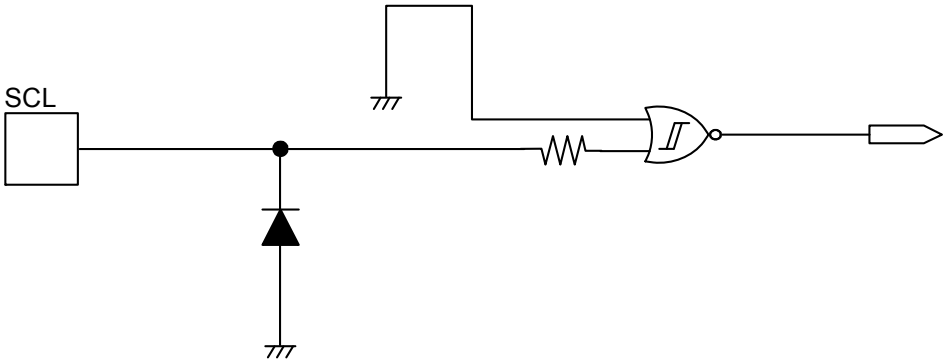


Figure 5 SCL Pin (When selecting CLK option)

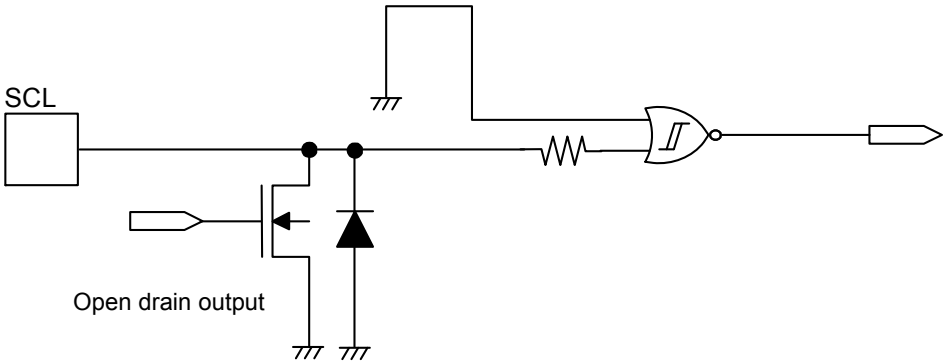


Figure 6 SCL Pin (When selecting BPDX option)

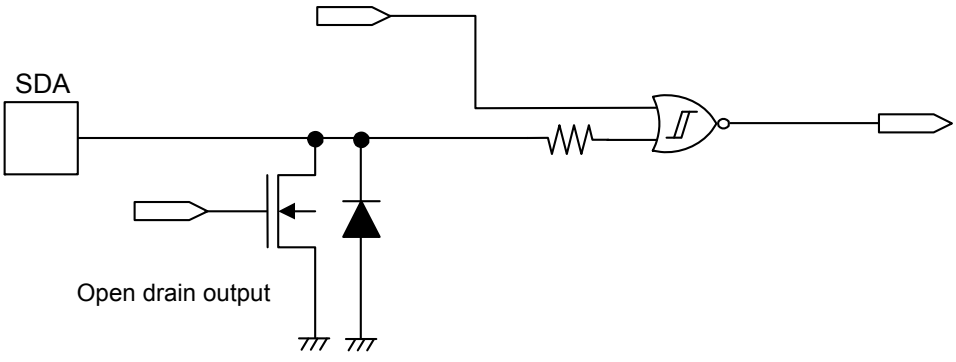


Figure 7 SDA Pin

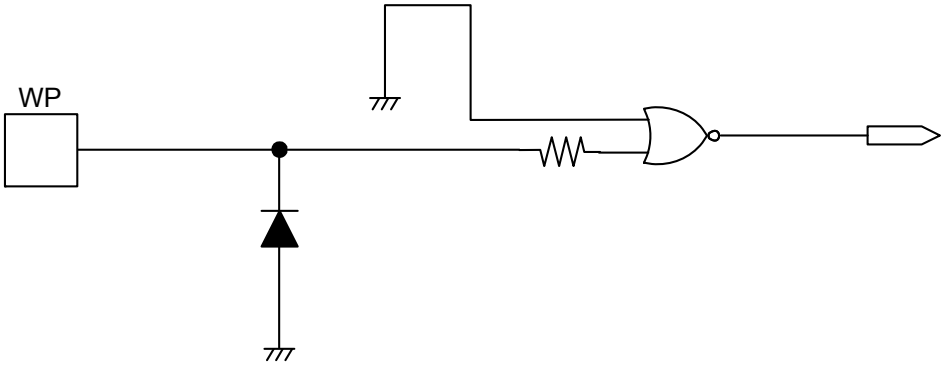


Figure 8 WP Pin

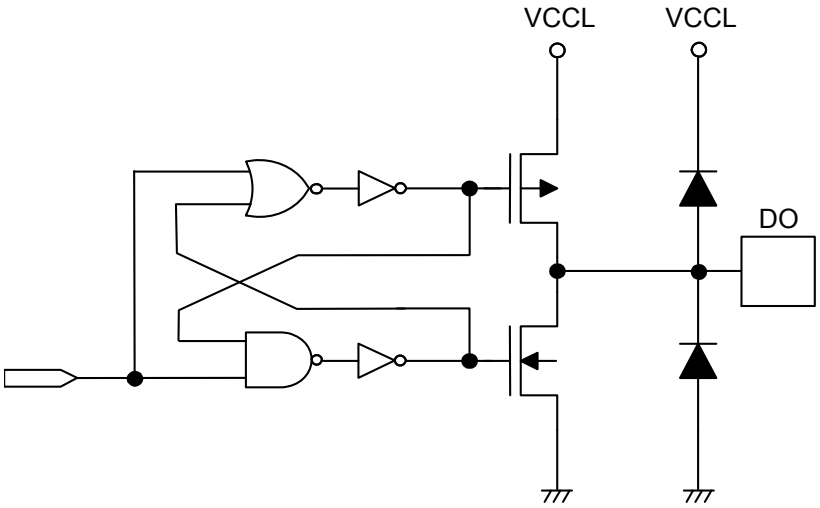


Figure 9 DO Pin

■ Option Regarding High/Low Leveled Input Voltage for Pin

For the SDA, SCL and TIMEN pins, the two types of high/low leveled input voltage are selectable by option.

1. CMOS input type

The high/low leveled input voltage varies according to the power supply voltage.
The value is defined by the rate for power supply voltage as; $V_{IH} \geq 0.7 \times V_{CCH}$ by high leveled input voltage, $V_{IL} \leq 0.3 \times V_{CCH}$ by low leveled input voltage.

2. Low voltage input type

This option is effective when the power supply voltage at MPU is lower than the one of the S-7760A.
If using this option, setting a level-shifter for an interface signal is unnecessary.
Independent of the power supply voltage, the high/low leveled input voltage is constant, moreover, the value is also constant unlike the definition by the rate as; $V_{IH} \geq 1.5$ V by high leveled input voltage, $V_{IL} \leq 0.3$ V by low leveled input voltage.

The TIMEN pin is able to set as the RESX pin by option, however, also in this case the types regarding high/low leveled input voltage are selectable.

■ Absolute Maximum Ratings

Table 3

Item	Symbol	Rating	Unit
Power supply voltage1	V_{CCH}	−0.3 to +7.0	V
Power supply voltage2	V_{CCL}	−0.3 to V_{CCH}	V
Input voltage	V_{IN}	−0.3 to V_{CCH}+0.3	V
Output voltage (SDA)	V_{OUT1}	−0.3 to V_{CCH}	V
Output voltage (DO)	V_{OUT2}	−0.3 to V_{CCL}	V
Operating ambient temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 4

Item	Symbol	Applicable Pin	Option	Min.	Typ.	Max.	Unit
Supply voltage 1	V_{CCH}	VCCH	–	2.3 *1	–	4.5	V
Output supply voltage 2	V_{CCL}	VCCL	–	1.5	–	V_{CCH} *2	V
High-level input voltage 1	V_{IH1}	WP, CLK	–	0.7 × V_{CCH}	–	V_{CCH}	V
Low-level input voltage 1	V_{IL1}		–	0.0	–	0.3 × V_{CCH}	V
High-level input voltage 2	V_{IH2}	SDA, SCL, TIMEN	CMOS input type	0.7 × V_{CCH}	–	V_{CCH}	V
			Low voltage input type	1.5	–	V_{CCH}	V
Low-level input voltage 2	V_{IL2}		CMOS input type	0.0	–	0.3 × V_{CCH}	V
			Low voltage input type	0.0	–	0.3	V

***1.** Set $V_{CCH} \geq 2.5$ V when rising VCCH and TIMEN simultaneously.
***2.** Set the voltage of VCCL as $V_{CCH} \geq V_{CCL}$.

■ Pin Capacitance

Table 5

(Ta = 25 °C, f = 1.0 MHz, V_{CCH} = 3 V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	SCL, WP, TIMEN, CLK	V_{IN} = 0 V	–	–	10	pF
Input/output capacitance	$C_{I/O}$	SDA	$V_{I/O}$ = 0 V	–	–	10	pF

■ Endurance

Table 6

Item	Symbol	Operating Temperature	Min.	Typ.	Max.	Unit
Endurance	N_W	−40 to +85 °C	10^5	–	–	cycles / word

■ DC Electrical Characteristics

Table 7 DC Characteristcs 1

Item	Symbol	Condition *1	Option	V_{CCH} = V_{CCL} = 2.3 to 4.5 V			Unit
				Min.	Typ.	Max.	
Current consumption during standby	I_{SB}	f_{SCL} = 0 Hz	CMOS input type	–	–	3.0	μA
Current consumption during standby	I_{SB}	f_{SCL} = 0 Hz	Low voltage input type	–	–	10.0	μA
Current consumption (READ)	I_{CC1}	f_{SCL} = 400 kHz	–	–	–	0.8	mA
Current consumption (WRITE)	I_{CC2}	f_{SCL} = 400 kHz	–	–	–	4.0	mA
Current consumption during operation of internal oscillation circuit	I_{CC3}	f_{SCL} = 0 Hz	–	–	–	0.8	mA

***1.** The total current consumption when V_{CCH} = V_{CCL}. No load on pins DO7 to 0.

Table 8 DC Characteristcs 2

Item	Symbol	Pin	Condition	V_{CCH} = 2.3 to 4.5 V			Unit
				Min.	Typ.	Max.	
Input current	I_{IH1}	CLK, TIMEN, WP, SDA, SCL	V_{IN} = V_{CCH}	–	–	1.0	μA
	I_{LI1}		V_{IN} = GND	–1.0	–	–	μA
Output leakage current	I_{LO1}	SDA	V_{IN} = V_{CCH}	–	–	1.0	μA
Low-level output voltage	V_{OL1}	SDA	I_{OL} = 3.2 mA	–	–	0.4	V
			I_{OL} = 1.5 mA	–	–	0.3	V
	V_{OL2}	DO	I_{OL} = 100 μA V_{CCL} = V_{CCH} to 1.5 V	–	–	0.1	V
High-level output voltage	V_{OH2}	DO	I_{OH} = –100 μA V_{CCL} = V_{CCH} to 1.5 V	V_{CCL}–0.2	–	–	V
Low-level output voltage *1	V_{OL3}	SCL	I_{OL} = 3.2 mA	–	–	0.6	V
			I_{OL} = 1.5 mA	–	–	0.4	V

***1.** When the option for BPDX is valid.

■ AC Electrical Characteristics

Table 9 Measurement Conditions

Input pulse voltage	$V_{IL} = 0.1 \times V_{CCH}$, $V_{IH} = 0.9 \times V_{CCH}$
Rising/falling time of input pulse	20 ns
Output reference voltage	$0.5 \times V_{CCH}$
Output load	100 pF+ Pull-up resistor 1.0 kΩ

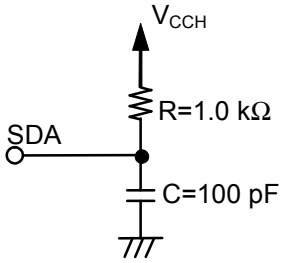


Figure 10 Output Load Circuit

Table 10 AC Electrical Characteristics

Item	Symbol	V_{CCH} = 2.3 to 4.5 V			Unit
		Min.	Typ.	Max.	
SCL clock frequency *1	f_{SCL}	0	–	400	kHz
SCL clock time "L" *1	t_{LOW}	1.3	–	–	µs
SCL clock time "H" *1	t_{HIGH}	0.6	–	–	µs
SDA output delay time *1	t_{AA}	–	–	0.9	µs
SDA output hold time *1	t_{DH}	50	–	–	ns
Start condition setup time *1	$t_{SU.STA}$	0.6	–	–	µs
Start condition hold time *1	$t_{HD.STA}$	0.6	–	–	µs
Data input setup time *1	$t_{SU.DAT}$	100	–	–	ns
Data input hold time *1	$t_{HD.DAT}$	0	–	–	ns
Stop condition setup time *1	$t_{SU.STO}$	0.6	–	–	µs
SCL, SDA rise time *1	t_R	–	–	0.3	µs
SCL, SDA fall time *1	t_F	–	–	0.3	µs
Bus release time *1	t_{BUF}	1.3	–	–	µs
Noise suppression time *1	t_I	–	–	50	ns
Frequency for external oscillation input *2	f_{TEX}	–	–	400	kHz

***1.** The timing is defined by 10% and 90% of the waveform.
***2.** When selecting the option for external oscillation input.

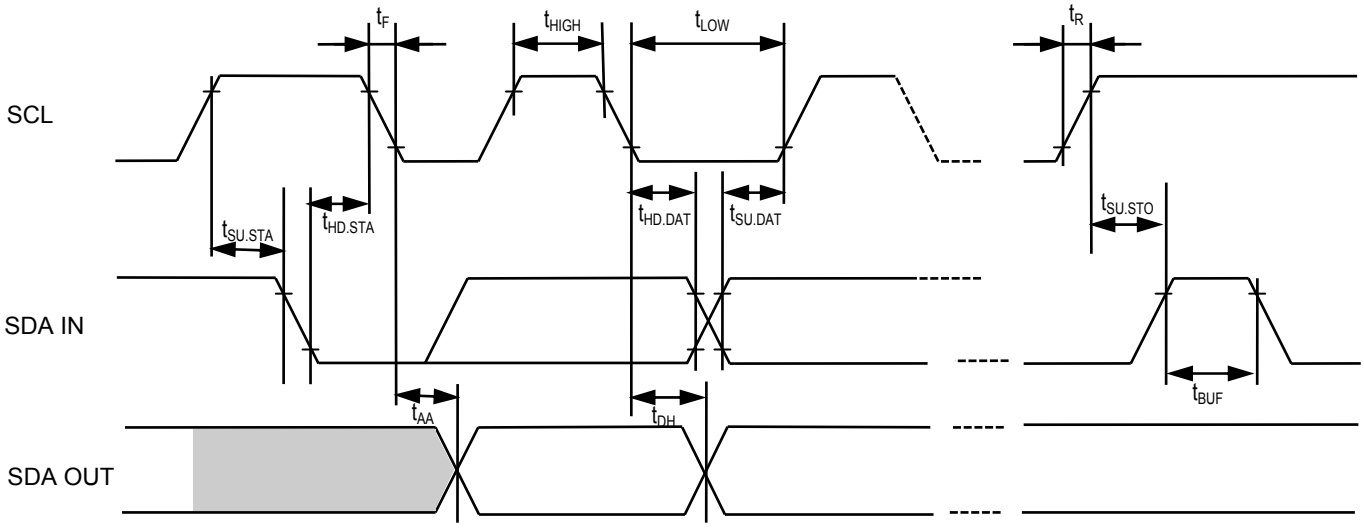


Figure 11 Bus Timing

Table 11 Characteristics of Period

Item	Symbol	Min.	Typ.	Max.	Unit
Write period to E²PROM	t_{WR}	–	2.0	5.0	ms
Delay time accuracy (short-time setting)*1	t_{DLY1}	0.8 × T	T	1.2 × T	µs
Delay time accuracy (long-time setting)*1	t_{DLY2}	0.8 × LT	LT	1.2 × LT	µs

***1.** Refer to **Figure 16 Timer Setting Register**.
T represents time reference (timer scale) in the short-time setting.
LT represents time reference (timer scale) in the long-time setting.

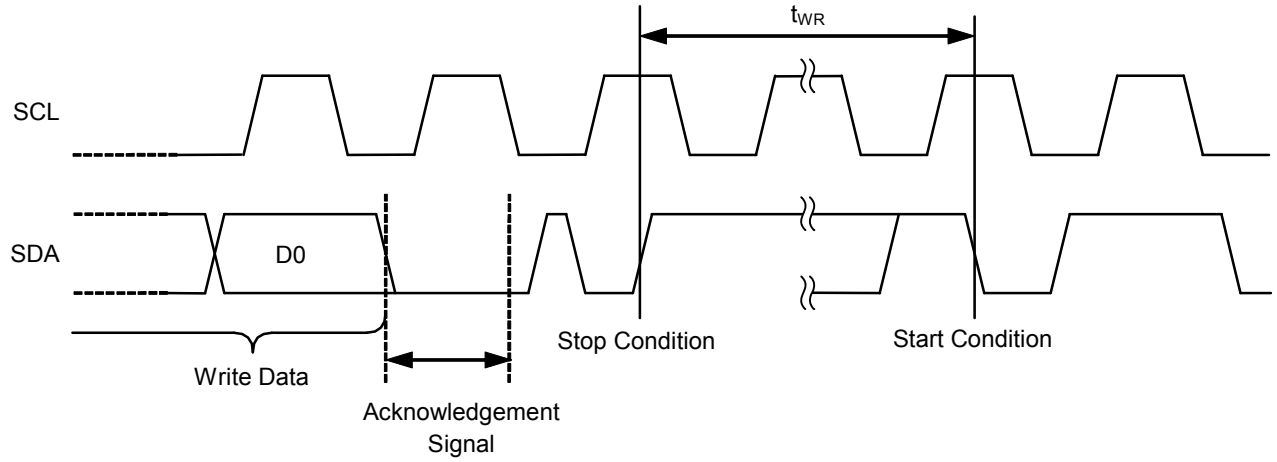


Figure 12 Write Cycle Timing

■ Device Addressing

To start communication, the master device (MPU) on the system generates a start condition for the slave device (S-7760A). After that, the master device sends a device address with 7-bit length and Read/Write instruction code with 1-bit length on the SDA bus. The higher 3 bits in a device address (DC2, DC1, DC0) are device codes. A device code can obtain the fixed value selected by option. Command is omitted if a device code does not correspond. Set the command in the following 4 bits (C3, C2, C1, C0). Next, by selecting either of Read or Write by Read/Write bit, the S-7760A sends an acknowledgement signal back. If the second byte is Read, MPU sends an acknowledgement signal back after outputting data Read with 8-bit length. If it is Write, after outputting Write data with 8-bit length, the S-7760A sends an acknowledgement signal back. To finish these sequential commands, the S-7760A generates a stop condition as its final procedure.
There is a 1-byte command for the S-7760A, but inputting the second byte as a dummy does not affect on this device addressing. In this case, the operation for the second byte is as well as for Read/Write because of the bit corresponding to Read/Write in the first byte.

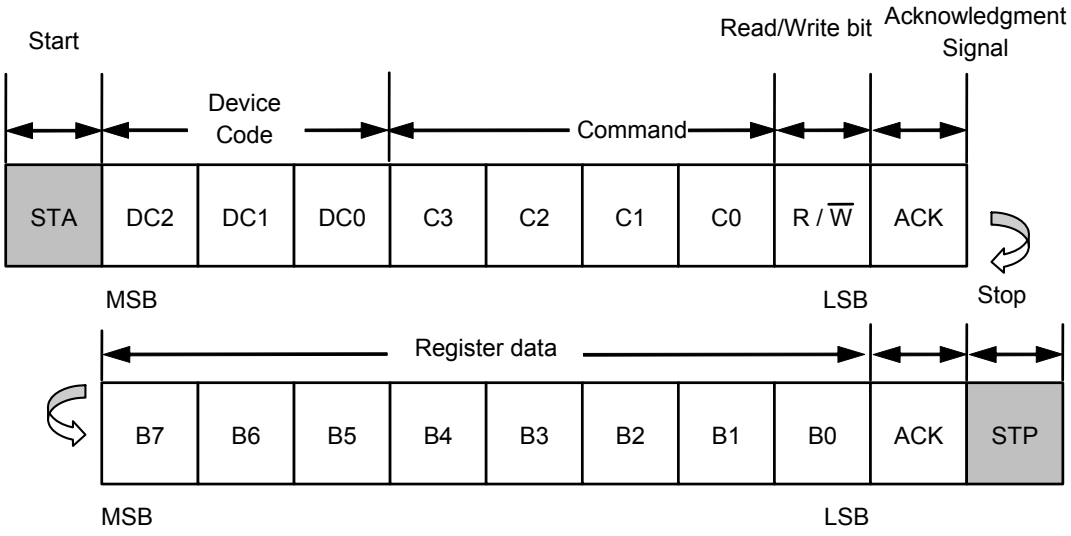


Figure 13 Device Address

■ Configuration of Command

Table 12 List of Command

Command	C3	C2	C1	C0	R / $\overline{W}$	Data							
						B7	B6	B5	B4	B3	B2	B1	B0
Reload	0	0	0	0	R / $\overline{W}$ *1	—							
Switching access to register/E²PROM	0	0	0	1	—*2	—							
Timer enable register	0	0	1	0	$\overline{W}$	—	—	—	—	TEN3	TEN2	TEN1	TEN0
Do not use (Do not access)	0	0	1	1	—	—							
Do not use (Do not access)	0	1	0	0	—	—							
Control port	0	1	0	1	R / $\overline{W}$ *3	CTR7	CTR6	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
Setting for timer scale	0	1	1	0	R / $\overline{W}$ *3	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0
Do not use (Do not access)	0	1	1	1	—	—							
Timer setting for DO0	1	0	0	0	R / $\overline{W}$ *3	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO1	1	0	0	1	R / $\overline{W}$ *3	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO2	1	0	1	0	R / $\overline{W}$ *3	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Timer setting for DO3	1	0	1	1	R / $\overline{W}$ *3	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T
Do not use (Do not access)	1	1	0	0	—	—							
Do not use (Do not access)	1	1	0	1	—	—							
Do not use (Do not access)	1	1	1	0	—	—							
Do not use (Do not access)	1	1	1	1	—	—							

***1.** R / $\overline{W}$ = 1/0 Both execute “reload”.

***2.** It is register access mode when R / $\overline{W}$ = 0, E²PROM access mode when R / $\overline{W}$ = 1.

***3.** By Switching access to register/E²PROM, users can select either register or E²PROM when Read/Write. Refer to “■ **Register and E²PROM**”.

■ Register and E²PROM

This IC has an E²PROM. Data in the E²PROM is maintained despite power-off. The S-7760A has a register which corresponds to the data in the E²PROM, the S-7760A sends data to this corresponding register during power-on (releasing detection of the low voltage) and inputting the reload command. In case of selecting the RESX pin by option, the S-7760A reloads after releasing reset. The following registers are the ones to be reloaded;

- Control port register (1-byte)
- Timer scale setting register (1-byte)
- DO3 to 0 Timer setting register (1-byte in each port, total 4 bytes)

Users are able to switch access between corresponding register and E²PROM by “Switching access to register/E²PROM” command. Immediately after power-on, the S-7760A is in “register access mode”. In this register access mode, only the register is rewritten, the E²PROM maintains the prior data. But in “E²PROM access mode”, both data in the register and the E²PROM is rewritten. In data Read, access mode data which is being selected by user; is read.

■ Command

1. Reload

This is a 1-byte command. Users can reload by inputting either of $R/\overline{W}$ in 0/1. When inputting this command, the data corresponding to the E²PROM is loaded to the register. After completing reload, (if the condition is satisfied), the timer action starts. The reload command is not accepted during the timer action (from its start to the final invert of output). Refer to "■ **Condition to Start Timer**" regarding details.

2. Switching access to register/E²PROM

This is a 1-byte command. The mode is in "register access mode" when this command is $R/\overline{W}$ = 0, "E²PROM access mode" when this command is $R/\overline{W}$ = 1. The register corresponding to the E²PROM is the one to be reloaded. In register access mode, only the register is rewritten, the E²PROM maintains the prior data. In "E²PROM access mode", both data in the register and E²PROM is rewritten.

3. Timer enable register

A timer enable register is a 4-bit register for Write only (it sends back FFh during Read). By setting each bit in the register in "1", an oscillation circuit starts, output from the lower 4ch ports (DO3 to 0) invert after the elapsed period which is set by a timer setting register. This action is called "timer action". This timer action starts at the point when receiving TEN0 which is LSB in the register. The bit automatically goes back in "0" after writing "1" in the timer enable register. Users cannot write in this register during the timer action (from the start to the final invert of output). This register is not the one to be reloaded, thus it does not have the data which corresponds to the E²PROM. The option is available for the condition to start a timer; Condition AND with TIMEN = High, depending on the option. Refer to "■ **Condition to Start Timer**" regarding details.

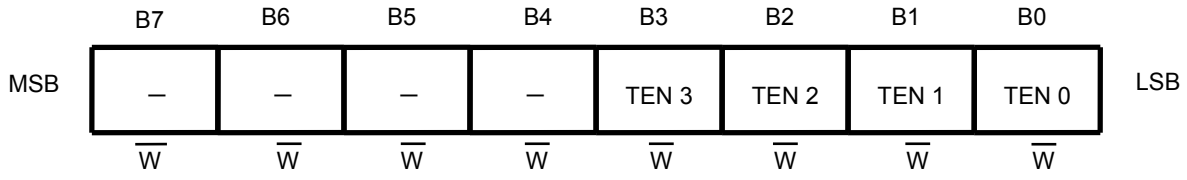


Figure 14 Timer Enable Register

0 : Disable to invert output
1 : Enable to invert output

4. Control port register

Control port register is an 8-bit register. Users can set output data which is from output ports (DO7 to 0). If data is “1”, output is “H”, and if it is “0”, output is “L”. This register is the one to be reloaded. Data in this register does not change even if output from the port is inverted by timer action.

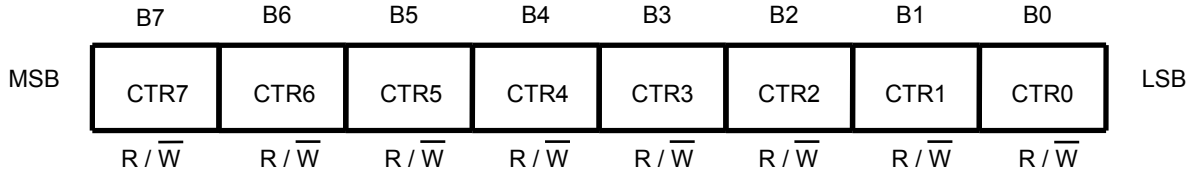
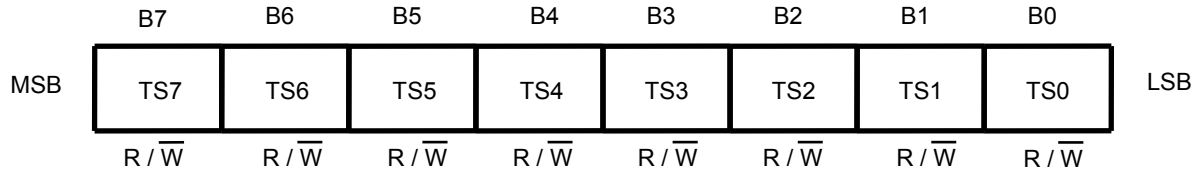


Figure 15 Control Port Register

5. Timer scale setting register

The lower 4 bits are registers for timer scale setting. Users can set, whether short-time or long-time, time reference (scale) for the delay time setting at each port DO3 to 0.
The higher 4 bits are Read/Write-able bits, however, they do not affect on circuit action because DO7 to 4 have fixed output. This register is the one to be reloaded.



TSn = 1 : Timer scale DO3 to 0 Short-time setting
TSn = 0 : Timer scale DO3 to 0 Long-time setting

Figure 16 Timer Scale Setting Register

6. DO0 to 3 Timer setting registers

These registers are 8-bit registers which correspond to each port, with these registers, users can set delay time for the change of output at output ports (DO0 to 3). When delay time is set, its value is a multiple of timer scale. The multiple is integers 1 to 8. By setting the corresponding bits seen in **Figure 17** in "1", a multiple is selected to determine delay time. For each port, set only 1-bit in the bit that you set "1". And if setting all 8 bits in "0", output is not inverted even if the condition to start a timer matches.

MSB	B7	B6	B5	B4	B3	B2	B1	B0	LSB
DO0	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO1	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO2	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
DO3	8×T	7×T	6×T	5×T	4×T	3×T	2×T	1×T	
	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	R / $\overline{W}$	

Figure 17 Timer Setting Register DO0 to 3

Figure 17 shows the short-time timer scale setting. In case of a long-time setting, T is LT.
The following options are available for timer setting.

- Using an internal oscillation circuit/Switching the external clock input
- Option setting for delay time (4 types)

(1) When using an internal clock (Typ.)
Option A : (Short-time setting scale, long-time setting scale) = (T, LT) = (5 μs, 320 μs)
Option B : (Short-time setting scale, long-time setting scale) = (T, LT) = (10 μs, 640 μs)

(2) When using an external clock (Period of input clock = T')
Option A : (Short-time setting scale, long-time setting scale) = (T, LT) = (T', 64 × T')
Option B : (Short-time setting scale, long-time setting scale) = (T, LT) = (2 × T', 128 × T')

In case that users select “delay time option A” and to use an internal oscillation circuit, and if setting “1” in B6 bit in the D03 timer setting register, “1” in TS3 in the timer scale register, DO3 inverts at delay time of 35 μs (7 × 5 μs). Other examples are shown in **Figure 18**.

	MSB B7	B6	B5	B4	B3	B2	B1	B0 LSB
Example 1-1	40 μs	35 μs	30 μs	25 μs	20 μs	15 μs	10 μs	5 μs
Example 1-2	2.56 ms	2.24 ms	1.92 ms	1.60 ms	1.28 ms	0.96 ms	0.64 ms	0.32 ms

	MSB B7	B6	B5	B4	B3	B2	B1	B0 LSB
Example 2-1	160 μs	140 μs	120 μs	100 μs	80 μs	60 μs	40 μs	20 μs
Example 2-2	10.24 ms	8.96 ms	7.68 ms	6.40 ms	5.12 ms	3.84 ms	2.56 ms	1.28 ms

Example 1. When using an internal CLK
Example 1-1 In case of; Timer scale register “1” (short-time setting), Delay time option “A” (×1 setting); (T = 5 μs)
Example 1-2 In case of; Timer scale register “0” (long-time setting), Delay time option “A” (×1 setting); (LT = 320 μs)

Example 2. When using an external CLK (100 KHz, T’ = 10 μs)
Example 2-1 In case of; Timer scale register “1” (short-time setting), Delay time option “B” (×2 setting); (T = 2 × T’ = 20 μs)
Example 2-2 In case of; Timer scale register “0” (long-time setting), Delay time option “B” (×2 setting); (LT = 128 × T’ = 1280 μs)

Figure 18 Example of Using Timer Setting Register 0 to 3

■ Condition to Start Timer

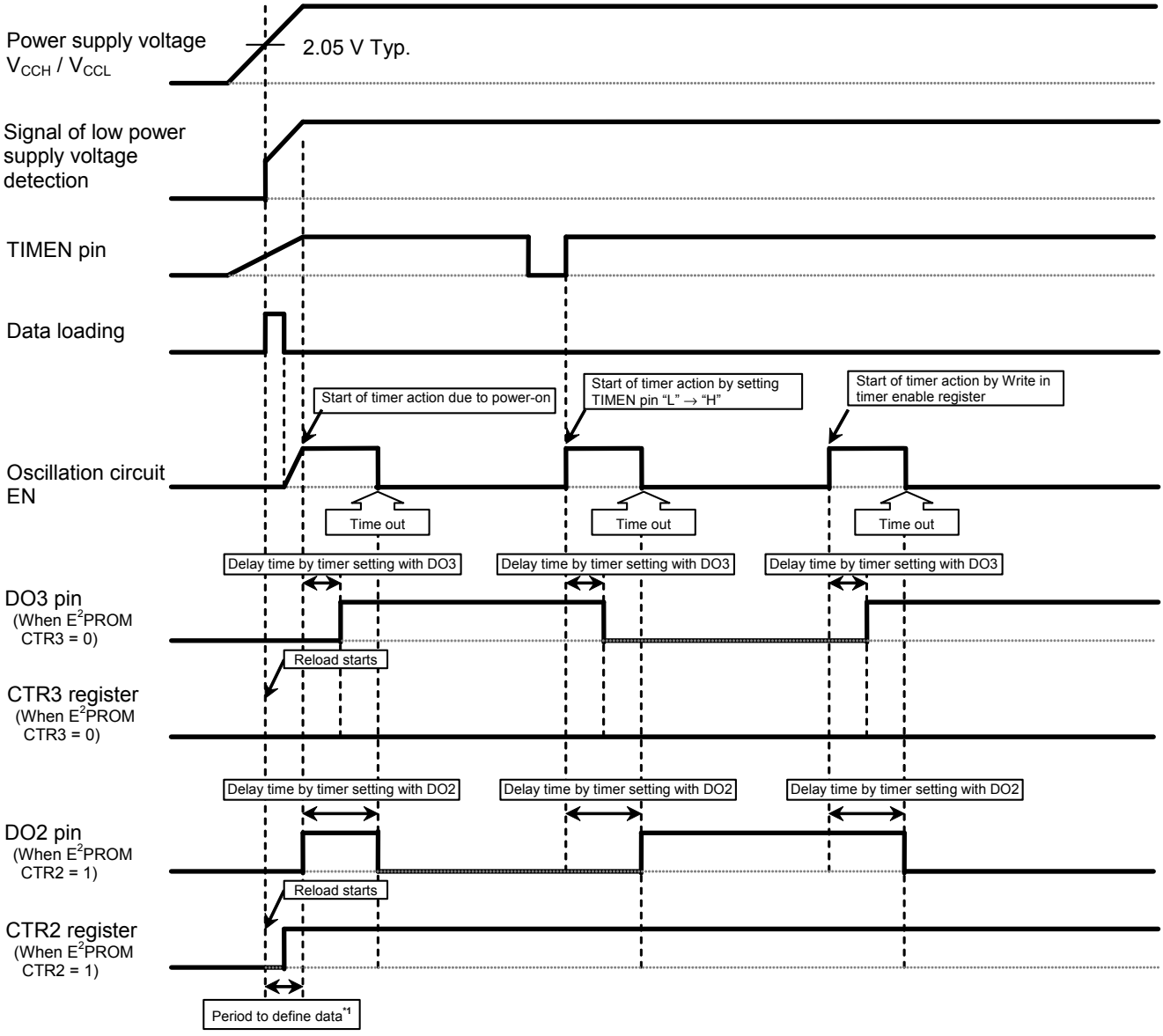
Table 13 Condition to Start Timer

Option	Condition	Reload	TIMEN Pin	Bit TEN3 to 0
1	A	Start → Finish	"H"	Don't care
	B	Regular status	"L" → "H"	Don't care
	C	Regular status	"H"	Write "0" → "1"
2	D	Regular status	Don't care	Write "0" → "1"

2 types of options are available for the condition to start a timer. Select either for each digital output port DO0 to 3; if selecting option 1, the condition to start a timer is three, A/B/C.
If in option 2, the condition is D only. In D, the S-7760A does not react to reload and rising of TIMEN. By writing "1" in TEN, not in TIMEN, the timer starts.
During power-on of power supply VCCH, the S-7760A automatically reloads (transmits data from the E²PROM to the register). In this case, TIMEN = "H" and it is in option 1, the S-7760A goes in the timer action after reloading. Thus the sequential action is; after power-on of power supply VCCH, reload → timer. This is as well if the status changed from detection to release of the low power supply voltage.
The timer action does not stop in the middle of its process even if setting TIMEN in "H" → "L" after the timer action has started. In selecting "the option for internal oscillation circuit", the oscillation circuit is generally being stopped, but the oscillation starts when the condition to start a timer matches. And it stops by finishing the timer action (the final invert of output).

■ Timing of Data Loading from E²PROM and Timer Action

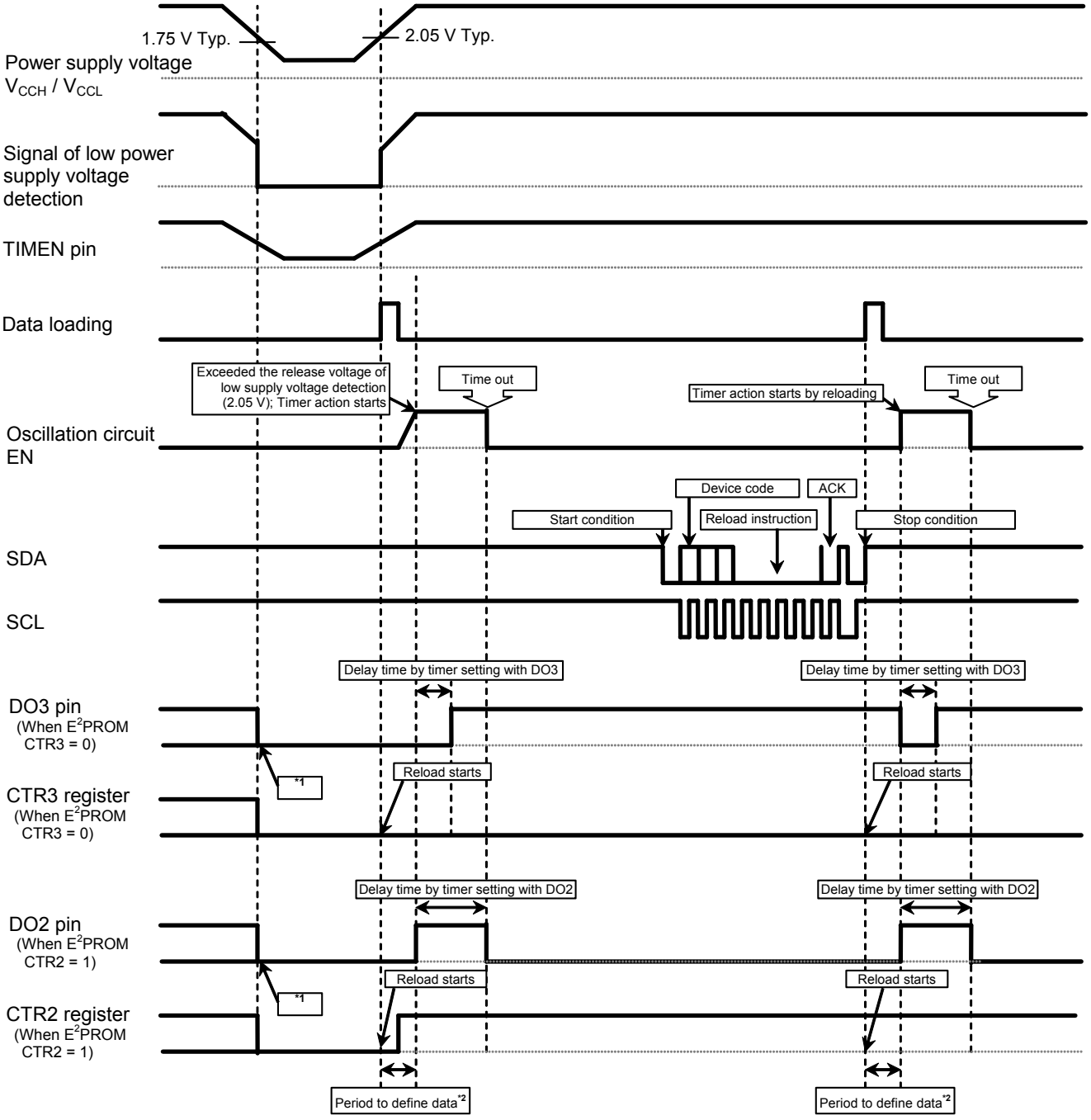
The example of timing chart of data loading from the E²PROM and timer action is shown in **Figure 19** and **20**.
Set $V_{CCH} \geq 2.5$ V when rising VCCH and TIMEN simultaneously.



***1.** A period to define data is; the loading period from E²PROM + the period to stabilize output from DO7 to 0 pin = within 100 μs.

Figure 19 Data Loading and Timer Action Example 1

This IC goes in the status to reset the circuits when the power supply voltage decreases less than the level of the detection voltage of the circuit for prevention malfunction by low voltage (1.75 V Typ.). And the DO7 to 0 pins go in "L". After that, when the power supply voltage increases more than the level of the release voltage of the circuit for prevention malfunction by low voltage (2.05 V Typ.), data is reloaded from the E²PROM to the register, the values of DO7 to 0 pins go back to its default.



***1.** Output from DO7 to 0 goes in "L" when the power supply voltage decreases more than the level of the detection voltage of the circuit for prevention malfunction by low voltage.

***2.** A period to define data is; the loading period from E²PROM + the period to stabilize output from DO7 to 0 pin = within 100 μs.

Figure 20 Data Loading and Timer Action Example 2

■ Flowchart of Data Loading from E²PROM and Timer Action

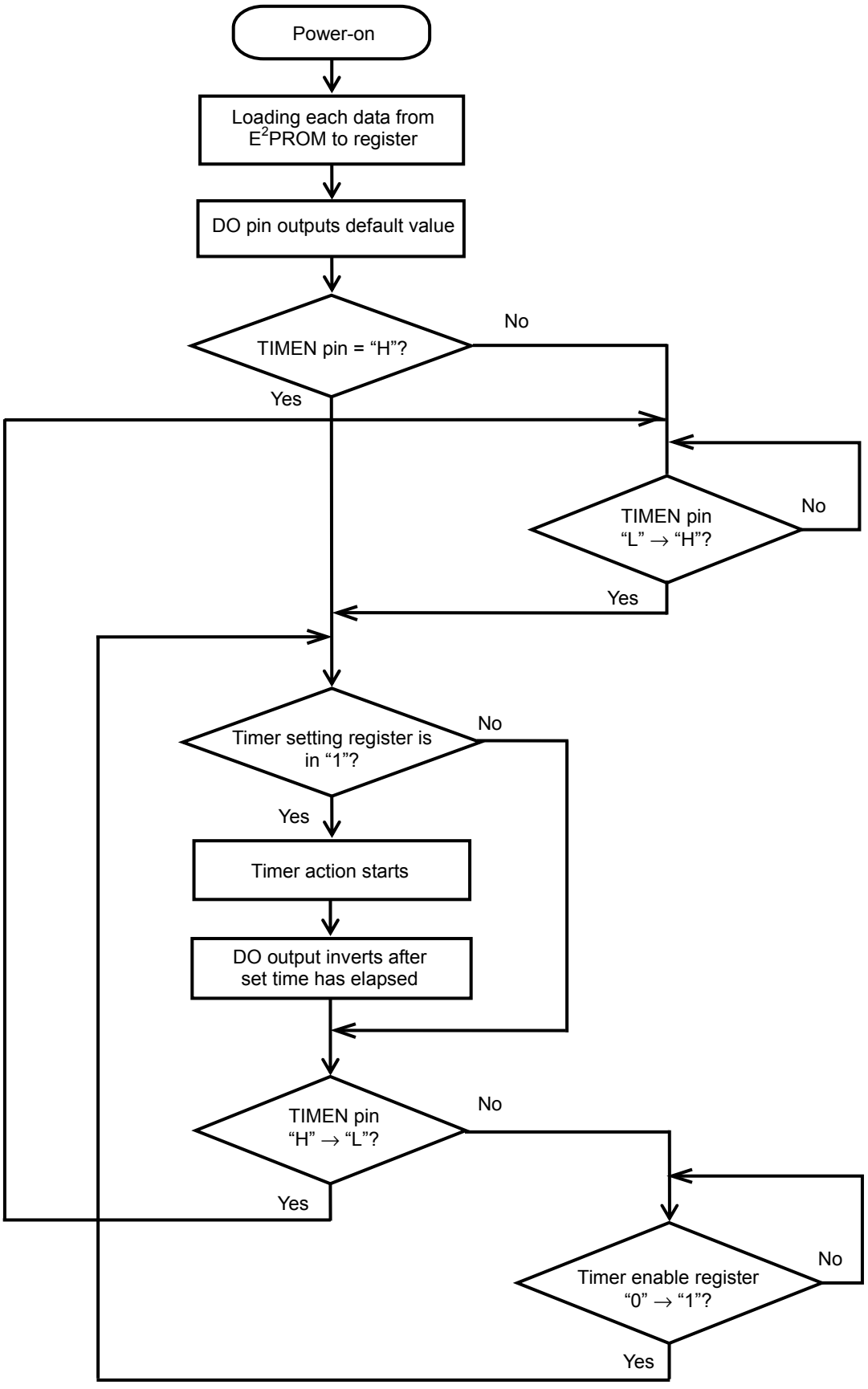


Figure 21 Flowchart of S-7760A's Action (When selecting "condition to start timer Option 1")

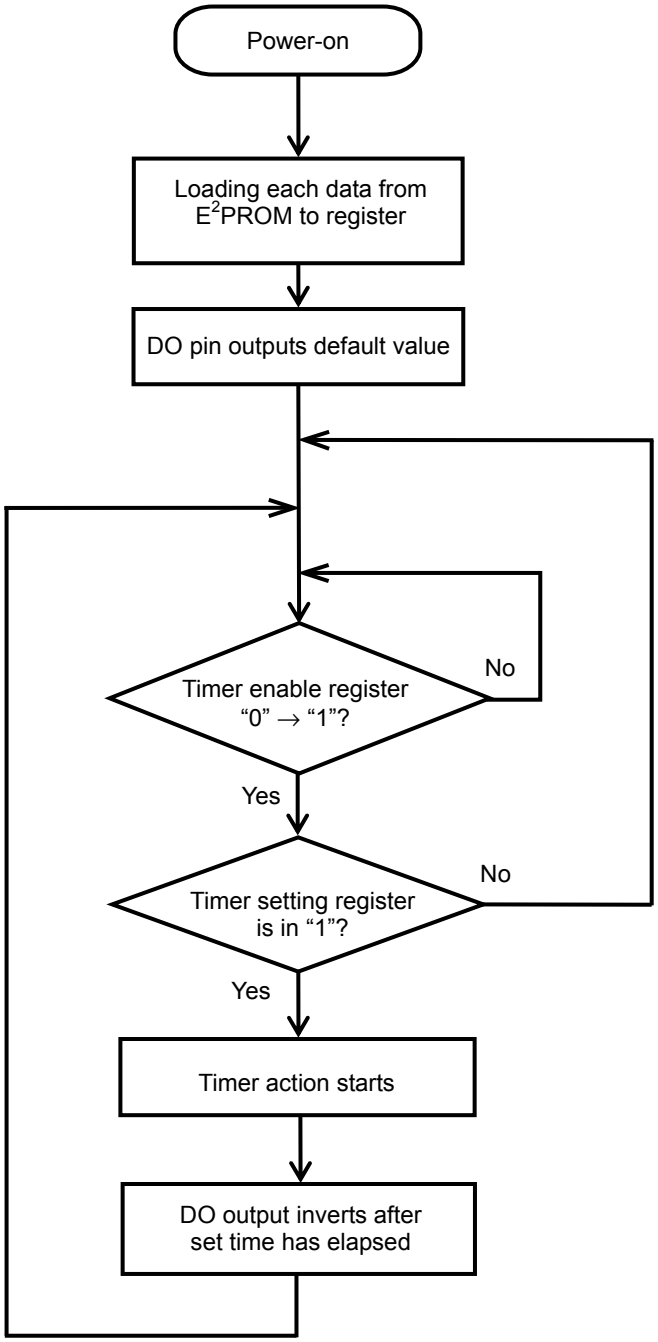


Figure 22 Flowchart of S-7760A's Action (When selecting "condition to start timer Option 2")

■ Operation

1. Start condition

A start condition starts by changing the SDA line from “H” to “L” while the SCL line is “H”. Input a start condition first when inputting a command via I²C-bus interface.

2. Stop condition

A stop condition starts by changing the SDA line from “L” to “H” while the SCL line is “H”. Input a stop condition in the end when inputting a command via I²C-bus interface.

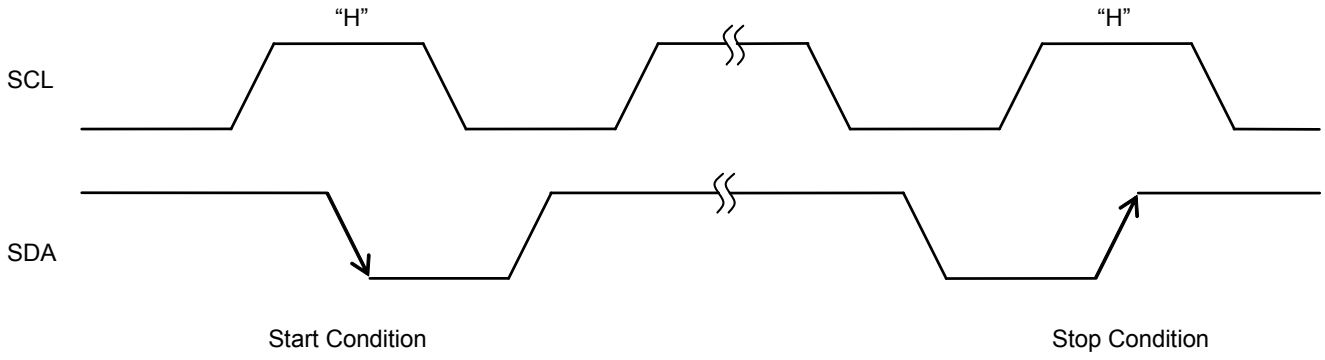


Figure 23 Start / Stop Condition

3. Data transfer

The S-7760 installs data in the SDA line at a rising edge of the SCL line.
Change the SDA line while the SCL line is “L” during the data transmission.
If changing the SDA line while the SCL line is “H”, the S-7760A goes in the start or stop condition status.

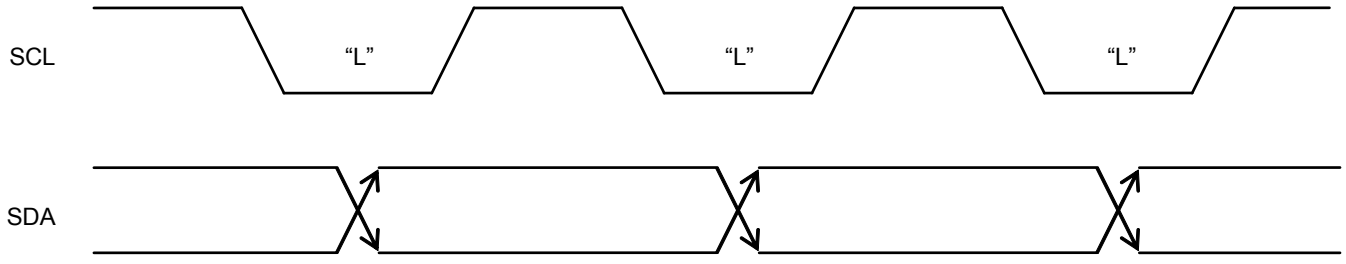


Figure 24 Data Transfer Timing

4. Acknowledgment

Data is transmitted sequentially in 8-bit. Changing the SDA line to "L" indicates that the devices on the system bus have received data, thus the devices send an acknowledgment signal back during the 9th clock of cycle.
The S-7760A does not send an acknowledgment signal back during the Write operation.

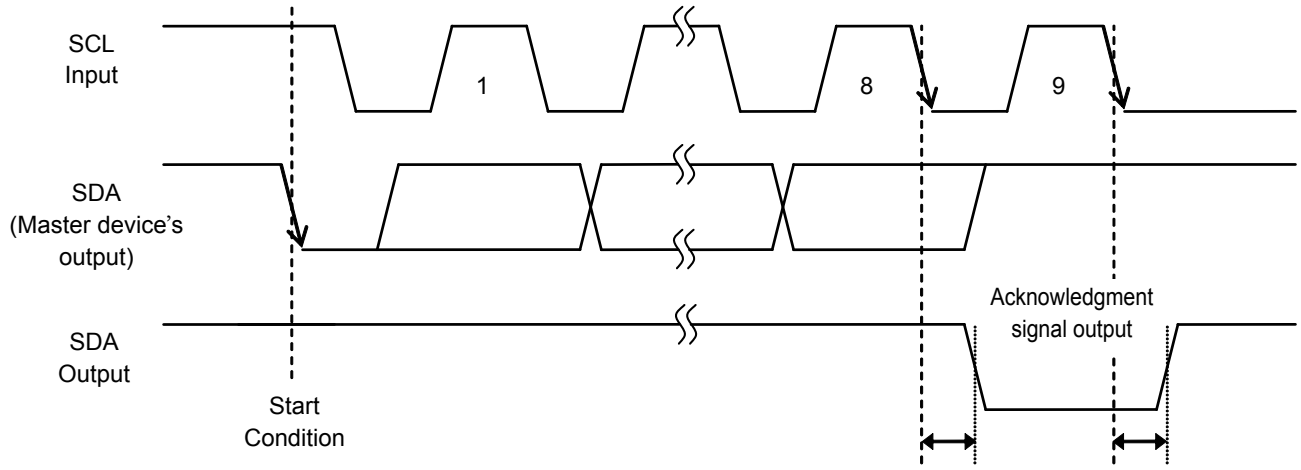


Figure 25 Acknowledgment Output Timing

5. Read operation

When this IC receives the 7-bit device address and the Read/Write instruction code "1" after receiving a start condition, it generates an acknowledgment signal.
Next, data with 8-bit length is output from this IC synchronizing with the SCL clock.
After that, the master device sends a stop condition, not an acknowledgment signal in order to finish the Read operation.

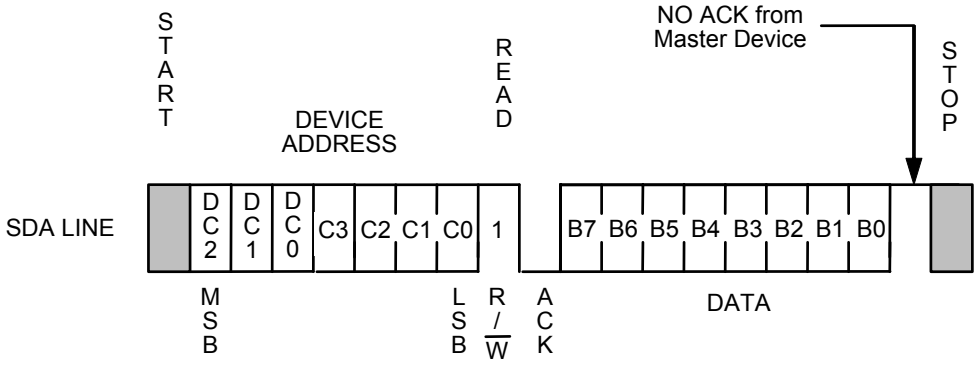


Figure 26 Read

6. Write operation

6. 1 Write

When this IC receives the 7-bit device address and the Read/Write instruction code “0” after receiving a start condition, it generates an acknowledgment signal.
Next, after it receives the 8-bit word address and generates an acknowledgment signal, it receives a stop condition to finish the Write command.
In the Write operation to the E²PROM, the Write operation starts with a stop condition, the S-7760A finishes it after the period to Write (max. 5 ms) has elapsed. During Write to the E²PROM, all operations are inhibited to be performed and the S-7760A does not send back any acknowledgment signals for command inputs.

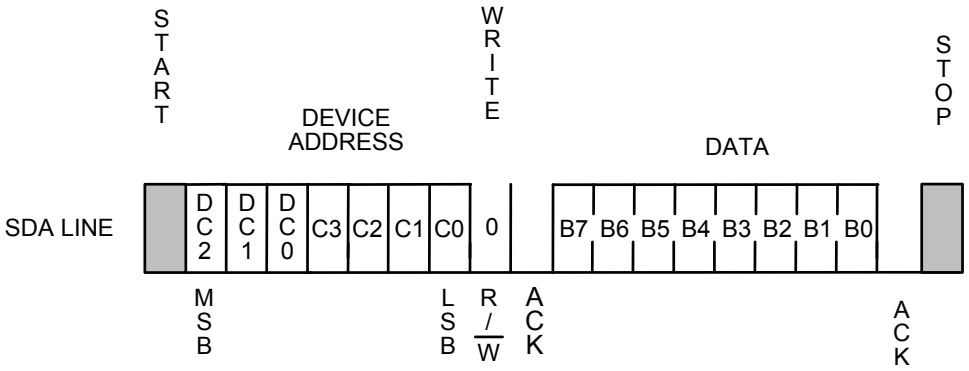


Figure 27 Write

6. 2 Write Protect

Write protect is available in the S-7760A.
When the WP pin is connected to V_{CCH}, the Write operation in all memory area is inhibited. When the WP pin is connected to GND, Write protect becomes invalid so that the Write operation in all memory area is accepted.
Fix the WP pin during the period; from rising of SCL at installing the last bit in Write data until the completion of Write period (max. 5 ms).
Written data in the address is not assured if the condition of the WP pin is changed during this period. Be sure to connect the WP pin to GND when you don’t use Write Protect. Write Protect is valid in the range of power supply voltage.

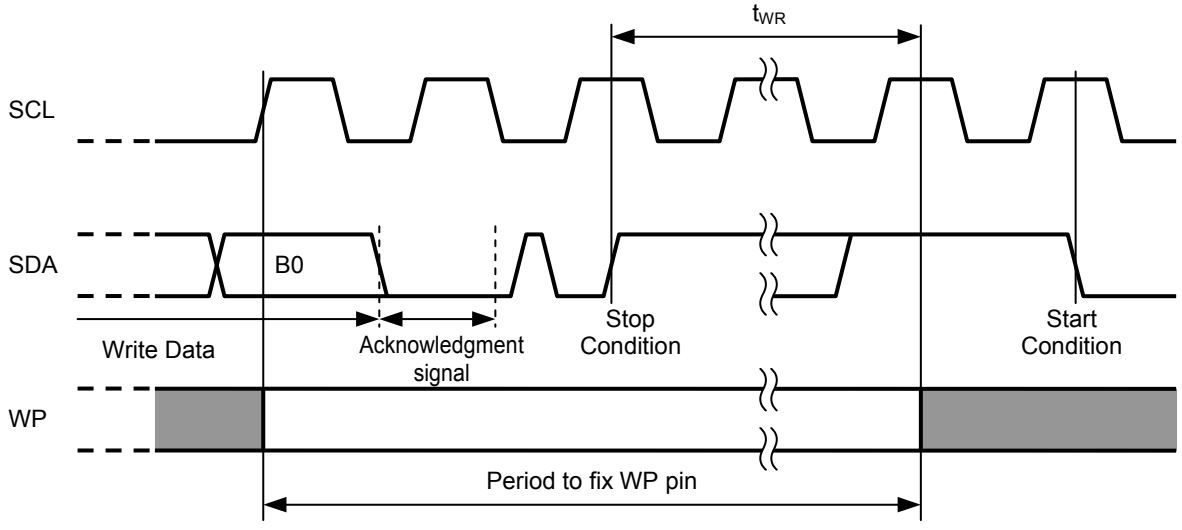


Figure 28 Period to Fix WP Pin

6. 3 Acknowledgment polling

Acknowledge polling is used to find when the Write operation has completed. After receiving a stop condition the Write operation has once started, all operations are inhibited to be performed so that the S-7760A cannot respond to the signals transmitted from the master device. The master device sends a start condition, the device address and Read/Write instruction code to the S-7760A (slave device), and detects the response from the slave device. It is possible to find when the Write operation has completed. Thus if the slave device does not send an acknowledgment signal back, the Write operation is in progress. If it sends an acknowledgment signal back, the Write operation has completed. Fix the WP pin until an acknowledgment is confirmed. It is recommended to use the Read instruction "1" for the Read/Write instruction code transmitted from the master device during acknowledgment polling.

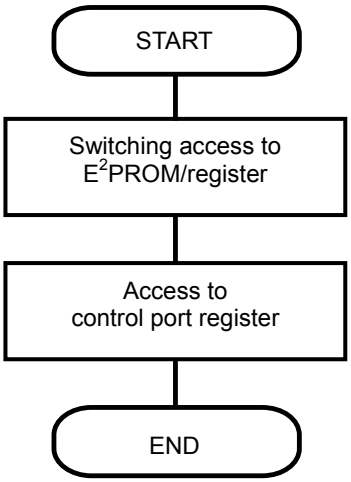
6. 4 Irregular action

In the middle of inputting Write data, if inputting a stop condition in clock less than the specified data length (8-bit), the S-7760A does not perform Write to the E²PROM. And it either does not perform Write to the E²PROM if receiving a stop condition after receiving data over 9-bit. However, data in the register has been rewritten at the point when the S-7760A has received the specified length data. Be sure not to input clock which exceeds the specified value due to noise or other causes.

■ Example of Flowchart for Software

1. Read/Write in register

The example of flowchart for software when accessing to the control port register is shown in **Figure 29**.



1-byte command

(ST, DC2 to 0, 0001, **0**, ACK, SP)*1

2-byte command

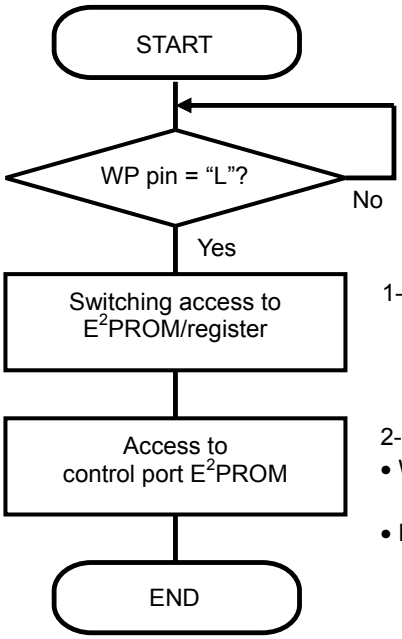
- Write
  (ST, DC2 to 0, 0101, **0**, ACK, CTR7 to 0, ACK, SP)*1
- Read
  (ST, DC2 to 0, 0101, **1**, ACK, CTR7 to 0, ACK, SP)*1

***1.** ST : Start condition
DC2 to 0 : Device code
ACK : Acknowledgment
CTR7 to 0 : Control port register
SP : Stop condition

Figure 29 Flowchart for Software Example 1

2. Read/Write in E²PROM

The example of flowchart for software when accessing to the E²PROM is shown in **Figure 30**.



1-byte command
(ST, DC2 to 0, 0001, **1**, ACK, SP)*1

2-byte command
- Write
  (ST, DC2 to 0, 0101, **0**, ACK, CTR7 to 0, ACK, SP)*1
- Read
  (ST, DC2 to 0, 0101, **1**, ACK, CTR7 to 0, ACK, SP)*1

***1.** ST : Start condition
DC2 to 0 : Device code
ACK : Acknowledgment
CTR7 to 0 : Control port register
SP : Stop condition

Figure 30 Flowchart for Software Example 2

■ Write Protect Function during the Low Power Supply Voltage

The S-7760A has a built-in detection circuit which operates with the low power supply voltage, cancels Write when the power supply voltage drops and power-on. Its detection voltage is 1.75 V (Typ.) and the release voltage is 2.05 V (Typ.), and its hysteresis is approx. 0.3 V.
The S-7760A cancels Write by detecting a low power supply voltage when it receives a stop condition.
Both in the data transmission and the Write operation, data in the address written during the low power supply voltage is not assured.

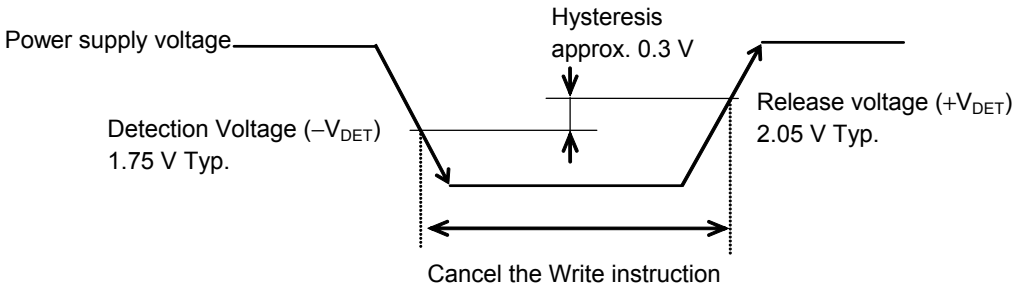


Figure 31 Operation during Low Power Voltage

■ How to Use S-7760A

1. SDA I/O pin and SCL input pin

In consideration of I²C-bus protocol function, the SDA I/O and SCL input pins*1 should be connected with a pull-up resister of 1 to 5 kΩ.
The S-7760A cannot transmit normally without using a pull-up resistor.

***1.** In the case that the SCL input pin of the S-7760A is connected to the tri-state output pin in the master device, connect the SCL input pin with a pull-up resistor as well in order not to set the SCL input pin in high impedance. This prevents the S-7760A from error caused by high impedance from the tri-state pin when resetting the master device during the voltage drop.

The bus pull-down function is available for S-7760A by option because it is assumed that the pull-up power supply may be in high impedance depending on case. Except for this IC, if users do not have an element to fix the potentials of SDA and SCL pins, set BPDX in "L" output in order to pull down the SDA and SCL pins.

2. Reset after transmission interruption

This IC does not have a pin to reset, but it generally resets the internal circuit by inputting a stop or start condition. However, in case that transmission is interrupted, for example, only the master device is reset because the power supply voltage drops during transmission; the internal circuit maintains the status before interruption. If the status is that the SDA pin outputs "L" (outputs an acknowledge signal or in Read), this IC does not perform the next operation because it cannot receive a start or stop condition from the master device. Therefore it is necessary to finish outputting an acknowledgment signal and the Read operation in SDA. **Figure 32** shows how to reset.
First, input a start condition. (While the SDA pin is outputting "L", the S-7760A does not go in the start condition but this "L" output does not affect on the slave device.) Next, input clock (27 clocks) which is equivalent to 3-byte data access from the SCL pin. During this procedure, pull up the SDA line which is connected closer to the master device.
Due to this, the SDA pin's I/O prior to transmission interruption ends so that the SDA pin goes in "H". After that, by inputting a stop condition, the S-7760A returns to the status possible to perform the general transmission. It is recommended to perform this reset when you initialize, after power-on the master device. A circuit for prevention malfunction by a low power supply voltage is equipped in this IC, thus it automatically resets internally when a low voltage is applied to this IC.

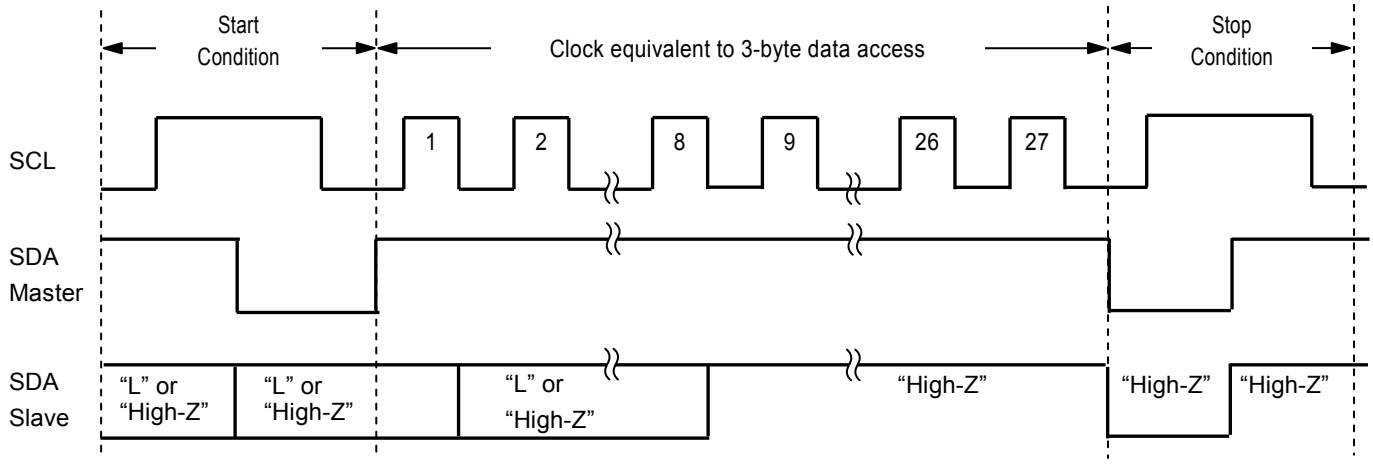


Figure 32 How to Reset S-7760A

3. Acknowledgment check

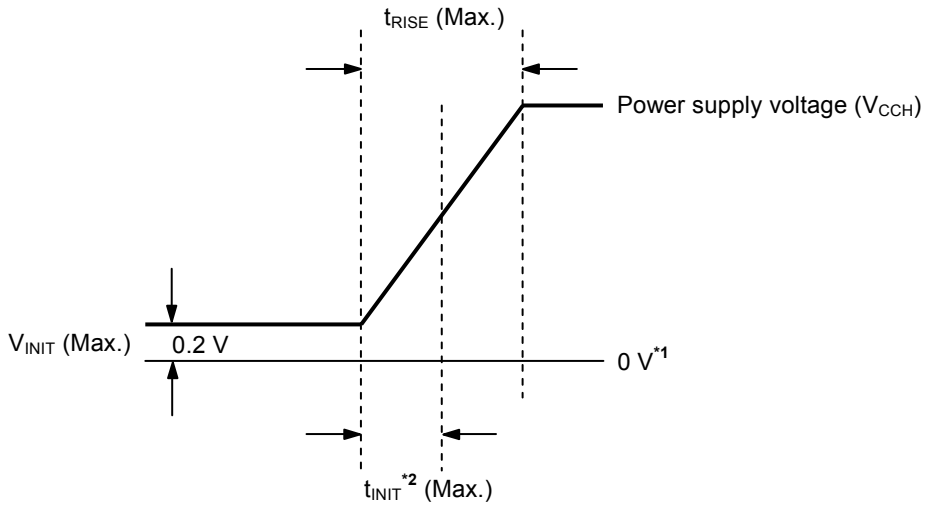
The I²C-bus protocol includes an acknowledgment check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the master device and the S-7760A.

4. Built-in power-on-clear circuit

The S-7760A has a built-in power-on-clear circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-clear circuit normally, the following conditions must be satisfied to raise the power supply voltage.

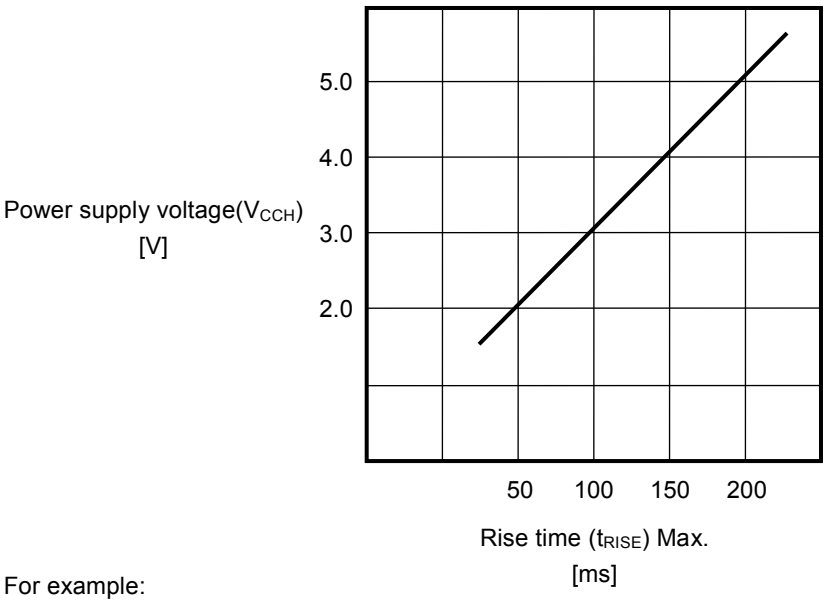
4. 1 Raising power supply voltage

As shown in **Figure 33**, raise the power supply voltage from 0.2 V max., within the time defined as t_{RISE} which is the time required to reach the power supply voltage to be set.
For example, if the power supply voltage is 3.0 V, t_{RISE} = 100 ms as seen in **Figure 34**. The power supply voltage must be raised within 100 ms.



***1.** 0 V means there is no difference in potential between the VCCH pin and the VSS pin of the S-7760A.
***2.** t_{INIT} is the time required to initialize the S-7760A. No instructions are accepted during this time.

Figure 33 Raising Power Supply Voltage



For example:

If your S-7760A's supply voltage = 3.0 V, raise the power supply voltage to 3.0 V within 100 ms.

Figure 34 Raising Time of Power Supply Voltage

When initialization is successfully completed by the power-on-clear circuit, the S-7760A enters the standby status. If the power-on-clear circuit does not operate, the followings are the possible causes.

(1) Because the S-7760A has not completed initialization, an instruction previously input is still valid or an instruction may be inappropriately recognized. In this case, S-7760A may perform the Write operation.

(2) The voltage drops due to power off while the S-7760A is being accessed. Even if the master device is reset due to the low power voltage, the S-7760A may malfunction unless the conditions for the power-on-clear operation are satisfied.

4. 2 Initialization time

The S-7760A initializes at the same time when the power supply voltage is raised. Input instructions to the S-7760A after initialization. The S-7760A does not accept any instruction during initialization.
Figure 35 shows the initialization time of the S-7760A.

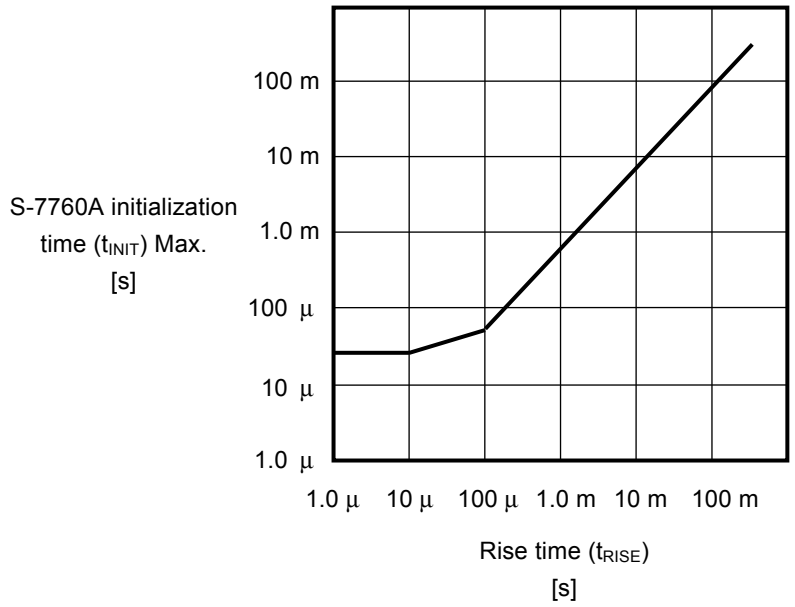


Figure 35 Initialization Time of S-7760A

5. Data hold time ($t_{HD.\ DAT}$ = 0 ns)

If SCL and SDA of the S-7760A are changed at the same time, the timing which takes to reach this IC slightly lags due to a load on the bus line. As a result, the change in the SDA precedes a falling edge of SCL so that S-7760A may recognize a start/stop condition.
To avoid this, in the S-7760A, it is recommended to set the delay time of over 0.3 µs for a falling edge of SCL.
In its specs, it is described as the S-7760A works at 0 ns of data hold time, however, take account into the above action in actual use.

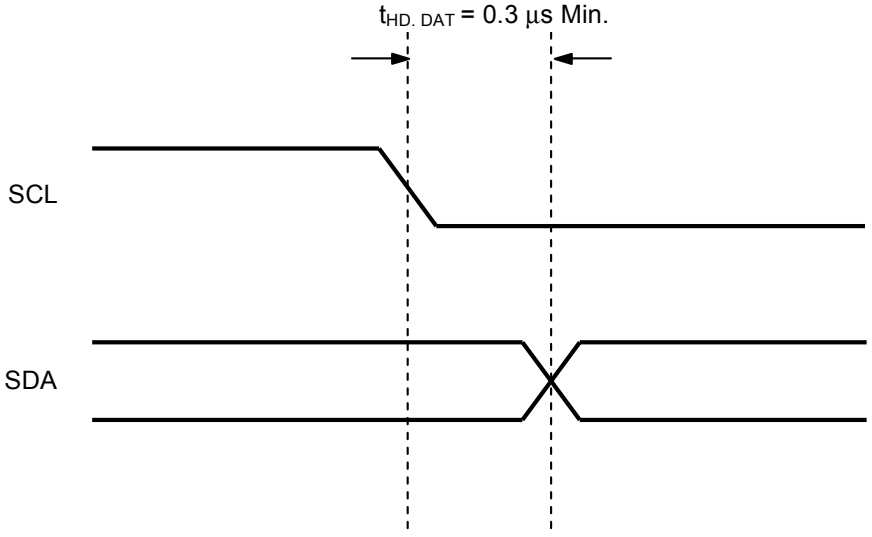


Figure 36 Data Hold Time

6. SDA pin and SCL pin noise suppression time

The S-7760A includes a built-in low-pass filter at the SDA and SCL pins to suppress noise.
This filter suppresses noise with the width of less than 130 ns when the power supply voltage is 3.0 V.
Refer to noise suppression time (t_I) in **Table 10** regarding details of the assurable value.

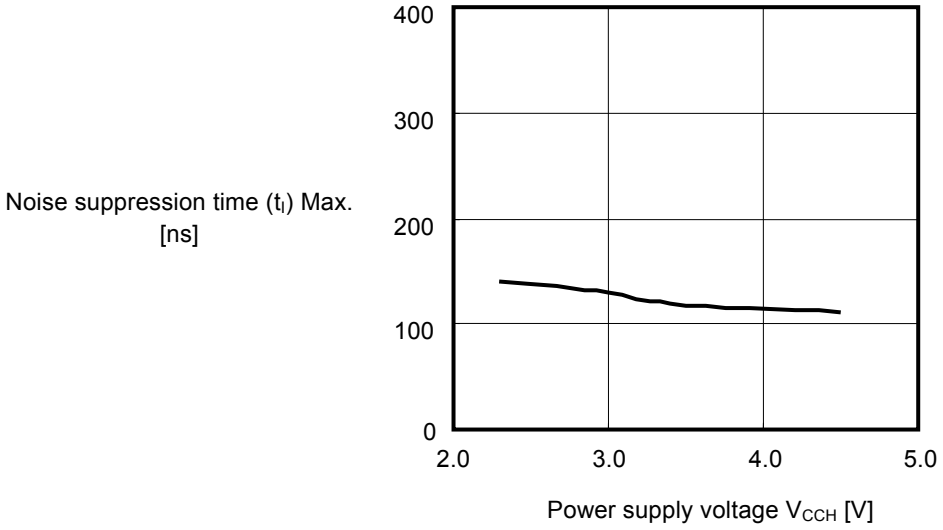


Figure 37 Noise Suppression Time for SDA and SCL Pins (CMOS input type)

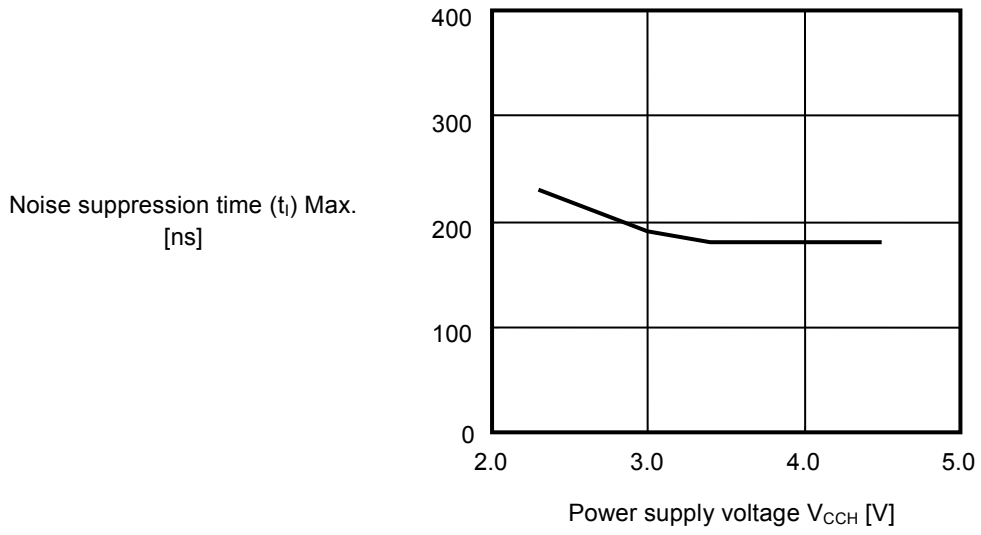


Figure 38 Noise Suppression Time for SDA and SCL Pins (Low voltage input type)

■ Precautions

- Semiconductor devices must be used within the absolute maximum rating. Special caution is required for the supply voltage. A momentary surge voltage exceeding the rated value may cause latch-up and malfunction. Confirm the detailed usage conditions required for each parameter by referring to the data sheet before use.
- If the S-7760A operates with moisture remaining in the circuits, a short circuit may occur between pins, causing a malfunction. When the S-7760A is taken out of the constant-low-temperature bath during evaluation, the pins of the S-7760A may be frosted. Note that, if the S-7760A is operated with the pins frosted, the pins may be short-circuited by moisture, causing a malfunction.
  The same applies when the S-7760A is used in an environment where condensation may occur, so care is required.
- Although the IC contains a static electricity protection circuit, static electricity that exceeds the limit of the protection circuit should not be applied.
- SII Semiconductor Corporation assumes no responsibility for the way in which this IC is used in products created using this IC or for the specifications of that product, nor does SII Semiconductor Corporation assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

■ Precautions for WLP Package

- The device's silicon substrate side is exposed to the marking side of the device package. Since this portion has a lower strength against mechanical stress than a standard plastic package, take sufficient care to avoid chips and cracks when handling the package. Moreover, the exposed side of the silicon has the electrical potential of the device substrate, and needs to be kept out of contact with the external potential.
- In this package, the transistor area side is overcoated with a translucent resin. Keep in mind that the characteristics of the package may be affected if the device is exposed under an intensive light source.

■ Option

The explanation of seven options which are available for this IC and the option tables are shown here. When selecting the option, follow these descriptions.

1. Device code (8 types)

Selecting the arbitrary device address code is available (Refer to **Figure 13**).

Table 14 Option List of Device Code

No.	C2	C1	C0
Opt10	0	0	0
Opt11	0	0	1
Opt12	0	1	0
Opt13	0	1	1
Opt14	1	0	0
Opt15	1	0	1
Opt16	1	1	0
Opt17	1	1	1

2. Internal generation of oscillation CLK/External input

Although this IC has an oscillation circuit for generating delay time, without operating this circuit, it is also possible to use this IC's external oscillation CLK for generating delay time.

Table 15 Option List of Oscillation CLK

No.	Internal/External
Opt20	Using an internal oscillation circuit
Opt21	Using an external oscillation circuit

3. Delay time

Delay time is selectable in the following settings (T' : Oscillation CLK cycle (approx. 5 μs when using an internal oscillation circuit).

Table 16 Option List of Delay Time

No.	Timer scale setting register	
	1: Delay time for short-time setting (T)	0: Delay time for long-time setting (LT)
Opt30	T' × 1	T' × 64
Opt31	T' × 2	T' × 128

4. TIMEN/RESX pin

Users can select whether to use a pin as TIMEN or RESX.

Table 17 Option List of TIMEN/RESX

No.	Function
Opt40	TIMEN
Opt41	RESX

5. CLK/BPDX pin

Users can select whether to use a pin as CLK or BPDX.

Table 18 Option List of CLK/BPDX

No.	Function
Opt50	CLK
Opt51	BPDX

6. Condition to start timer

For the lower output ports 4 channels, users can select the condition to start a timer at each port.

Table 19 Option List of Condition to Start Timer

Output	No.	Condition to start timer
DO0	Opt60	(Power on and TIMEN = High) or (TIMEN = Low to High) or (TEN0 = 0 to 1 and TIMEN = High)
	Opt61	TEN0 = 0 to 1
DO1	Opt70	(Power on and TIMEN = High) or (TIMEN = Low to High) or (TEN1 = 0 to 1 and TIMEN = High)
	Opt71	TEN1 = 0 to 1
DO2	Opt80	(Power on and TIMEN = High) or (TIMEN = Low_to_High) or (TEN2 = 0 to 1 and TIMEN = High)
	Opt81	TEN2 = 0 to 1
DO3	Opt90	(Power on and TIMEN = High) or (TIMEN = Low to High) or (TEN3 = 0 to 1 and TIMEN = High)
	Opt91	TEN3 = 0 to 1

7. High/low leveled input voltage type for pin

Users can select the input voltage types either high or low level for the SDA, SCL and TIMEN pins.

Table 20 Option List of High/low Leveled Input Voltage

No.	Function
Opt100	CMOS input type
Opt101	Low voltage input type

■ Option Format

Please fill in check in this table and send to our sales office when you order the option.

Item	No.	Option	Fill in check here
Device code DC2 to 0	Opt10	0,0,0	
	Opt11	0,0,1	
	Opt12	0,1,0	
	Opt13	0,1,1	
	Opt14	1,0,0	
	Opt15	1,0,1	
	Opt16	1,1,0	
	Opt17	1,1,1	
Oscillation clock	Opt20	Using an internal oscillation circuit	
	Opt21	Using an external oscillation circuit	
Delay time and timer scale	Opt30	T' × 1 , T' × 64	
	Opt31	T' × 2 , T' × 128	
Pin function Option 1	Opt40	TIMEN	
	Opt41	RESX	
Pin function Option 2	Opt50	CLK	
	Opt51	BPDX	
DO0 condition to start timer	Opt60	(Power on and TIMEN = "H") or (TIMEN = "L" to "H") or (TEN0 = 0 to 1 and TIMEN = "H")	
	Opt61	TEN0 = 0 to 1	
DO1 condition to start timer	Opt70	(Power on and TIMEN = "H") or (TIMEN = "L" to "H") or (TEN1 = 0 to 1 and TIMEN = "H")	
	Opt71	TEN1 = 0 to 1	
DO2 condition to start timer	Opt80	(Power on and TIMEN = "H") or (TIMEN = "L" to "H") or (TEN2 = 0 to 1 and TIMEN = "H")	
	Opt81	TEN2 = 0 to 1	
DO3 condition to start timer	Opt90	(Power on and TIMEN = "H") or (TIMEN = "L" to "H") or (TEN3 = 0 to 1 and TIMEN = "H")	
	Opt91	TEN3 = 0 to 1	
High/low leveled input voltage for pin	Opt100	CMOS input type	
	Opt101	Low voltage input type	

■ Table for Write data to E²PROM

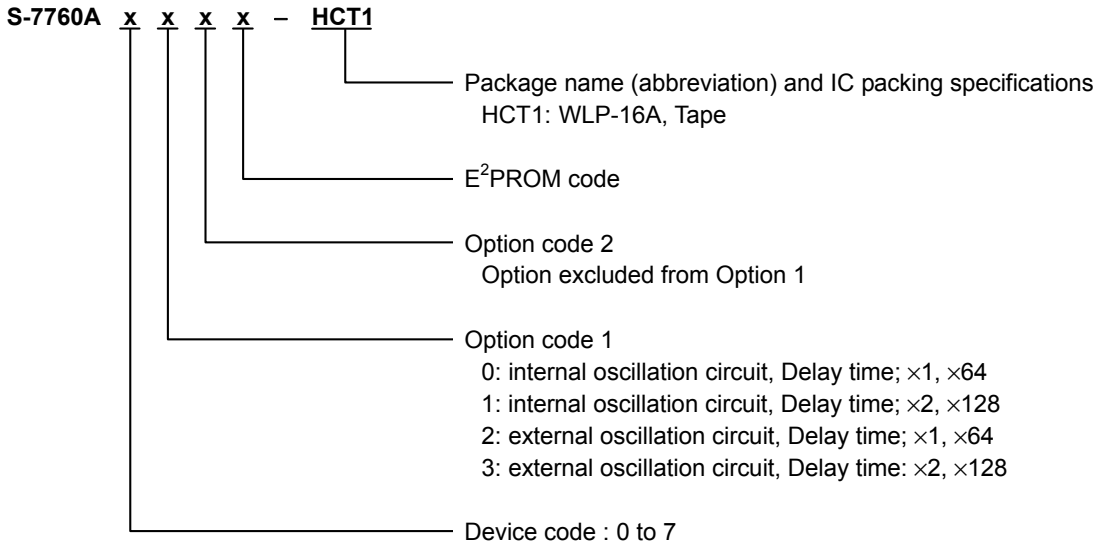
Please fill this table and send to our sales office when you order Write data to E²PROM.

E²PROM (Command code)	Write data	Default	Remark
Control port (0101)		00H	–
Timer scale setting (0110)		FFH	1: Short-time, 0; Long-time
D0 timer setting (1000)		00H	1 for time that you select, 0 for others
D1 timer setting (1001)		00H	1 for time that you select, 0 for others
D2 timer setting (1010)		00H	1 for time that you select, 0 for others
D3 timer setting (1011)		00H	1 for time that you select, 0 for others

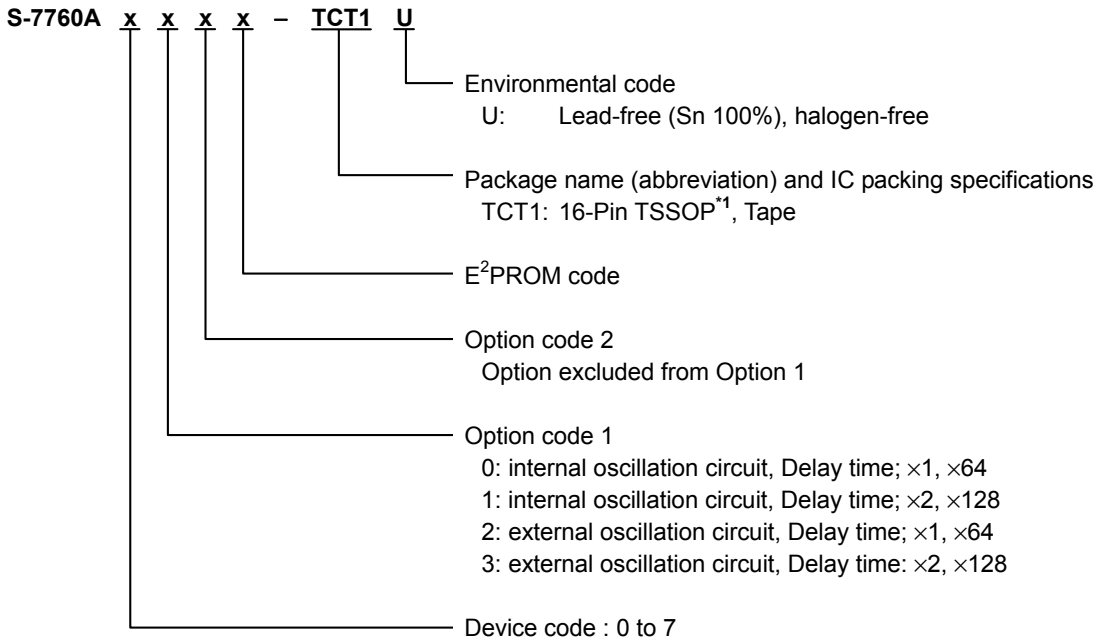
■ Product Name Structure

1. Product name

1. 1 WLP-16A



1. 2 16-Pin TSSOP



***1.** Under development

2. Package

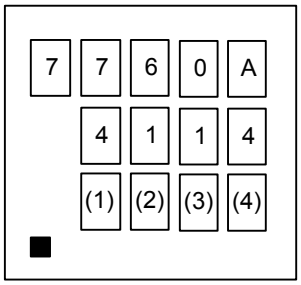
Package Name	Drawing Code		
	Package	Tape	Reel
WLP-16A	HA016-C-P-SD	HA016-C-C-SD	HA016-C-R-SD
16-Pin TSSOP*1	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-S1

***1.** Under development

■ Marking Specification

(1) WLP-16A

WLP-16A
Top view



(1) to (4) : Lot number

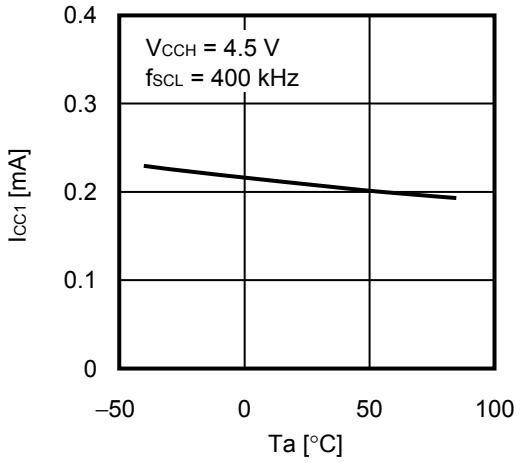
This is an example in S-7760A4114

Remark Contact our sales office regarding information on marking that you use.

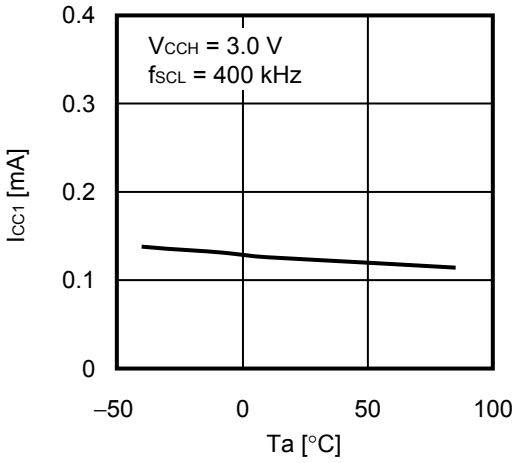
■ Characteristics (Typical Data)

1. DC Characteristics

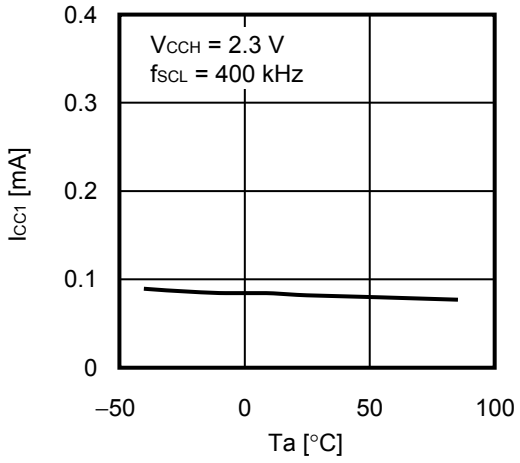
1. 1 Current consumption (READ) I_{CC1} vs. Ambient temperature Ta



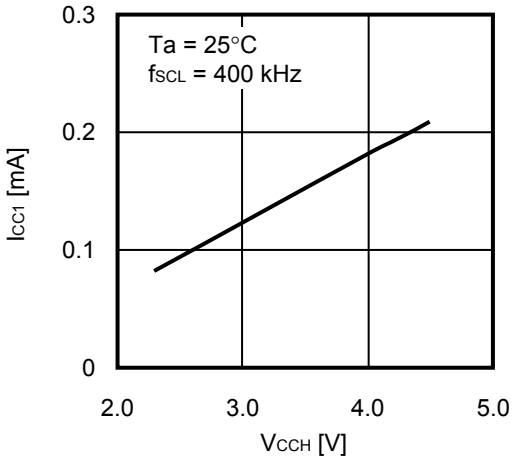
1. 2 Current consumption (READ) I_{CC1} vs. Ambient temperature Ta



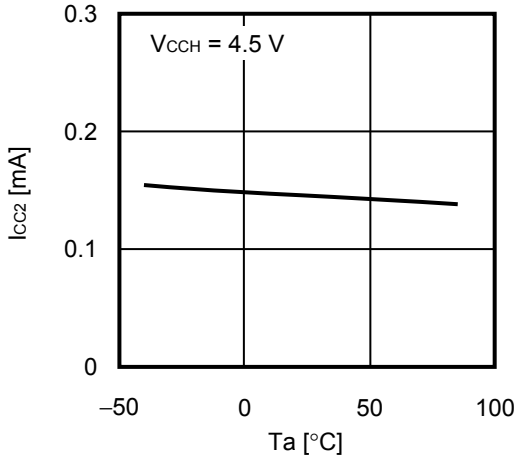
1. 3 Current consumption (READ) I_{CC1} vs. Ambient temperature Ta



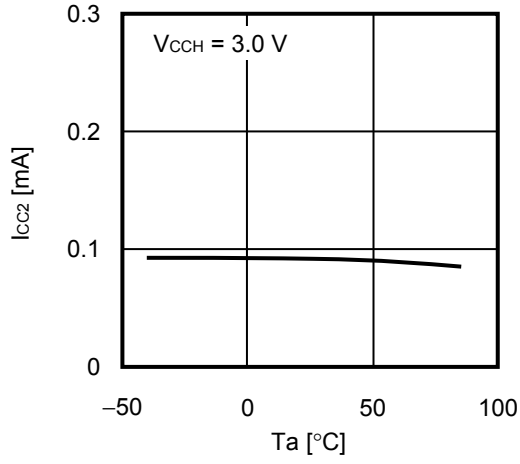
1. 4 Current consumption (READ) I_{CC1} vs. Power supply voltage V_{CCH}



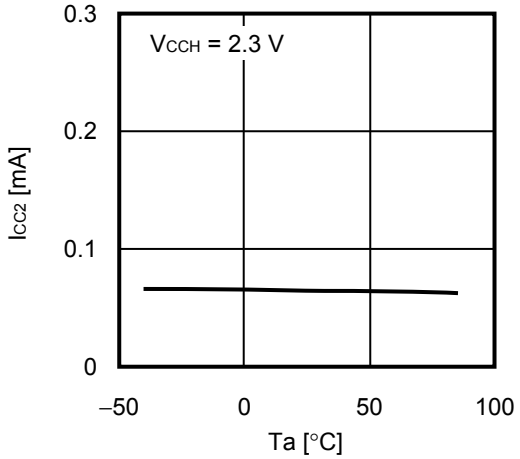
1. 5 Current consumption (PROGRAM) I_{CC2} vs. Ambient temperature Ta



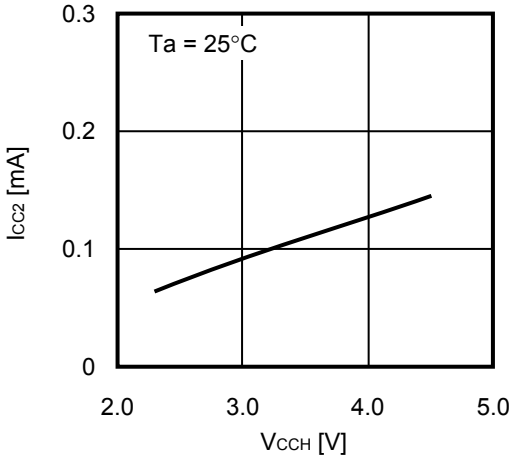
1. 6 Current consumption (PROGRAM) I_{CC2} vs. Ambient temperature Ta



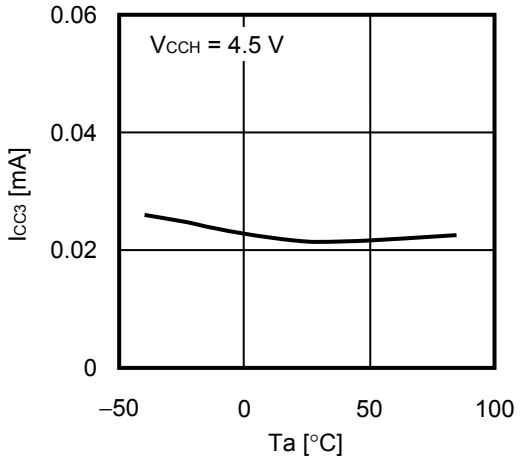
1. 7 Current consumption (PROGRAM) I_{CC2} vs. Ambient temperature Ta



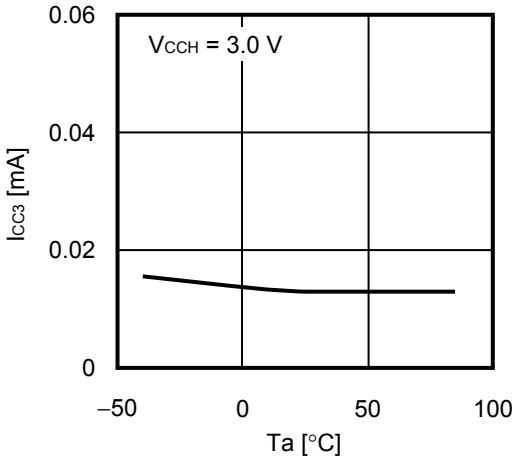
1. 8 Current consumption (PROGRAM) I_{CC2} vs. Power supply voltage V_{CCH}



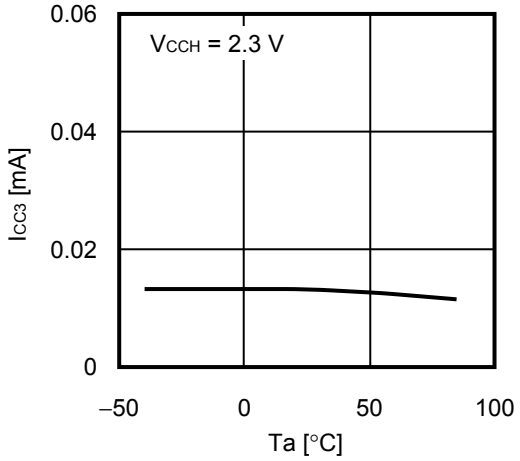
1. 9 Internal oscillator current consumption during operation I_{CC3} vs. Ambient temperature Ta



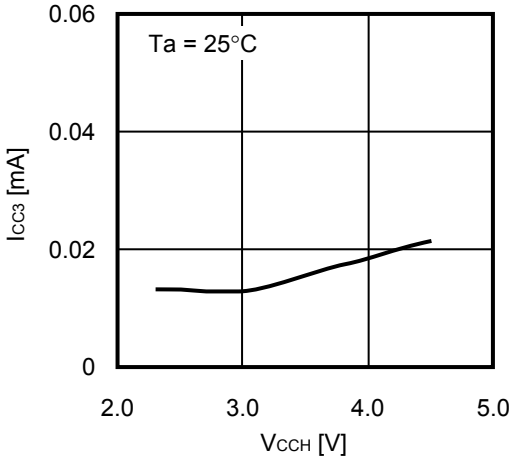
1. 10 Internal oscillator current consumption during operation I_{CC3} vs. Ambient temperature Ta



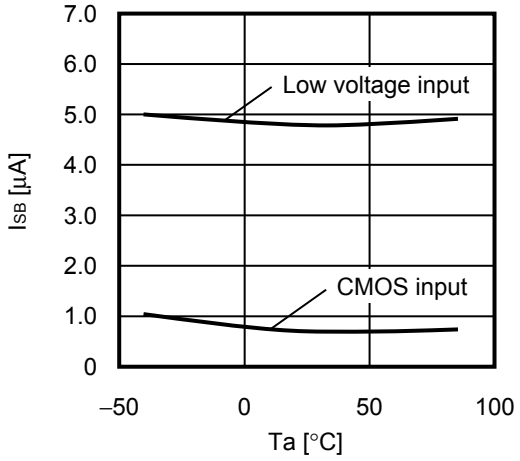
1. 11 Internal oscillator current consumption during operation I_{CC3} vs. Ambient temperature Ta



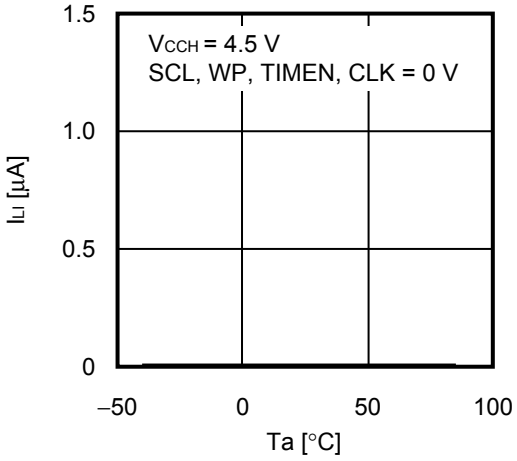
1. 12 Internal oscillator current consumption during operation I_{CC3} vs. Power supply voltage V_{CCH}



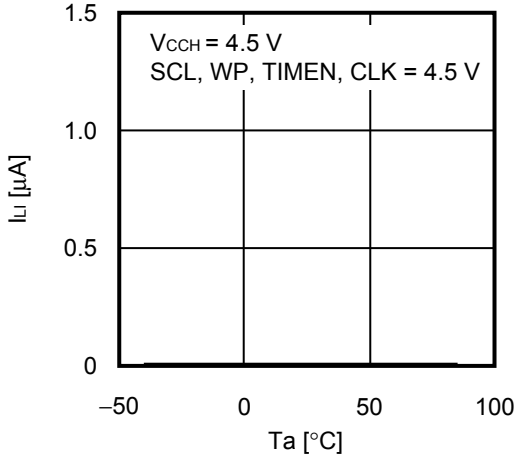
1. 13 Standby current consumption I_{SB} vs. Ambient temperature Ta



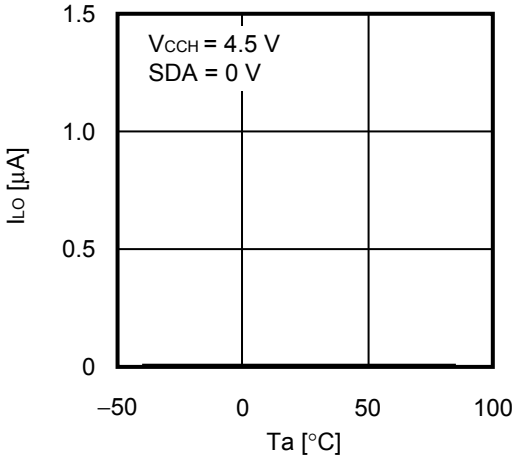
1. 14 Input leakage current I_{LI} vs. Ambient temperature Ta



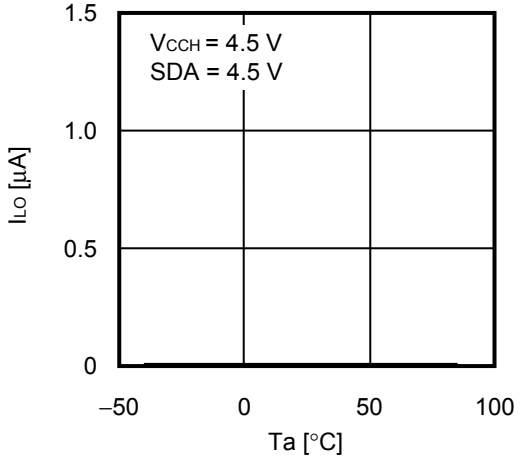
1. 15 Input leakage current I_{LI} vs. Ambient temperature Ta



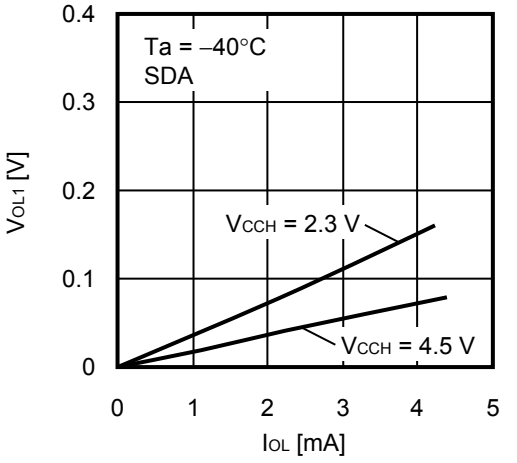
1. 16 Output leakage current I_{LO} vs. Ambient temperature Ta



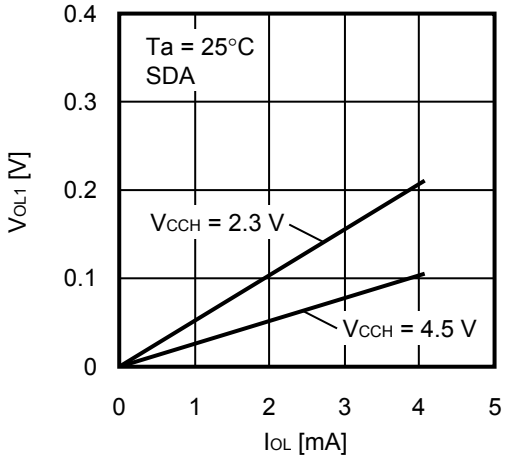
1. 17 Output leakage current I_{LO} vs. Ambient temperature Ta



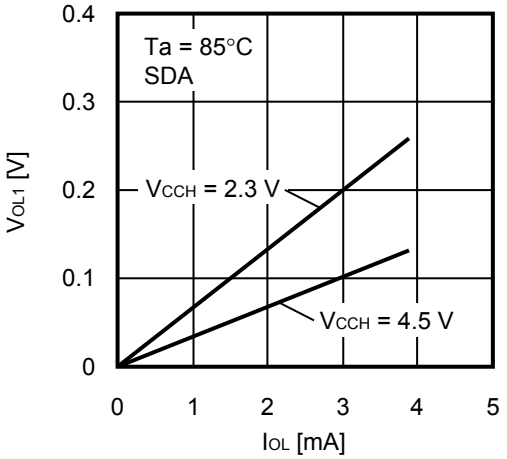
1. 18 Low level output voltage V_{OL1} vs. Low level output current I_{OL}



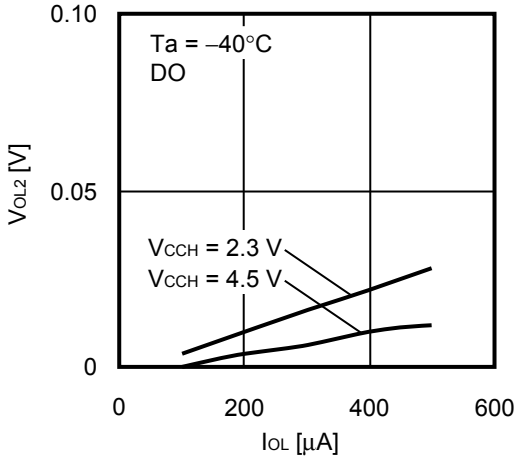
1. 19 Low level output voltage V_{OL1} vs. Low level output current I_{OL}



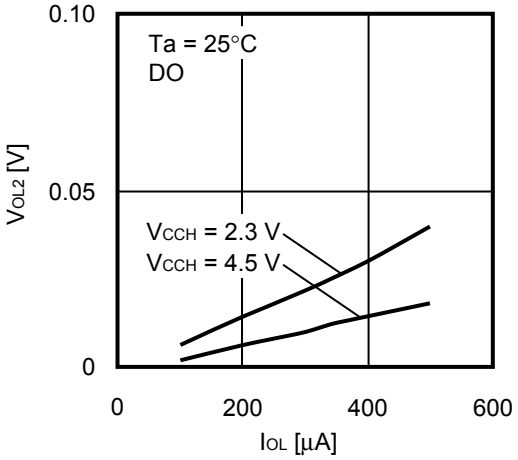
1. 20 Low level output voltage V_{OL1} vs. Low level output current I_{OL}



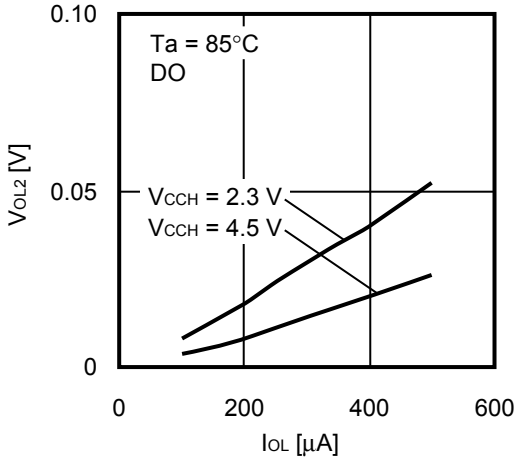
1. 21 Low level output voltage V_{OL2} vs. Low level output current I_{OL}



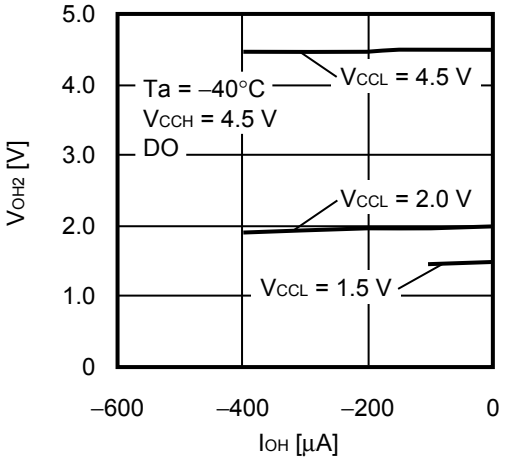
1. 22 Low level output voltage V_{OL2} vs. Low level output current I_{OL}



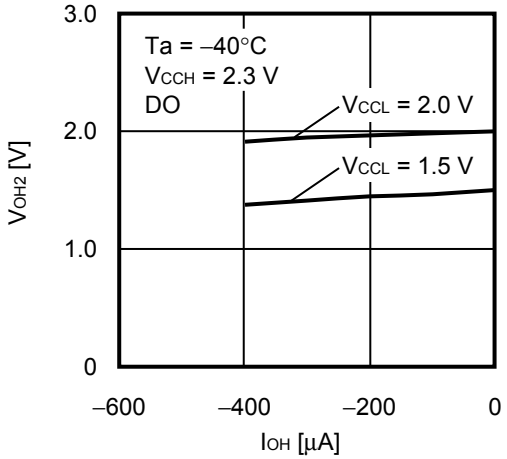
1. 23 Low level output voltage V_{OL2} vs. Low level output current I_{OL}



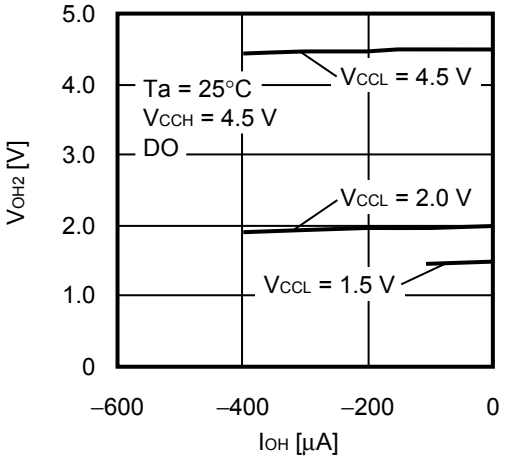
1. 24 High level output voltage V_{OH2} vs. High level output current I_{OH}



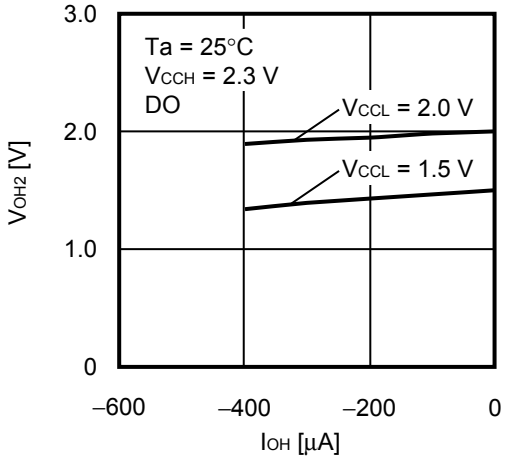
1. 25 High level output voltage V_{OH2} vs. High level output current I_{OH}



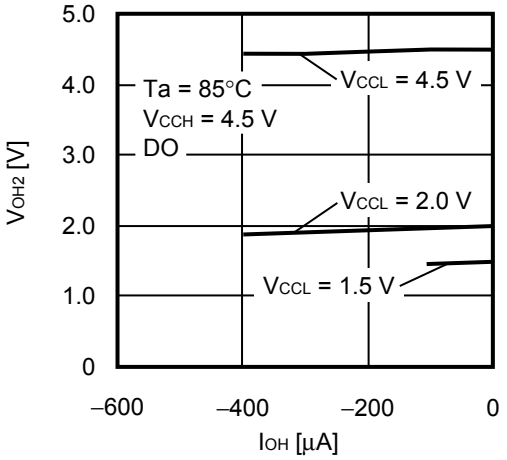
1. 26 High level output voltage V_{OH2} vs. High level output current I_{OH}



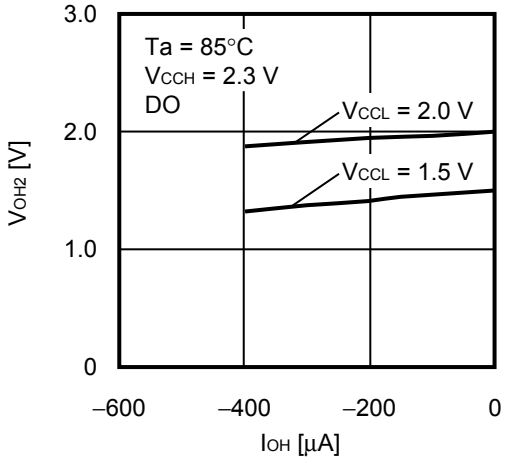
1. 27 High level output voltage V_{OH2} vs. High level output current I_{OH}



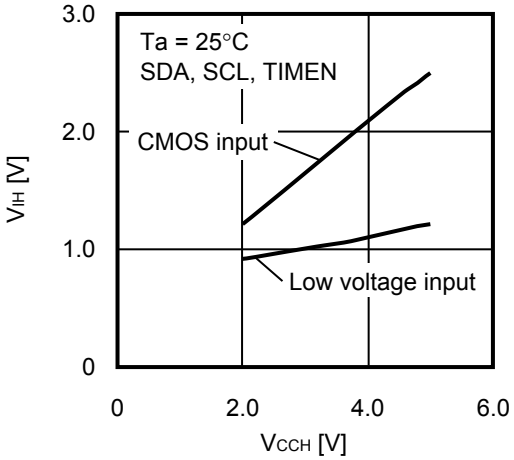
1. 28 High level output voltage V_{OH2} vs. High level output current I_{OH}



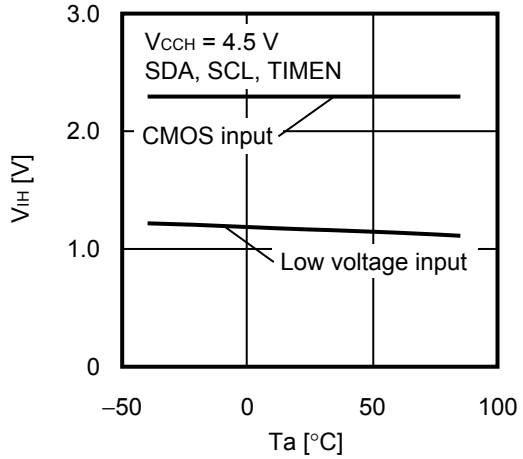
1. 29 High level output voltage V_{OH2} vs. High level output current I_{OH}



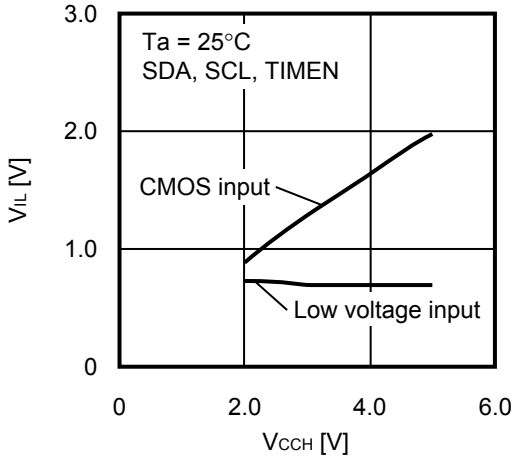
1. 30 High level input inversion voltage V_{IH} vs. Power supply voltage V_{CCH}



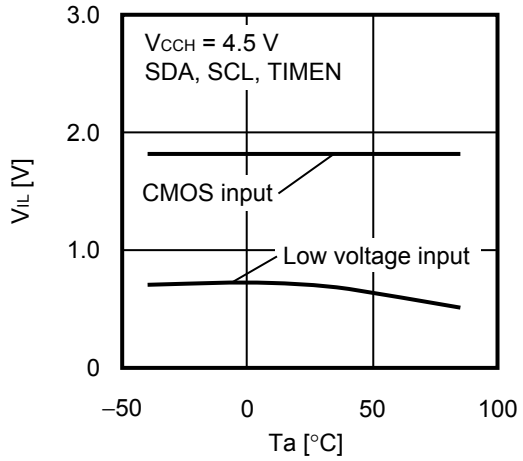
1. 31 High level input inversion voltage V_{IH} vs. Ambient temperature Ta



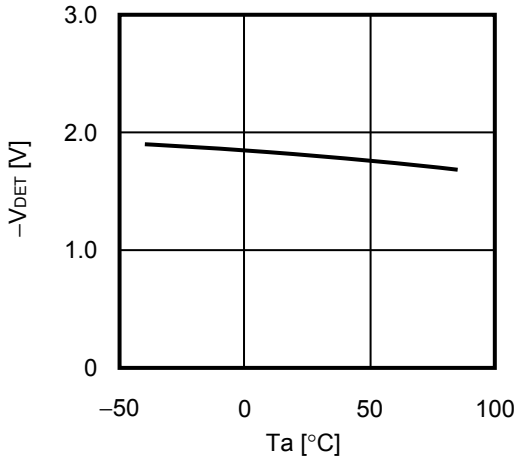
1. 32 Low level input inversion voltage V_{IL} vs. Power supply voltage V_{CCH}



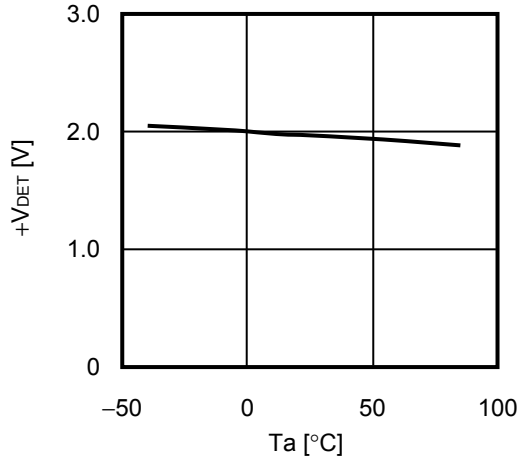
1. 33 Low level input inversion voltage V_{IL} vs. Ambient temperature Ta



1. 34 Low power supply detection voltage $-V_{DET}$ vs. Ambient temperature Ta

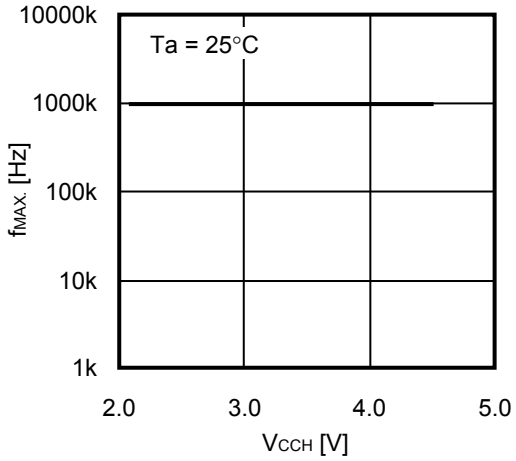


1. 35 Low power supply release voltage $+V_{DET}$ vs. Ambient temperature Ta

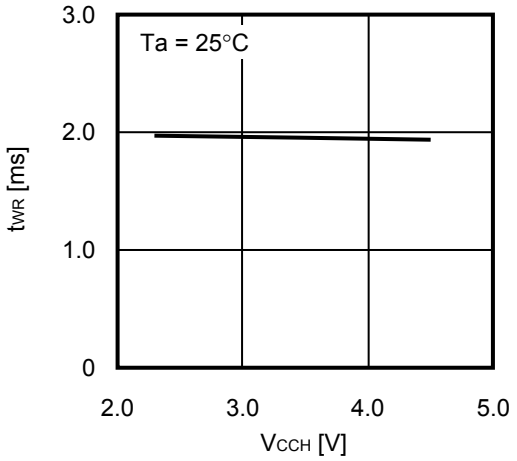


2. AC Characteristics

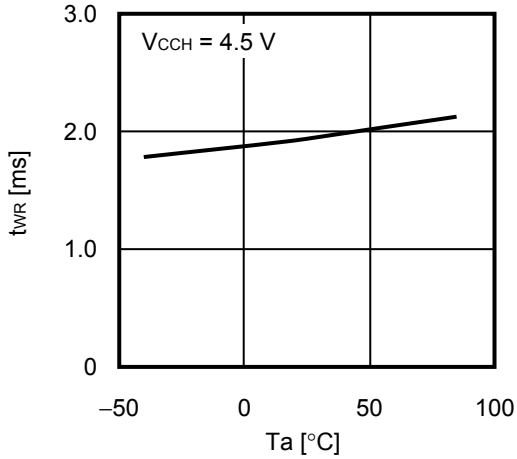
2. 1 Maximum operating frequency $f_{MAX.}$ vs. Power supply voltage V_{CCH}



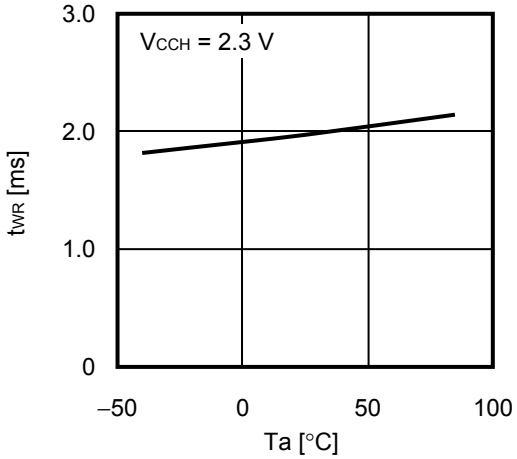
2. 2 Write time t_{WR} vs. Power supply voltage V_{CCH}



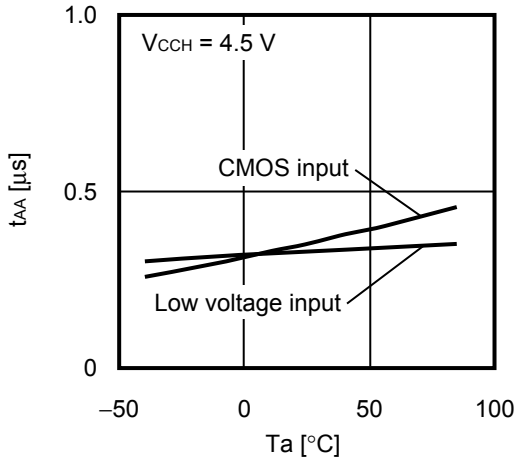
2. 3 Write time t_{WR} vs. Ambient temperature Ta



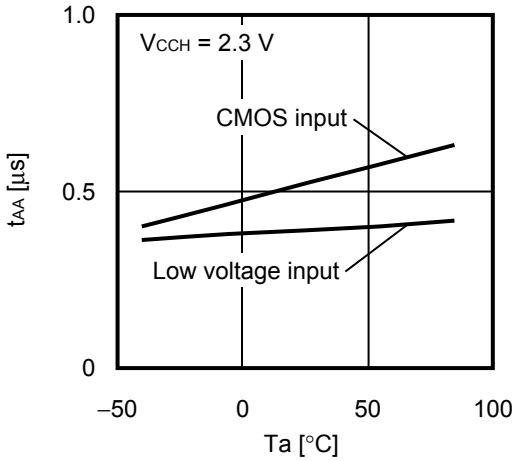
2. 4 Write time t_{WR} vs. Ambient temperature Ta

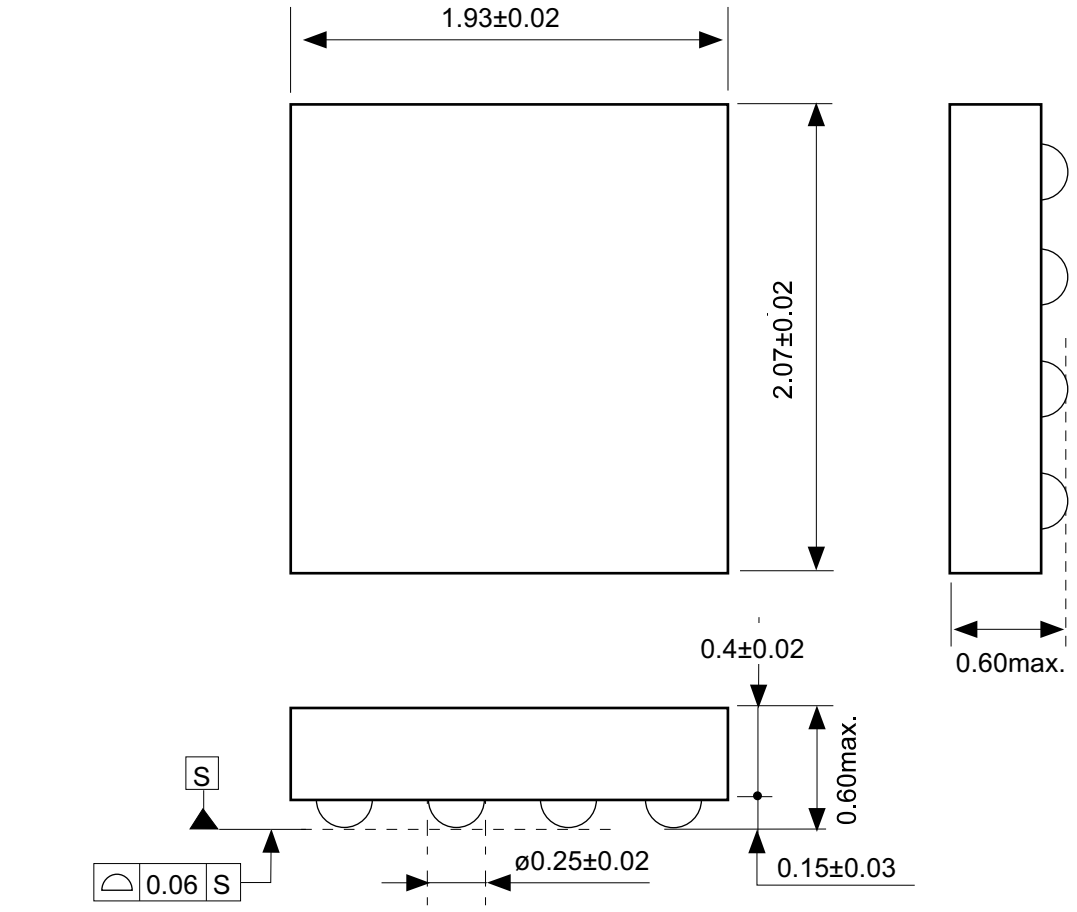


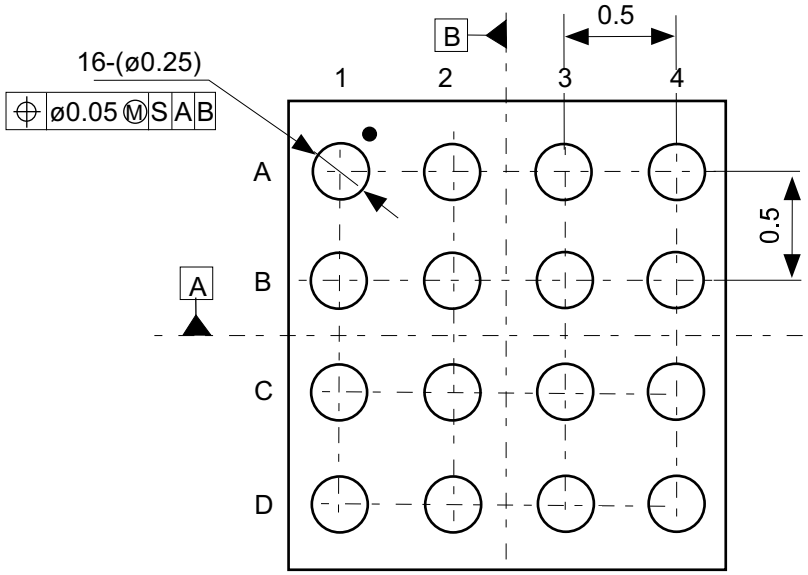
2. 5 SDA output delay time t_{AA} vs. Ambient temperature Ta



2. 6 SDA output delay time t_{AA} vs. Ambient temperature Ta





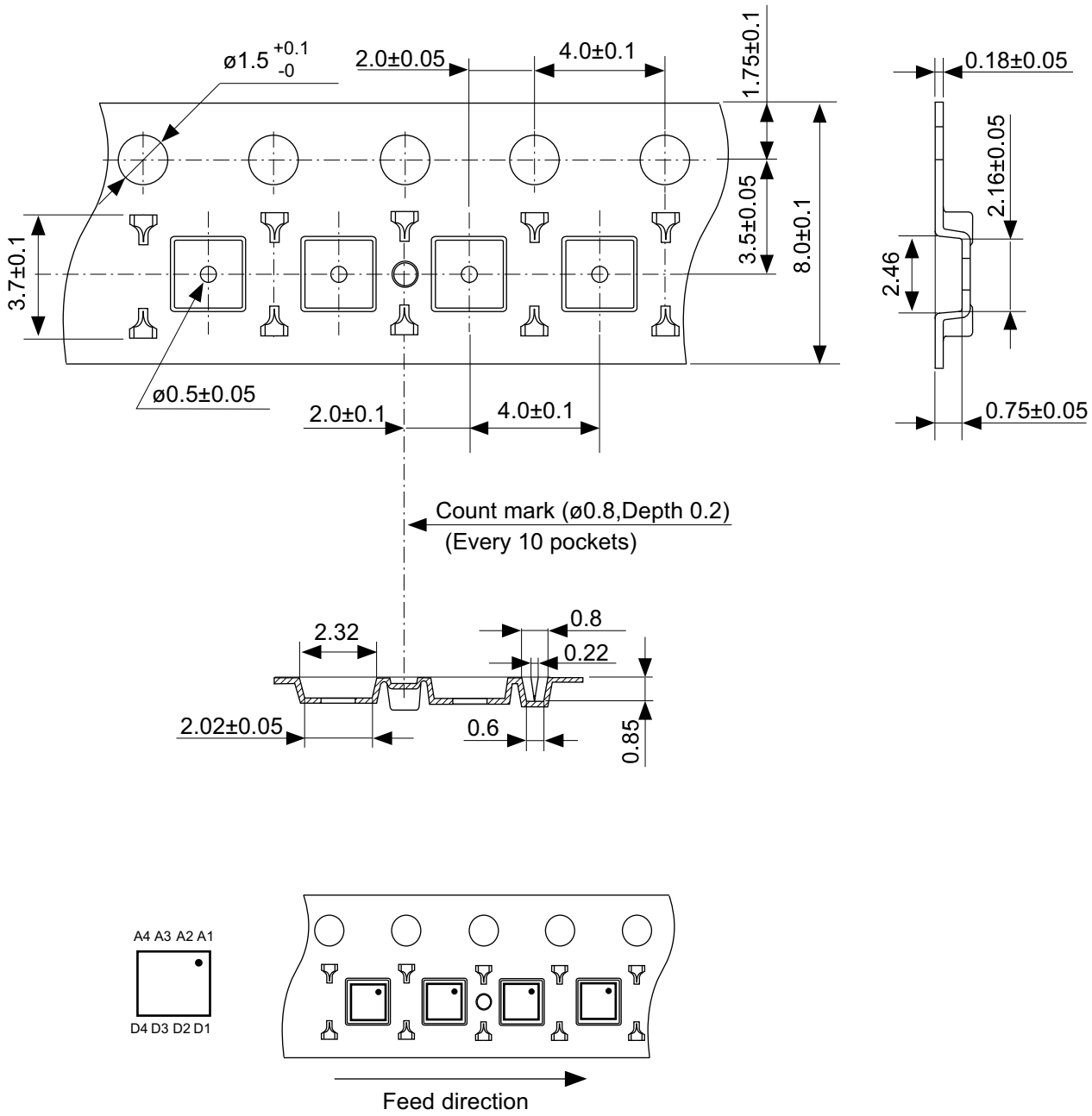


Pin No.	Pin name
A1	CLK or BPDX
A2	SCL
A3	WP
A4	VCCH
B1	DO7
B2	VSS
B3	SDA
B4	DO0
C1	DO6
C2	TIMEN or RESX
C3	DO3
C4	DO1
D1	DO5
D2	DO4
D3	VCCL
D4	DO2

No. HA016-C-P-SD-1.0

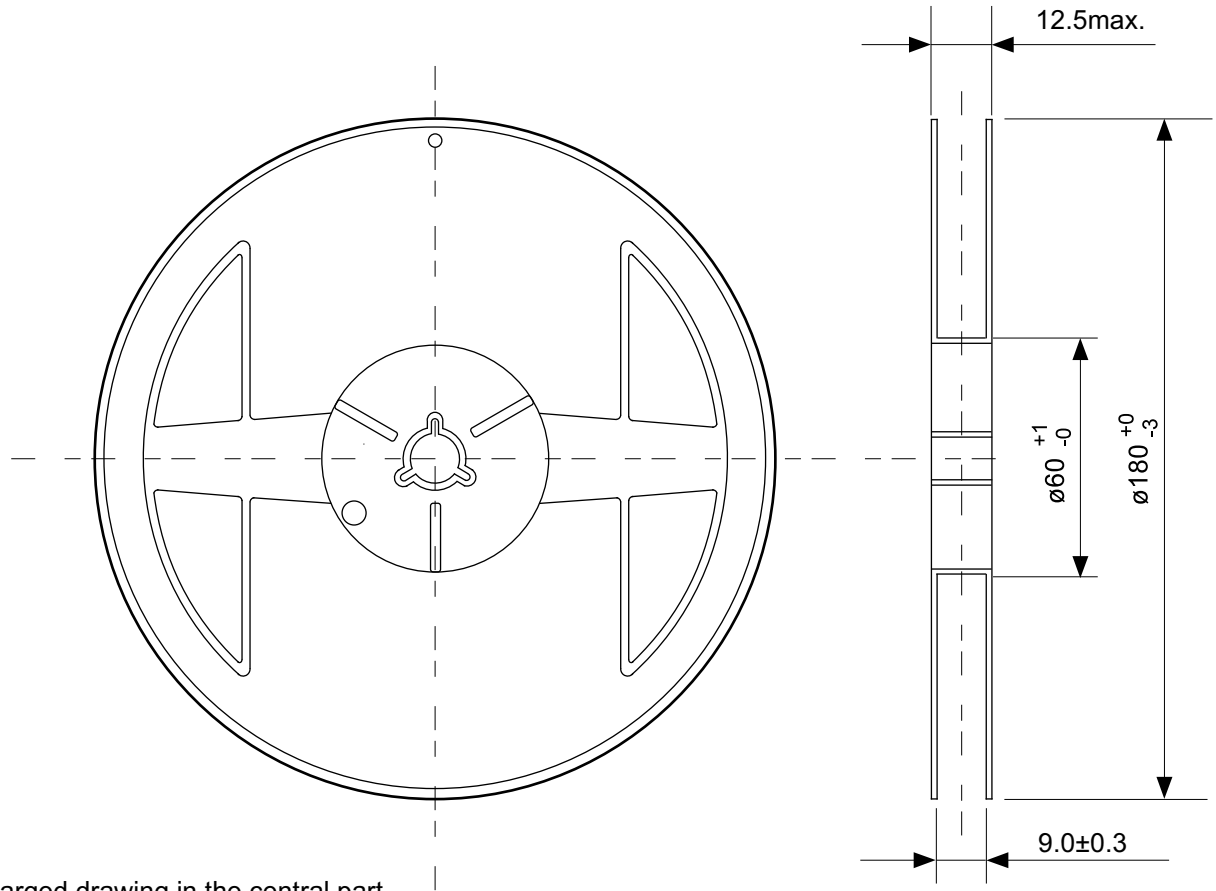
TITLE	WLP-16A-C-PKG Dimensions (S-7760A)
No.	HA016-C-P-SD-1.0
SCALE	
UNIT	mm

SII Semiconductor Corporation

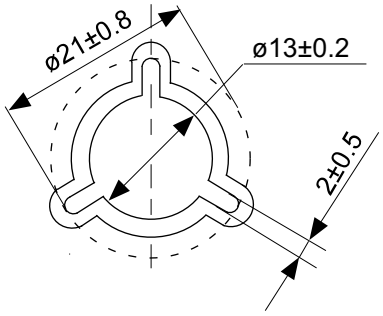


No. HA016-C-C-SD-1.1

TITLE	WLP-16A-C-Carrier Tape (S-7760A)
No.	HA016-C-C-SD-1.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	

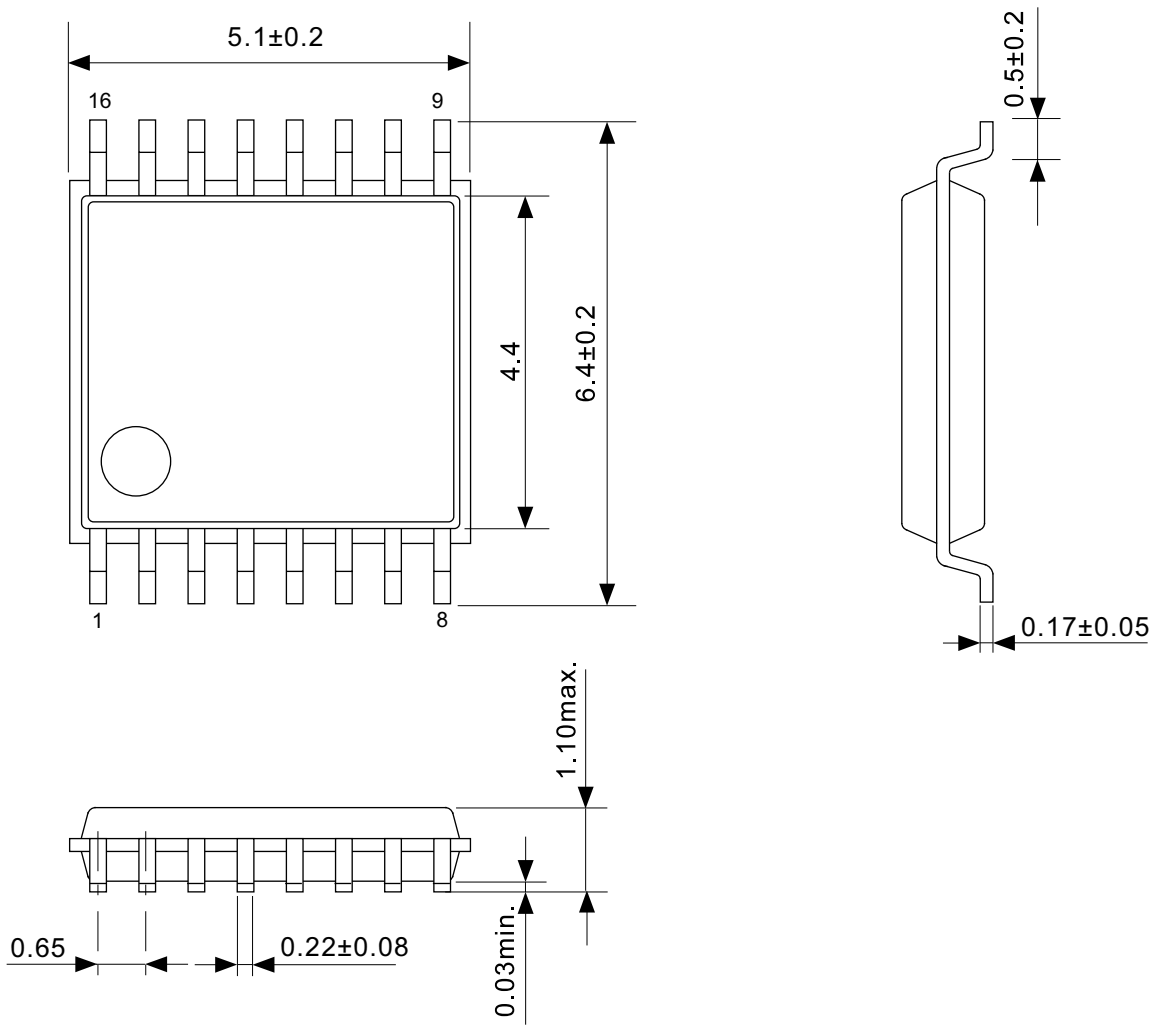


Enlarged drawing in the central part



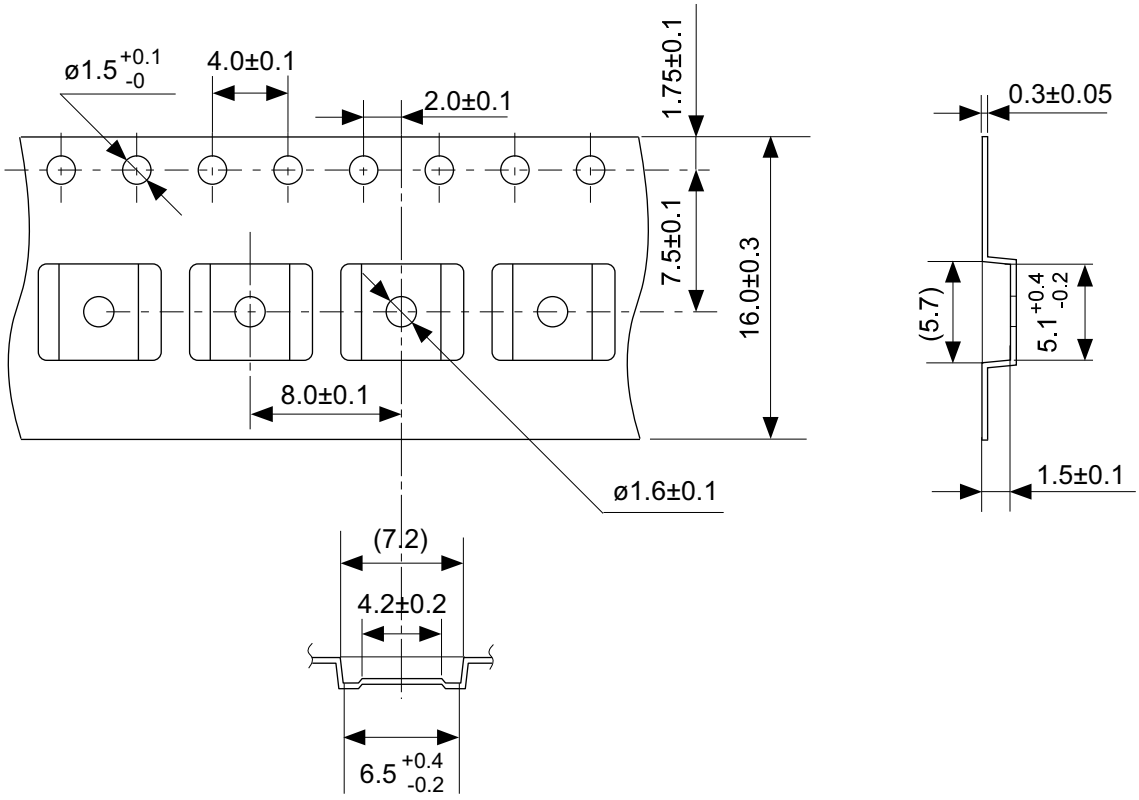
No. HA016-C-R-SD-1.0

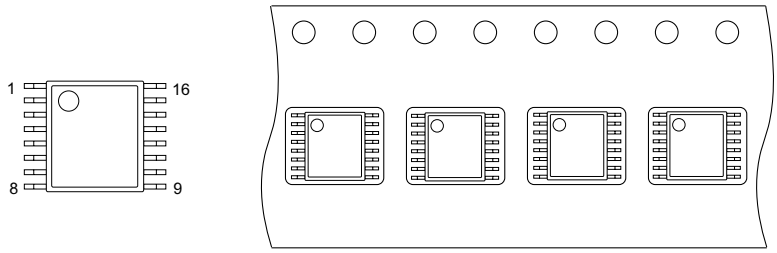
TITLE	WLP-16A-C-Reel (S-7760A)		
No.	HA016-C-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
SII Semiconductor Corporation			



No. FT016-A-P-SD-1.1

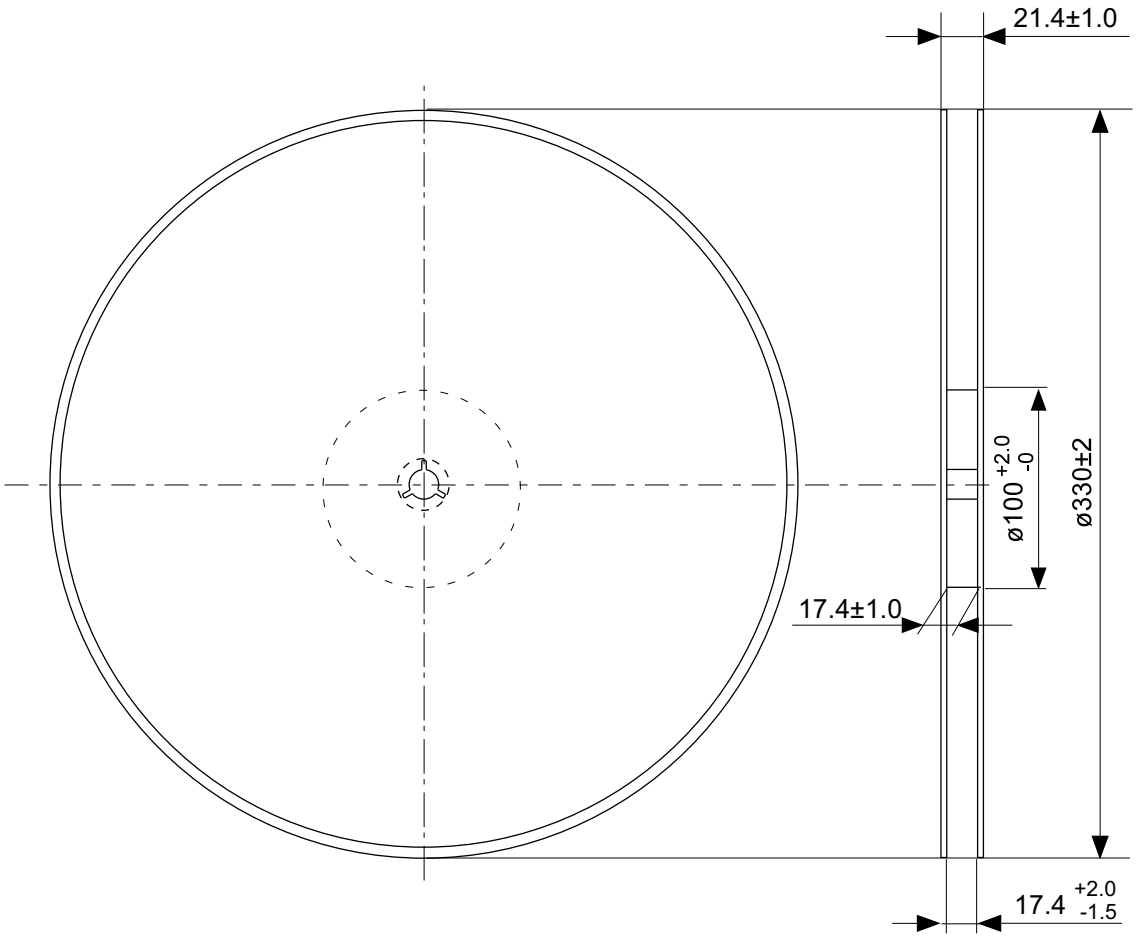
TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	



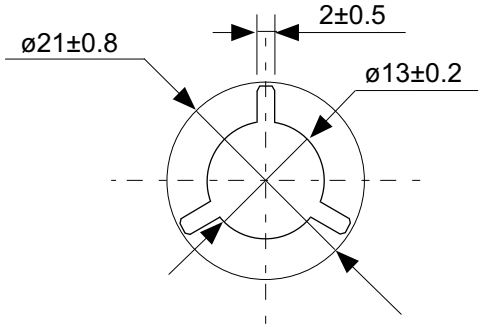


No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
SCALE	
UNIT	mm
SII Semiconductor Corporation	



Enlarged drawing in the central part



No. FT016-A-R-S1-1.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-S1-1.0		
SCALE		QTY.	4,000
UNIT	mm		
SII Semiconductor Corporation			

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