

## CMOS IC Application Note

# S-8209B Series Usage Guidelines Rev.1.5\_01

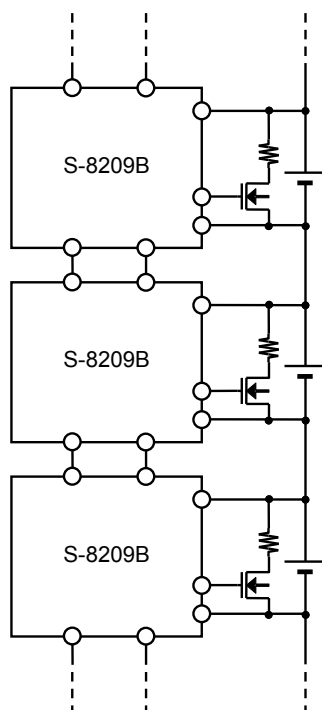
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The S-8209B Series is a battery protection IC with the cell-balance function. This application note is a guideline on the typical connection examples when using the S-8209B Series for applications. Refer to the datasheet for details and spec of this IC.

It is possible to configure the following applications with the S-8209B Series.

- A protection circuit with series multi-cell; 2 cells or more
- A battery protection circuit with cell-balance function

- Protection circuit with S-8209B Series for series multi-cells



## Contents

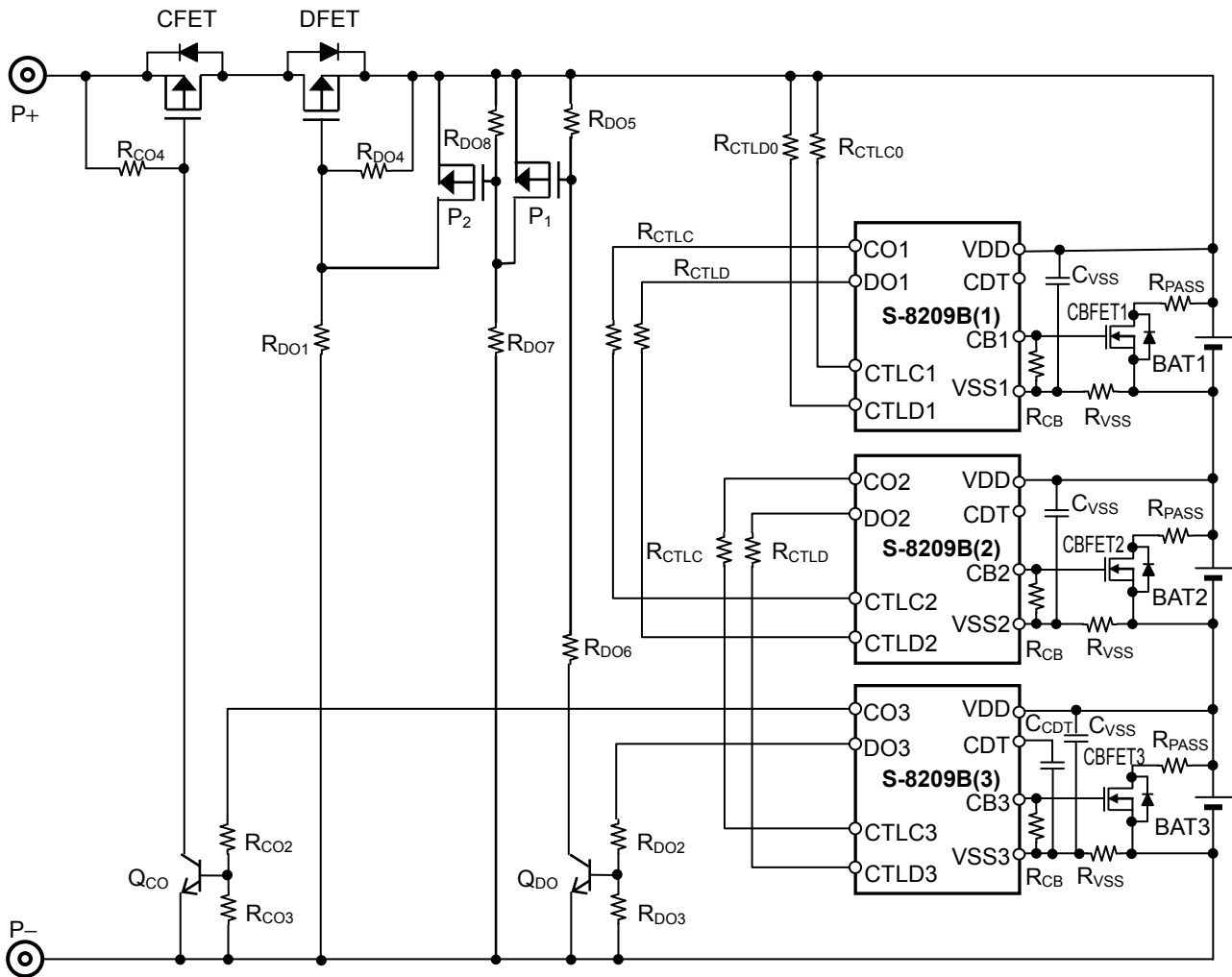
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### 1. Protection circuit with S-8209B Series (without discharge cell-balance function) for series multi-cells

In the connection of the S-8209B Series, connecting the CTLC, CTLD pins to the CO, DO pins allows to configure a protection circuit for series-connected batteries.

#### 1.1 Connection example of battery protection IC

Figure 1 shows the example of protection circuit with S-8209B for series multi-cells.



**Remark** Refer to “4. External components list” for constants of external components.

Figure 1

- Caution 1.** The above constants may be changed without notice.
- 2.** The example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

## 1.2 Operation

Following is about the operation of protection circuit with S-8209B for series multi-cell shown in **Figure 1**.

### 1.2.1 Normal status

Following is about the operation of S-8209B Series in the normal status.

The S-8209B goes in the normal status;

In the S-8209B (1), The CTLC1, CTLD1 pins are pulled up to the level of VDD1 pin, BAT1 is more than the overdischarge detection voltage ( $V_{DL}$ ) and less than the overcharge detection voltage ( $V_{CU}$ ). The CO1, DO1 pins get the level of VDD1 pin.

In the S-8209B (2), The CTLC2, CTLD2 pins are pulled up to the level of VDD1 pin by the CO1, DO1 pins, BAT2 is more than  $V_{DL}$  and less than  $V_{CU}$ . The CO2, DO2 pins get the level of VDD2 pin.

In the S-8209B (3), The CTLC3, CTLD3 pins are pulled up to the level of VDD2 pin by the CO2, DO2 pins, BAT3 is more than  $V_{DL}$  and less than  $V_{CU}$ . The CO3, DO3 pins get the level of VDD3 pin.

The status of each pin in the normal status is shown in **Table 1**.

**Table 1**

CTLC pin	CTLD pin	Status of battery	CO pin	DO pin
CTLC1 = VDD1	CTLD1 = VDD1	$V_{DL} < BAT1 < V_{CU}$	CO1 = VDD1	DO1 = VDD1
CTLC2 = VDD1	CTLD2 = VDD1	$V_{DL} < BAT2 < V_{CU}$	CO2 = VDD2	DO2 = VDD2
CTLC3 = VDD2	CTLD3 = VDD2	$V_{DL} < BAT3 < V_{CU}$	CO3 = VDD3	DO3 = VDD3

The S-8209B (3) in the normal status turns on the charge control FET (CFET) and the discharge control FET (DFET) via transistors ( $Q_{CO}$ ,  $Q_{DO}$ ,  $P_1$ ,  $P_2$ ) externally set to each CO3 and DO3 pin.

Therefore it is possible to charge/discharge by a charger or a load connected between  $P_+$  and  $P_-$ .

**1. 2. 2 Status to inhibit charge**

Following is about the status to inhibit charge, for example, the S-8209B (1) detects overcharge, the S-8209B (2) and (3) are in the normal status.

The S-8209B (1) goes in the overcharge status when BAT1 gets  $V_{CU}$  or more by charging. The CO1 pin is set in high impedance.

The CTLC2 pin of the S-8209B (2) is pulled down to the level of VSS2 pin by the CTLC pin sink current ( $I_{CTLC}$ ). The CTLC2 pin gets the level of VSS2 pin by the high impedance CO1 pin. Thus the S-8209B (2) goes in the overcharge status after the level of CTLC2 pin gets the CTLC pin L voltage ( $V_{CTLC}$ ) or less. The CO2 pin is set in high impedance.

The CTLC3 pin of the S-8209B (3) is pulled down to the level of VSS3 pin by  $I_{CTLC}$  as well. The CTLC3 pin gets the level of VSS3 pin by the high impedance CO2 pin. The S-8209B (3) also goes in the overcharge status after the level of CTLC3 pin gets  $V_{CTLC}$  or less.

The status of each pin in this case is shown in **Table 2**.

**Table 2**

CTLC pin	CTLD pin	Status of battery	CO pin	DO pin
CTLC1 = VDD1	CTLD1 = VDD1	$V_{CU} \leq BAT1$	CO1 = High-Z	DO1 = VDD1
CTLC2 = VSS2	CTLD2 = VDD1	$V_{DL} < BAT2 < V_{CU}$	CO2 = High-Z	DO2 = VDD2
CTLC3 = VSS3	CTLD3 = VDD2	$V_{DL} < BAT3 < V_{CU}$	CO3 = High-Z	DO3 = VDD3

The S-8209B (3) in the overcharge status turns off the CFET via a bipolar transistor ( $Q_{CO}$ ) set externally to the CO3 pin. In this case, charging via a charger connected between P+ and P- is inhibited.

By this operation the overcharge status is transmitted from the top (S-8209B (1)) to the bottom (S-8209B (3)), from the CO pin to the CTLC pin.

Charging is also inhibited; BAT2 or BAT3 gets  $V_{CU}$  or more.

**S-8209B Series Usage Guidelines****1. 2. 3 Status to inhibit discharge**

Following is the status to inhibit discharge, for example, the S-8209B (1) detects overdischarge, the S-8209B (2) and (3) are in the normal status.

The S-8209B (1) goes in the overdischarge status when BAT1 gets  $V_{DL}$  or less by discharging. The DO1 pin is set in high impedance.

The CTLD2 pin of the S-8209B (2) is pulled down to the level of VSS2 pin by the CTLD pin sink current ( $I_{CTLDL}$ ). The CTLD2 pin gets the level of VSS2 pin by the high impedance DO1 pin. Thus the S-8209B (2) goes in the overdischarge status after the level of CTLD2 pin gets the CTLD pin L voltage ( $V_{CTLDL}$ ) or less. The DO2 pin is set in high impedance.

The CTLD3 pin of the S-8209B (3) is pulled down to the level of VSS3 pin by  $I_{CTLDL}$  as well. The CTLD3 pin gets the level of VSS3 pin by the high impedance DO2 pin. The S-8209B (3) also goes in the overdischarge status after the level of CTLD3 pin gets  $V_{CTLDL}$  or less.

The status of each pin in this case is shown in **Table 3**.

**Table 3**

CTLC pin	CTLD pin	Status of battery	CO pin	DO pin
CTLC1 = VDD1	CTLD1 = VDD1	$BAT1 \leq V_{DL}$	CO1 = VDD1	DO1 = High-Z
CTLC2 = VDD1	CTLD2 = VSS2	$V_{DL} < BAT2 < V_{CU}$	CO2 = VDD2	DO2 = High-Z
CTLC3 = VDD2	CTLD3 = VSS3	$V_{DL} < BAT3 < V_{CU}$	CO3 = VDD3	DO3 = High-Z

The S-8209B (3) in the overdischarge status turns off the DFET via transistors ( $Q_{DO}$ ,  $P_1$ ,  $P_2$ ) externally set to the DO3 pin. In this case, discharging to a load connected between  $P_+$  and  $P_-$  is inhibited.

By this operation the overdischarge status is transmitted from the top (S-8209B (1)) to the bottom (S-8209B (3)), from the DO pin to the CTLD pin.

Charging is also inhibited; BAT2 or BAT3 gets  $V_{DL}$  or less.

#### 1. 2. 4 Charge cell-balance function

In **Figure 1**, The S-8209B (1) sets the CB1 pin at the level of VDD1 pin when BAT1 gets the cell-balance detection voltage ( $V_{BU}$ ) or more by charging. By this operation, the cell-balance control FET (CBFET1) is turned on so that the cell-balance control FET bypasses the charge current which flows into BAT1.

At this point, if BAT2, BAT3 are less than  $V_{BU}$ , the speed to charge BAT1 gets slower than to charge BAT2, BAT3. This is the charge cell-balance function. Even if any of battery voltages reaches  $V_{BU}$ , the cell-balance control FET which corresponds to each battery turns on and the cell-balance is adjusted.

The S-8209B Series turns off the cell-balance control FET when the battery voltage decreases to the cell-balance release voltage ( $V_{BL}$ ) or less by discharging again.

**Caution** If a battery having the voltage  $V_{BL}$  or more is included among batteries when composing a protection circuit shown in **Figure 1**, the cell-balance control FET may turn on immediately after connecting the batteries.

#### 1. 2. 5 Delay circuit

Connecting a delay capacitor only to the CDT3 pin of the S-8209B (3), as seen in **Figure 1**, allows to gain the detection delay time ( $t_{DET}$ ) and the release delay time ( $t_{REL}$ ). In detecting by any of batteries, each delay time is the same length.

##### (1) Detection delay time ( $t_{DET}$ )

BAT1 gets  $V_{CU}$  or more by charging, the CTLC2 pin gets the level of VSS2 pin because a capacitor is not connected to the CDT1 pin so that the CO1 pin is set in high impedance after delay of several hundred  $\mu$ s.

After that in the S-8209B (2), the level of CTLC2 pin gets  $V_{CTLCL}$  or less, after delay of several hundred  $\mu$ s the CO2 pin is set in high impedance.

In the S-8209B (3), after delay of  $10.0 [M\Omega] (Typ.) \times 0.01 [\mu F] = 0.1 [s] (Typ.)$ , the CO3 pin is set in high impedance because  $C_{CDT}$  is connected to the CDT3 pin.

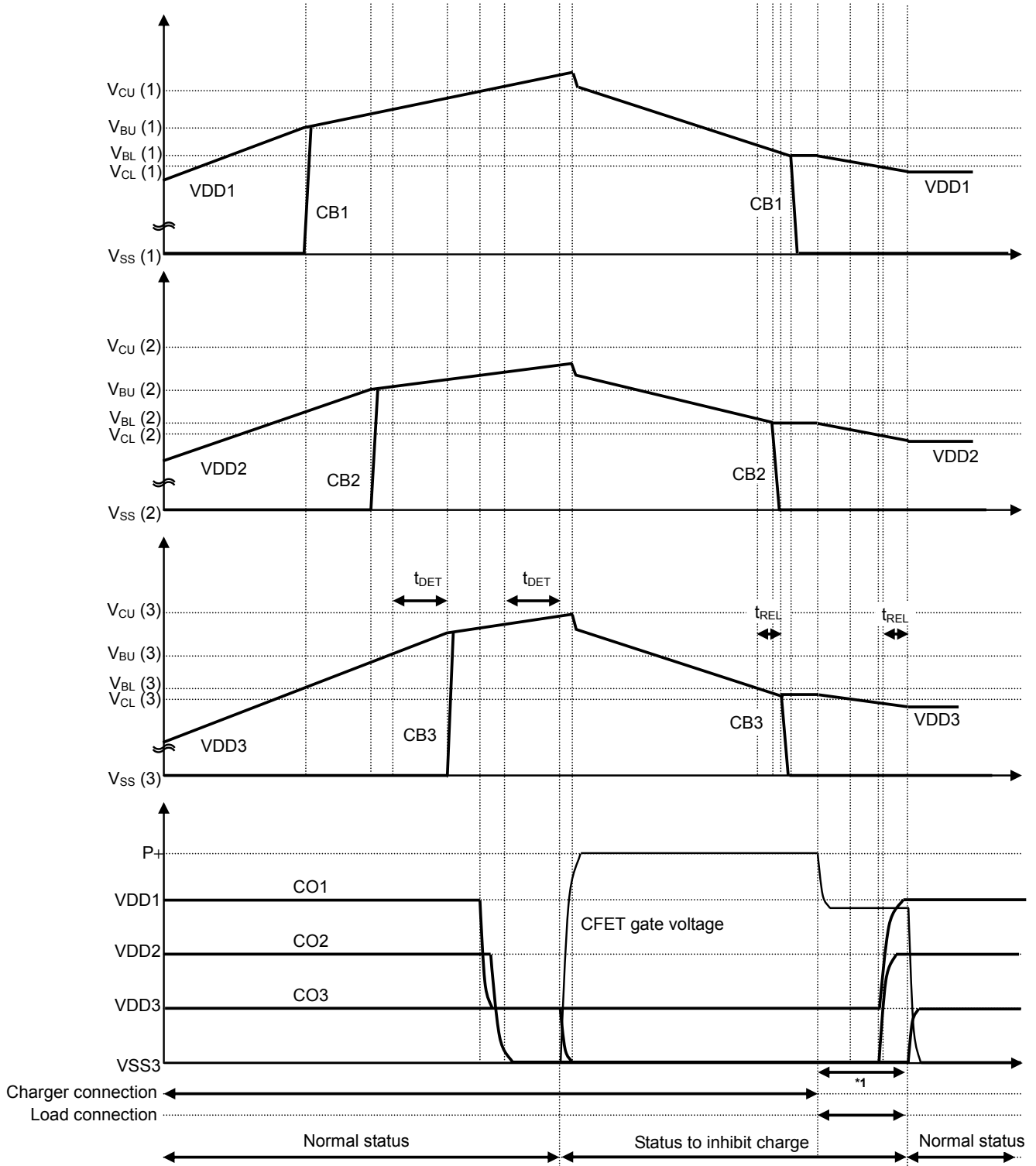
Even if any of batteries detects, by this operation, users are able to gain the detection delay time almost the same to delay time of the S-8209B (3), because it defines the whole delay time in the S-8209B Series.

##### (2) Release delay time ( $t_{REL}$ )

The S-8209B Series also has the release delay time ( $t_{REL}$ ), and this delay time is set its length as approx. 1/10 of the detection delay time. Connecting a delay capacitor only to the CDT3 pin of the S-8209B (3) allows having the same release delay time, as well as in the detection delay time.

1.3 Timing chart

1.3.1 Overcharge detection

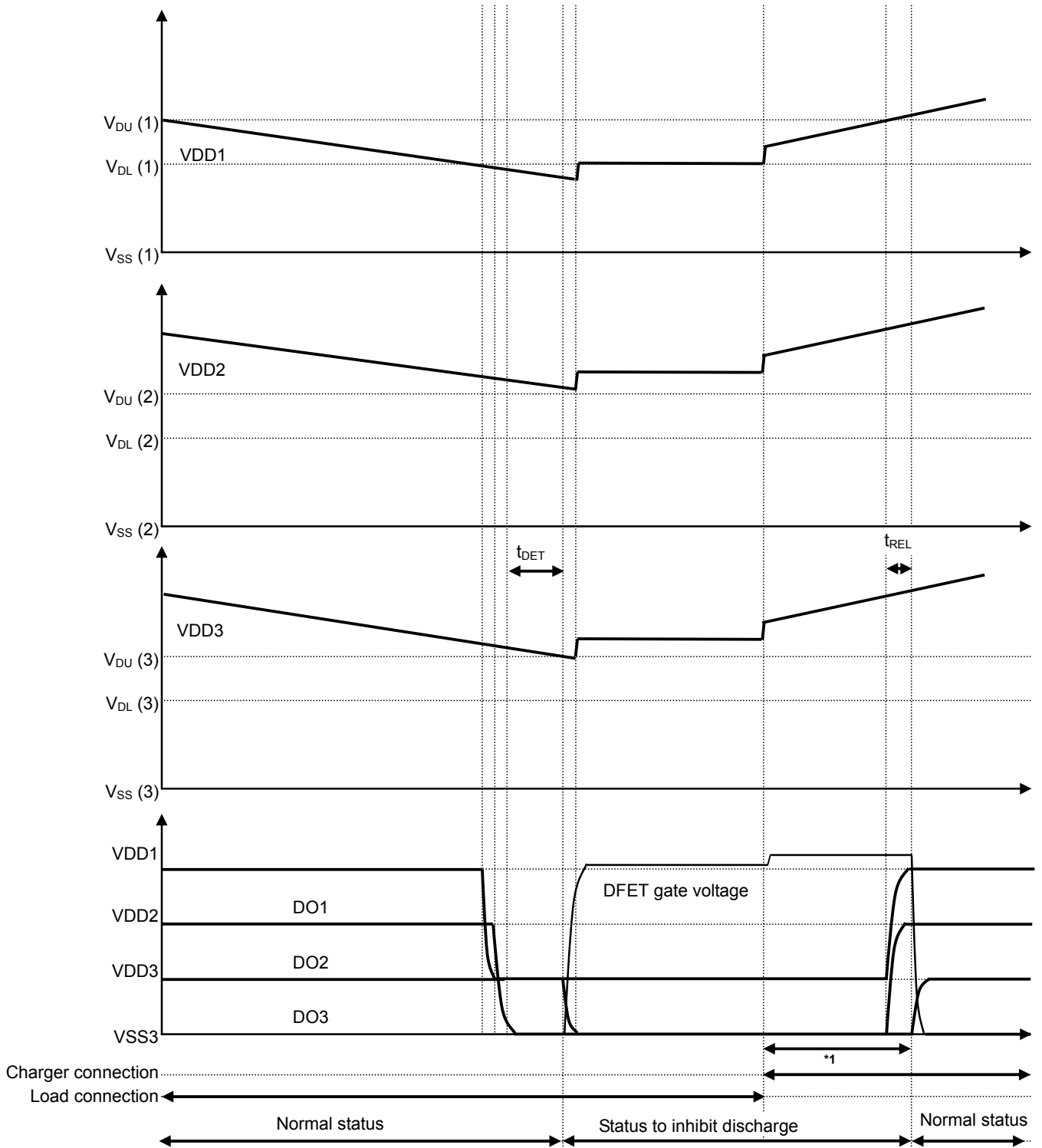


\*1. In this period, the discharge current flows via a parasitic diode in the CFET.

Figure 2



1.3.2 Overdischarge detection



\*1. In this period, the charge current flows via a parasitic diode in the DFET.

Figure 3

1.4 Demonstration data of charge cell-balance detection

The demonstration data shows cell-balance for 3-series lithium ion rechargeable battery using the S-8209BAA.

1.4.1 High ratio of bypass current to charge current

Charger: a constant current charger (0.05 C = 145 mA)

S-8209BAA charge cell-balance, 0.05 C constant current charger

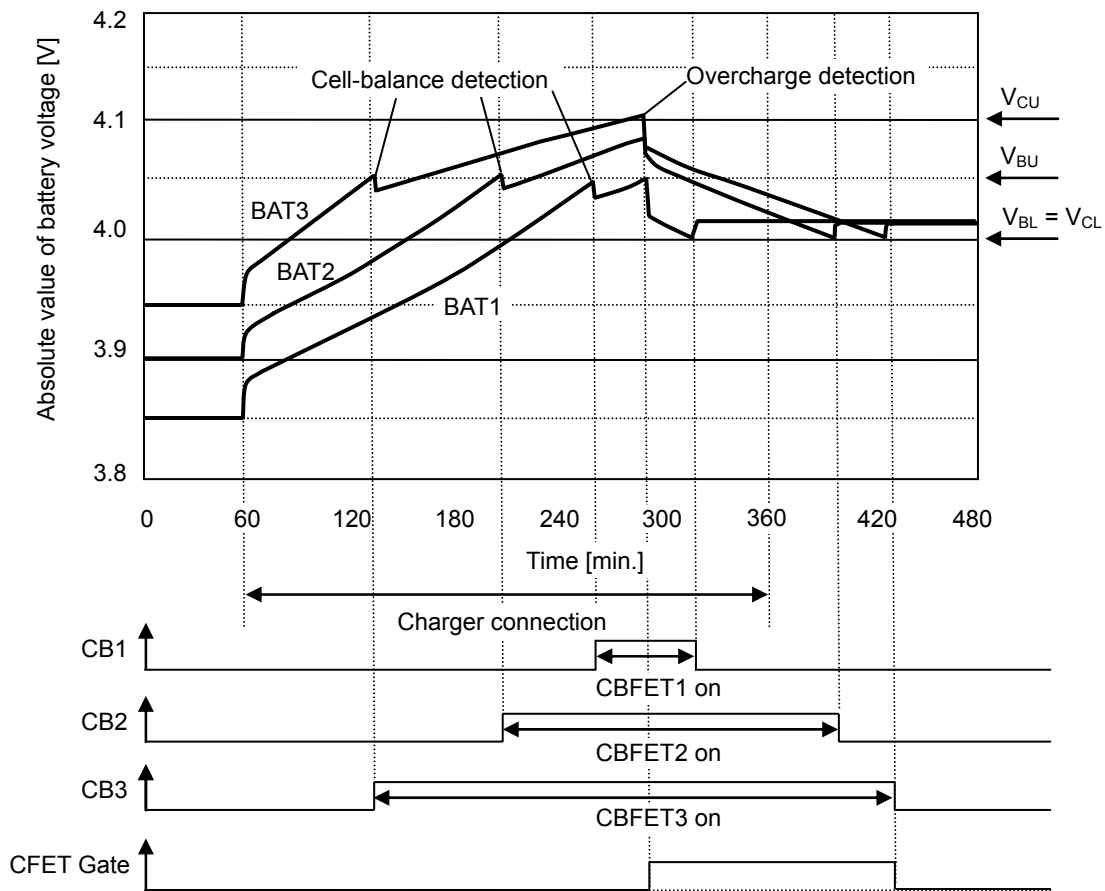


Figure 4

Test conditions

Test circuit: Figure 1

IC: S-8209BAA ( $V_{CU} = 4.100\text{ V}$ ,  $V_{CL} = 4.000\text{ V}$ ,  $V_{BU} = 4.050\text{ V}$ ,  $V_{BL} = 4.000\text{ V}$ ,  $V_{DL} = 2.500\text{ V}$ ,  $V_{DU} = 2.700\text{ V}$ )

Battery: 3-series cell lithium ion rechargeable battery, Nominal capacitance: 2.9 Ah, Size: 18650

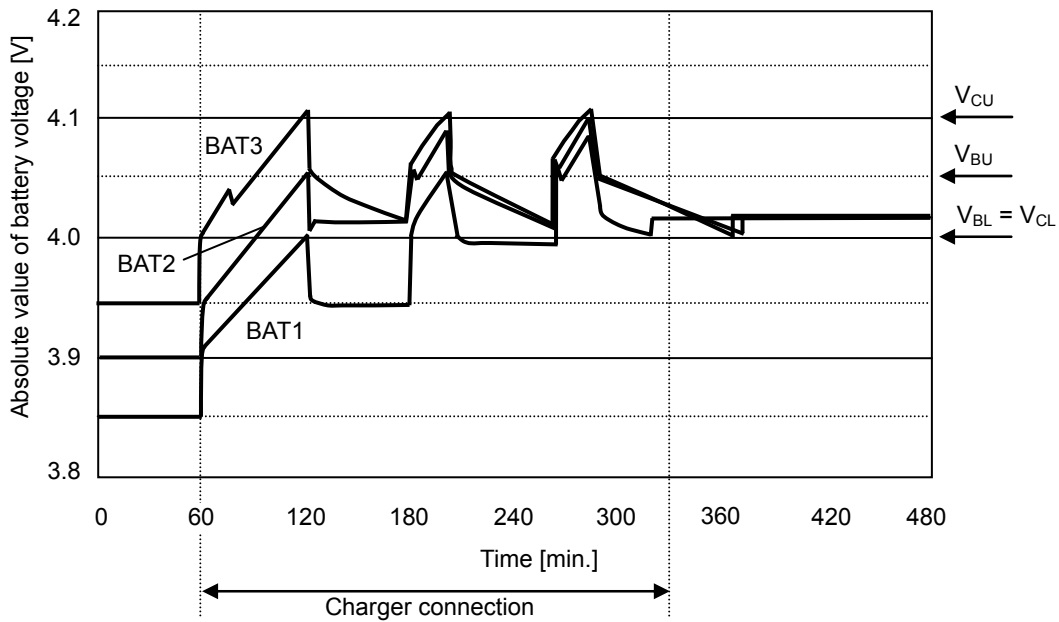
$R_{PASS} = 51\ \Omega$  (1 W)  $\rightarrow$  Bypass current =  $4.1\text{ V} / 51\ \Omega = 80\text{ mA}$

**1. 4. 2 Low ratio of bypass current to charge current**

When the ratio of bypass current to charge current is low, repeating cell-balance cycle enables to adjust cell-balance.

Charger: a constant current charger (0.1 C = 290 mA)

S-8209BAA charge cell-balance, 0.1 C constant current charger



**Figure 5**

**Test conditions**

Test circuit: **Figure 1**

IC: S-8209BAA ( $V_{CU} = 4.100\text{ V}$ ,  $V_{CL} = 4.000\text{ V}$ ,  $V_{BU} = 4.050\text{ V}$ ,  $V_{BL} = 4.000\text{ V}$ ,  $V_{DL} = 2.500\text{ V}$ ,  $V_{DU} = 2.700\text{ V}$ )

Battery: 3-series cell lithium ion rechargeable battery, Nominal capacitance: 2.9 Ah, Size: 18650

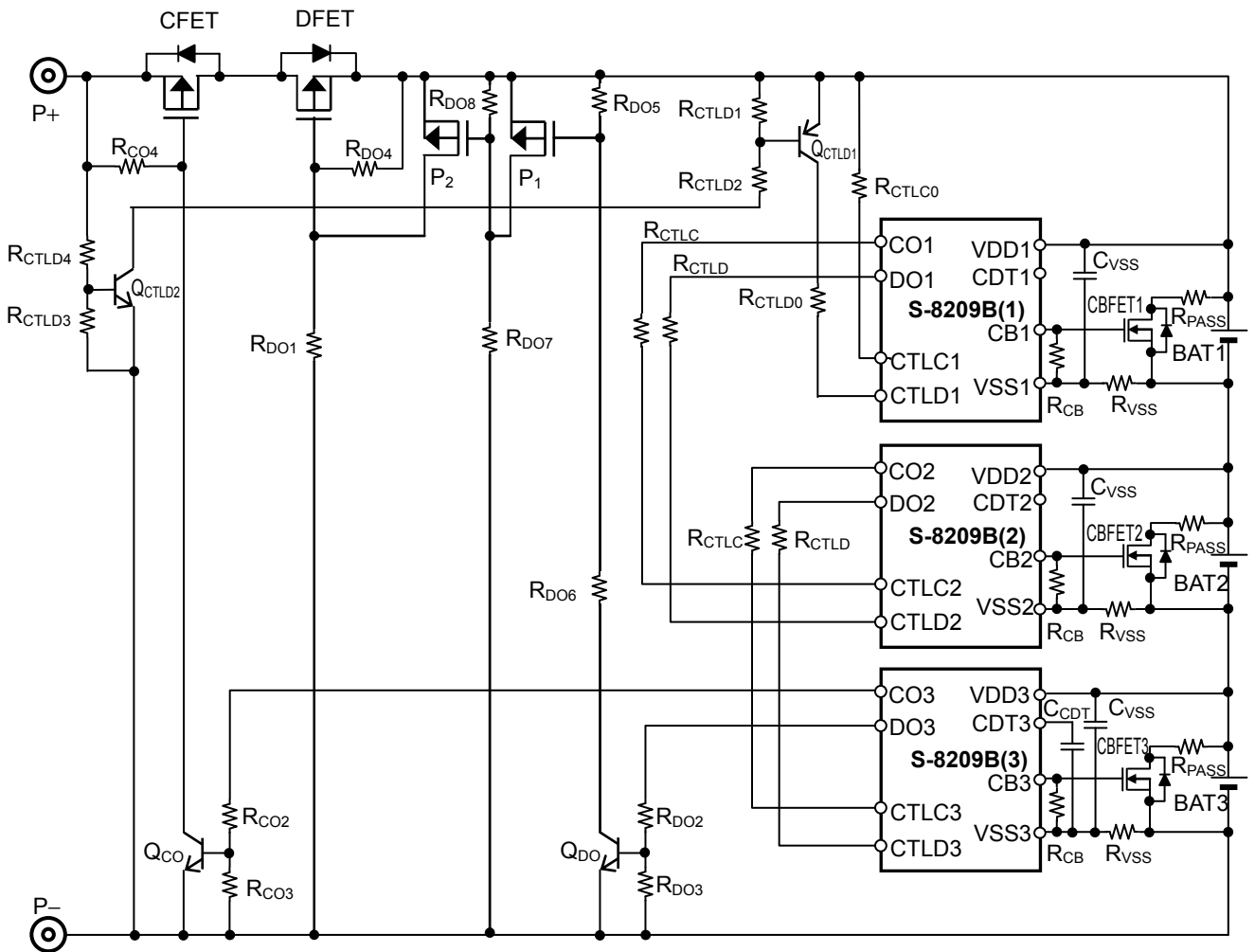
$R_{PASS} = 51\ \Omega$  (1 W)  $\rightarrow$  bypass current =  $4.1\text{ V} / 51\ \Omega = 80\text{ mA}$

**S-8209B Series Usage Guidelines**

**2. Protection circuit with S-8209B Series (with discharge cell-balance function) for series multi-cells**

**2.1 Connection example of battery protection IC**

Setting bipolar transistors ( $Q_{CTLD1}$ ,  $Q_{CTLD2}$ ) allows adding the function to transmit the overdischarge status from the bottom (S-8209B (3)) to the top (S-8209B (1)).



**Remark** Refer to “4. External components list” for constants of external components.

**Figure 6**

- Caution 1.** The above constants may be changed without notice.
- 2.** The example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

## 2.2 Operation

Following is about the operation of protection circuit with S-8209B for series multi-cell shown in **Figure 6**.

Setting bipolar transistors ( $Q_{CTLD1}$ ,  $Q_{CTLD2}$ ) to the circuit in **Figure 6** allows adding the function to transmit the overdischarge status from the bottom (S-8209B (3)) to the top (S-8209B (1)). By this, even if any IC among the S-8209B (1) to (3) first goes in the overdischarge status, it is possible to turn on all other cell-balance control FETs (CBFET) of the S-8209B Series. Thus cell-balance is certainly adjusted.

Following is about the operation in the status to inhibit discharge, when the S-8209B (2) detects overdischarge, and the S-8209B (1), (3) are in the normal status.

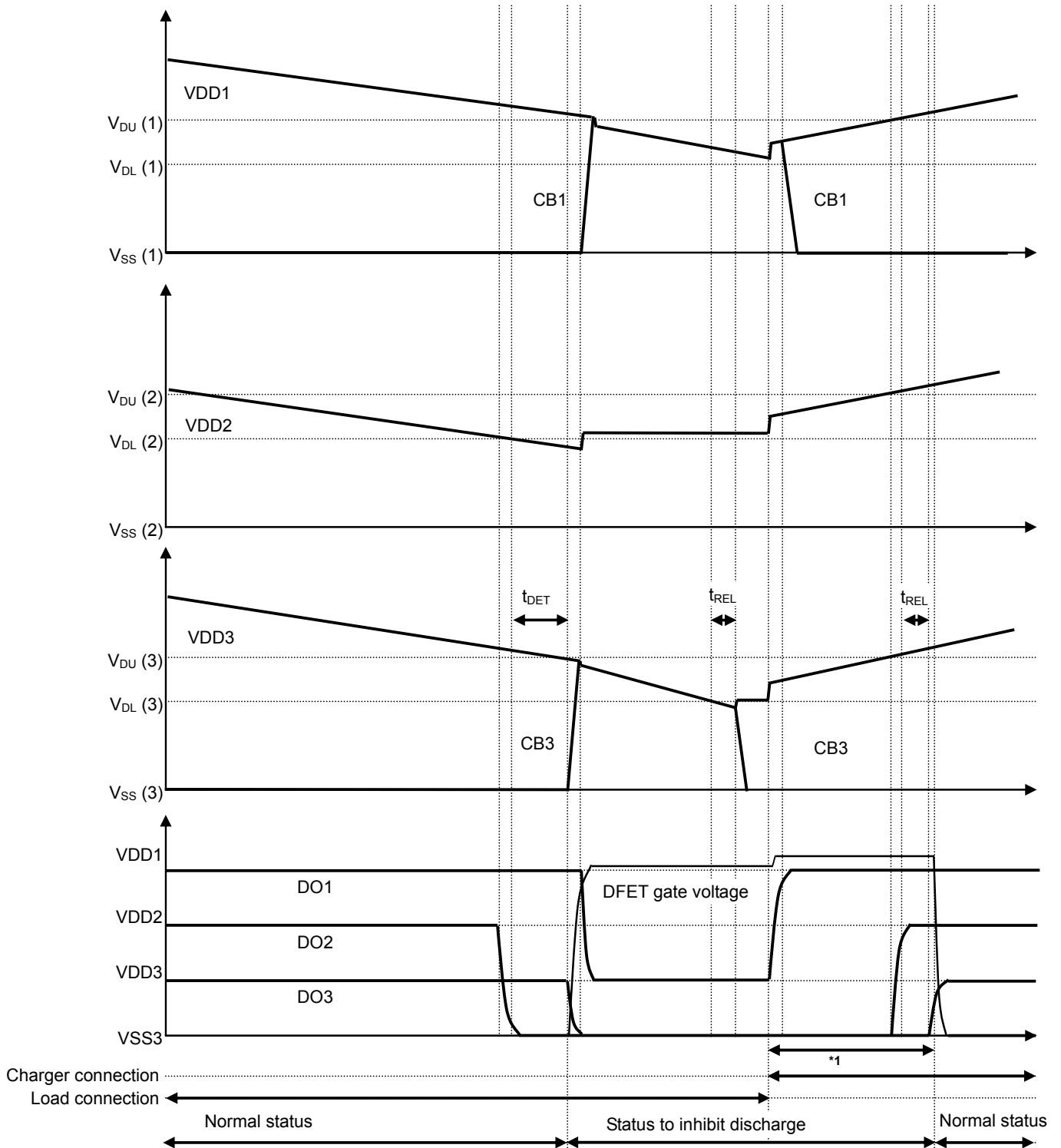
1. The S-8209B (2) goes in the overdischarge status when BAT2 decreases to  $V_{DL}$  or less by discharging. The DO2 pin is set in high impedance.
2. The S-8209B (3) also goes in the overdischarge status via the DO2 pin to the CTLD3 pin.
3. The S-8209B (3) turns on the cell-balance control FET (CBFET3) by the discharge cell-balance function.
4. The S-8209B (3) in the overdischarge status turns off DFET via a transistor ( $Q_{DO}$ ,  $P_1$ ,  $P_2$ ) and inhibits discharging to a load connected between  $P_+$  and  $P_-$ .
5. The  $P_+$  pin is pulled down by a load connected between  $P_+$  and  $P_-$ .
6.  $Q_{CTLD1}$ ,  $Q_{CTLD2}$  are turned off and the CTLD1 pin of the S-8209B (1) is set in high impedance.
7. The S-8209B (1) also goes in the overdischarge status. The cell-balance control FET (CBFET1) turns on by the discharge cell-balance function.

As mentioned above, even in case that the S-8209B (2) first detects overdischarge by voltage drop in BAT2, the overdischarge status is transmitted from the S-8209B (3) to S-8209B (1) via  $Q_{CTLD1}$ ,  $Q_{CTLD2}$ . As a result all (1) to (3) of the S-8209B go in the overdischarge status so that cell-balance is adjusted by the discharge cell-balance function, when each BAT is more than  $V_{DL}$ . The cell-balance FET which corresponds to each battery turns off by the voltages of BAT1 to 3 that decreased to  $V_{DL}$  or less.

And  $Q_{CTLD1}$ ,  $Q_{CTLD2}$  are turned on by connecting a charger between  $P_+$  and  $P_-$  after inhibit discharging, and the CTLD1 pin is pulled up to the level of VDD1 pin. In this case, the cell-balance control FET (CBFET1) turns off although the voltage of BAT1 does not reach  $V_{DL}$  or less.

**Caution** If a battery having the voltage  $V_{BL}$  or more, or a battery having the voltage overdischarge release voltage ( $V_{DU}$ ) or less is not included among batteries when composing a protection circuit shown in **Figure 6**, the cell-balance control FET may turn on immediately after connecting the battery. To turn off the cell-balance control FET, connect a charger between  $P_+$  and  $P_-$ .

2.3 Timing chart of overdischarge detection

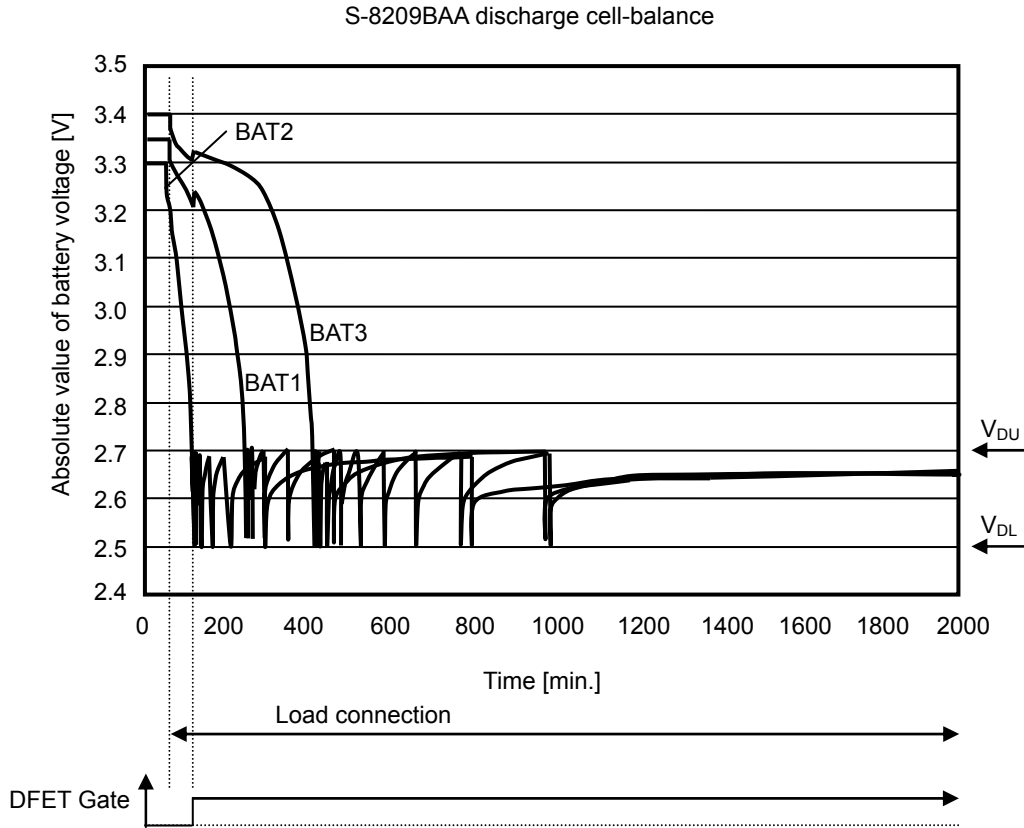


\*1. In this period, the charge current flows via a parasitic diode in the DFET.

Figure 7

**2.4 Demonstration data of overdischarge cell-balance detection**

The demonstration data shows cell-balance for 3-series lithium ion rechargeable battery using the S-8209BAA.



**Figure 8**

**Test conditions**

Test circuit: **Figure 6**

IC: S-8209BAA ( $V_{CU} = 4.100\text{ V}$ ,  $V_{CL} = 4.000\text{ V}$ ,  $V_{BU} = 4.050\text{ V}$ ,  $V_{BL} = 4.000\text{ V}$ ,  $V_{DL} = 2.500\text{ V}$ ,  $V_{DU} = 2.700\text{ V}$ )

Battery: 3-series cell lithium ion rechargeable battery, Nominal capacitance: 2.9 Ah, Size: 18650

$R_{PASS} = 51\ \Omega$  (1 W)  $\rightarrow$  bypass current =  $2.5\text{ V} / 51\ \Omega = 49\text{ mA}$

Load:  $100\ \Omega$

**Battery voltage's oscillation**

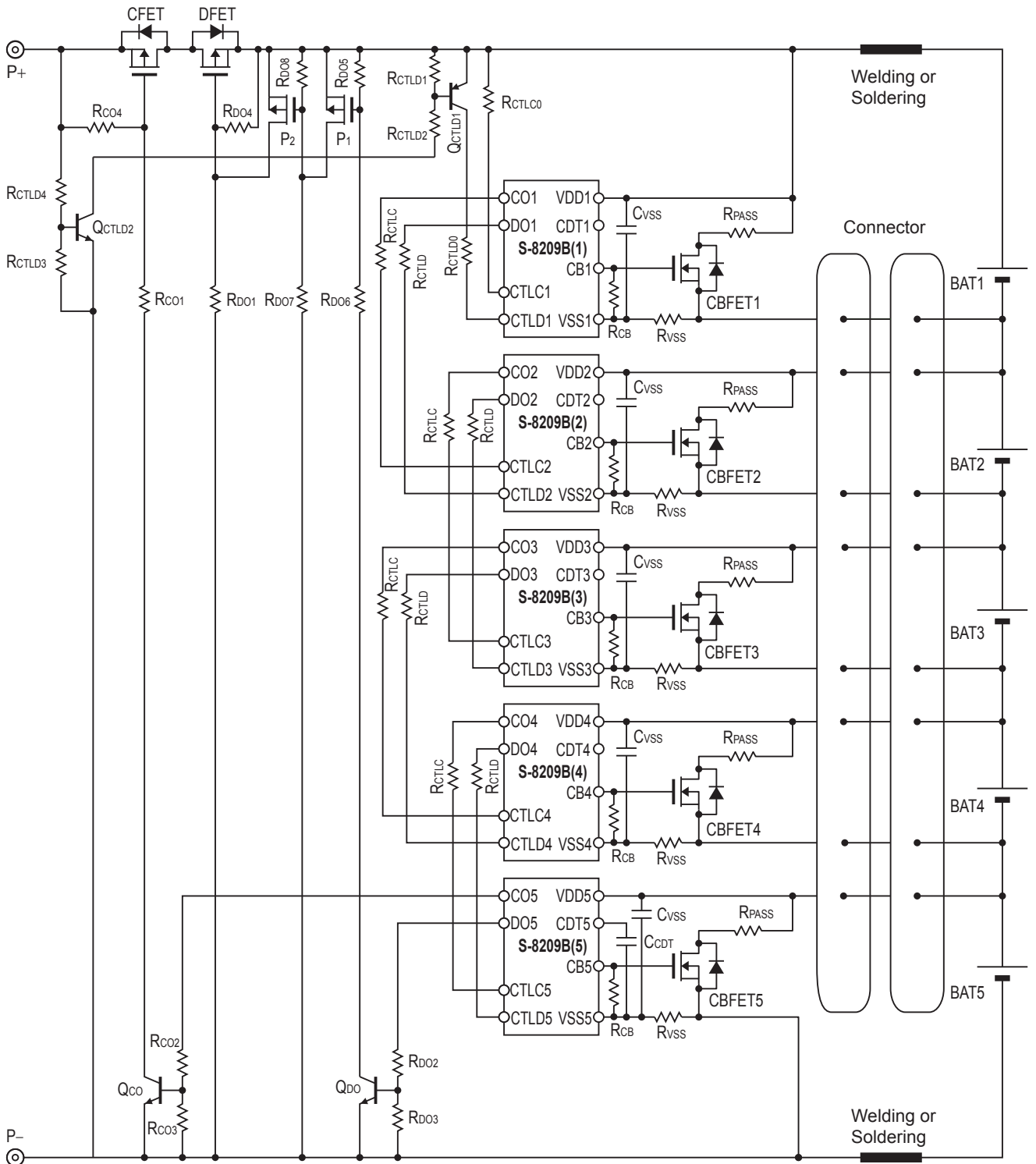
1. The cell-balance control FET turns off when the battery voltage decrease to the overdischarge detection voltage ( $V_{DL}$ ) or less.
2. Discharge via the cell-balance control FET stops so that the battery voltage rises.
3. The cell-balance control FET turns on when the battery voltage increases to the overdischarge release voltage ( $V_{DU}$ ) or more.
4. Discharge via the cell-balance control FET starts so that the battery voltage falls.

Repeating the procedures 1 to 4 enables to adjust cell-balance.

**S-8209B Series Usage Guidelines**

**3. Example of application circuit**

In the application that intermediate pins are connected by connectors as seen in the application circuit below, safety is enhanced since both charge and discharge stop even if the intermediate pins are disconnected.



**Remark** Refer to “4. External components list” for constants of external components.

**Figure 9**



#### 4. External components list

Table 4 shows external components in the connection examples in Figure 1, Figure 6 and Figure 9.

Table 4

Symbol	Typical	Unit	Components name	Maker	Remark
CBFET1 to CBFET5	—	—	—	—	User setting
CFET	—	—	—	—	User setting
DFET	—	—	—	—	User setting
C <sub>CDT</sub>	—	—	—	—	User setting
C <sub>VSS</sub>	0.1	μF	GRM188	Murata Manufacturing Co., Ltd.	Recommended
P <sub>1</sub>	—	—	2SJ210C	Renesas Electronics Corporation	Recommended
P <sub>2</sub>	—	—	2SJ210C	Renesas Electronics Corporation	Recommended
Q <sub>CTLD1</sub>	—	—	2SA1037AK	ROHM CO., LTD.	Recommended
Q <sub>CTLD2</sub>	—	—	2SC2412K	ROHM CO., LTD.	Recommended
Q <sub>CO</sub>	—	—	2SC2412K	ROHM CO., LTD.	Recommended
Q <sub>DO</sub>	—	—	2SC2412K	ROHM CO., LTD.	Recommended
R <sub>CB</sub>	10	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CO1</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CO2</sub>	510	kΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CO3</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CO4</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CTLC</sub> <sup>*1</sup>	1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CTLC0</sub>	1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CTLD</sub> <sup>*1</sup>	1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CTLD0</sub>	1	kΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CTLD1</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CTLD2</sub>	4.7	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CTLD3</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>CTLD4</sub>	4.7	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>DO1</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>DO2</sub>	510	kΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>DO3</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>DO4</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>DO5</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>DO6</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>DO7</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>DO8</sub>	1	MΩ	MCR03	ROHM CO., LTD.	Recommended
R <sub>PASS</sub> <sup>*2</sup>	—	—	—	—	User setting
R <sub>VSS</sub>	470	Ω	MCR03	ROHM CO., LTD.	Recommended

\*1. In order to prevent from damage when an overvoltage is applied to the IC, select R<sub>CTLC</sub> and R<sub>CTLD</sub> from 0 Ω to 100 kΩ.

\*2. Pay attention to the rated electric powers.

- Caution**
- The above constants may be changed without notice.
  - The example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.
  - Select external components considering its pressure when configuring a series protection cell with 5 cells or more.

**S-8209B Series Usage Guidelines**

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**5. Precaution**

- The usage described in this application note is typical example with our IC. Perform evaluation fully before use.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external components should be taken into consideration. SII Semiconductor Corporation shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

**6. Related source**

Refer to the following datasheet for details of the S-8209B Series.

**S-8209B Series Datasheet**

The information described herein is subject to change without notice.  
Contact our sales office for details.

Regarding the newest version, select product category and product name on our website, and download the PDF file.

**[www.sii-ic.com](http://www.sii-ic.com)**    **SII Semiconductor Corporation website**

## Disclaimers (Handling Precautions)

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4. Take care to use the products described herein within their specified ranges. Pay special attention to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.  
SII Semiconductor Corporation is not responsible for damages caused by failures and/or accidents, etc. that occur due to the use of products outside their specified ranges.
5. When using the products described herein, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
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7. The products described herein must not be used or provided (exported) for the purposes of the development of weapons of mass destruction or military use. SII Semiconductor Corporation is not responsible for any provision (export) to those whose purpose is to develop, manufacture, use or store nuclear, biological or chemical weapons, missiles, or other military use.
8. The products described herein are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not use those products without the prior written permission of SII Semiconductor Corporation. Especially, the products described herein cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.  
Prior consultation with our sales office is required when considering the above uses.  
SII Semiconductor Corporation is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.  
The user of these products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.  
The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products described herein are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products described herein do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Take care when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products described herein, comply with the laws and ordinances of the country or region where they are used.
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14. For more details on the information described herein, contact our sales office.

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