iC-MR 13-BIT S&H SIN/COS INTERPOLATOR WITH CONTROLLER INTERFACES

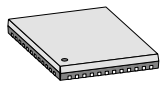
FEATURES

- Triggered 13-bit sine-to-digital conversion within 2 µs
- Precision PGA for differential and single-ended signals of up to 500 kHz
- Voltage or current input mode with signal monitoring
- Adjustable signal conditioning for offset, amplitude, and phase
- Input signal stabilization through LED or MR bridge current control of up to 50 mA
- 8-bit parallel and serial I/O interfaces (BiSS, SSI, and SPI)
- Absolute data interface (ADI: BiSS/SSI) for position preset
- Period counter of up to 50 bits with selectable singleturn/multiturn splitting
- Position data preset using ST/MT offset registers
- 12-bit A/D converter for temperature sensing
- Special functions for safety applications (signal monitoring, life counter, and extended CRC)
- Current-limited, differential 1 Vpp sine/cosine outputs to 100 Ω
- Device configurable through I/O interfaces or a serial EEPROM
- Single-sided 5 V operation from -40 to +110 °C

APPLICATIONS

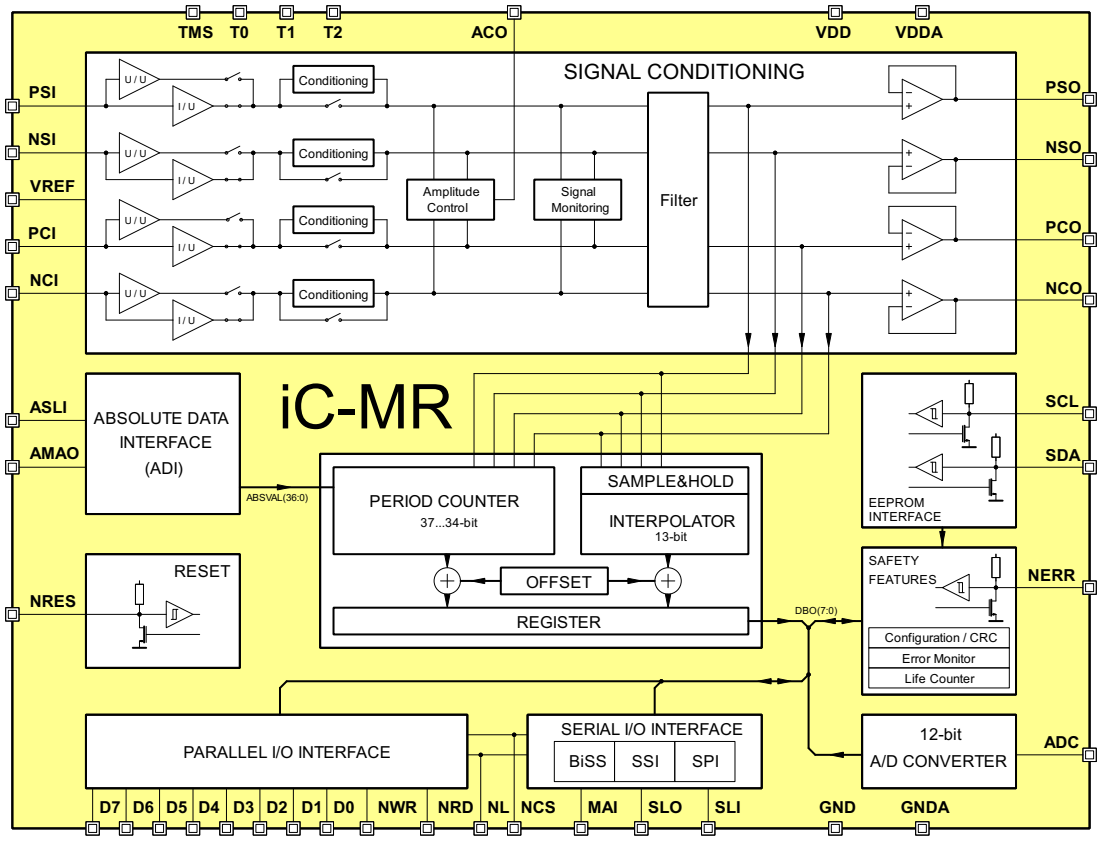
- Fast position decoding for safety-oriented encoder systems
- Motor feedback systems

PACKAGES



QFN48 7x7

BLOCK DIAGRAM



DESCRIPTION

Device iC-MR is a universal sine-to-digital converter with signal conditioning and various interfaces for configuration and data communication. Microcontrollers can be connected up through a parallel I/O interface with an 8-bit bus width (12.5 MHz) or using a serial I/O interface (4-pin SPI, 10 MHz). The serial I/O interface can function as a sensor interface either in BiSS C protocol (up to 10 MHz, bidirectional) or in SSI protocol (up to 4 MHz).

In the analog signal path iC-MR has precision input amplifiers with an adjustable gain for differential or referenced voltage signals of 10 mV peak to 1 V peak or for current signals of approx. 10 µA to 300 µA (input pins PSI, NSI, PCI, and NCI). A separate measurement input (VREF) enables signals to be referenced to the sensor's reference voltage.

The downstream signal conditioning unit can compensate for typical sine/cosine sensor signal errors, such as offset, amplitude, and phase errors. The conditioned signals are filtered and output through analog line drivers with an amplitude of typically 250 mV (output pins PSO, NSO, PCO, and NCO). A differential 1 Vpp signal to 100 Ω is available for line transmission.

A control signal is gained from the conditioned signals to stabilize the sine/cosine output signals. This can adjust the transmitting LED of optical encoder systems using the integrated 50 mA driver stage (output ACO). With magnetic sensors this driver output supplies the MR measuring bridges or can be used to feedback the bridge supply voltage. By tracking the sensor supply, sensor temperature and ageing effects are compensated for, the input signals are stabilized, and precise calibration of the input signals is maintained. This makes a constant interpolation accuracy possible across the entire operating temperature range.

At the same time the sensor is monitored for proper functioning. The amplitude and offset of the input signals at pins PSI, NSI, PCI, and NCI are checked, enabling wire-breakage or short circuits to be detected.

The control unit operating limits are also monitored so that an alarm can be signaled through the I/O interface and/or at error output NERR, depending on the configuration, with dirt or ageing of optical systems.

Sine-to-digital conversion is performed by a fast interpolator with a sample-&-hold circuit which resolves a sine period with 13 bits either continuously or on request. In parallel and independent of the interpolator a configurable 37-bit period counter logs the sine and cosine zero crossings. This period counter is programmable and can take its start value from the serial absolute data interface (ADI); the corresponding interface master operates either in BiSS C or SSI protocol.

For position measurement applications iC-MR differentiates between multiturn and singleturn data using a selectable intersection on the period counter. The position can be corrected accordingly using the multiturn and singleturn offset values.

An integrated 12-bit A/D converter digitizes linear measurement voltages at pin ADC for the evaluation of KTY temperature sensors, for example. Measurement of the calibratable converter is observed by settable threshold values so that a permissible operating temperature range with a lower and upper temperature threshold can be monitored.

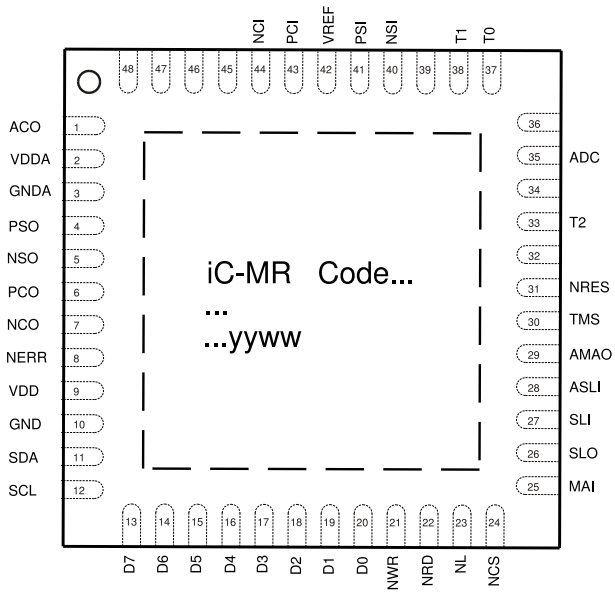
After power-on iC-MR collects its CRC protected configuration data from an external I^2C-EEPROM or waits for the configuration from one of the I/O interfaces. An undervoltage reset zeroes internal registers and is shown as a reset pulse at pin NRES, which also serves as a reset input (low active).

Errors can always be masked and allocated to an error bit (and displayed at error message output NERR) or a warning bit. The internal status registers are available to the I/O interfaces which have a number of different commands (software reset, memory verification, and error simulation).

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION QFN48-7x7
(topview)



PIN FUNCTIONS

No.	Name	Function
1	ACO	Amplitude Control, high-side current source output
2	VDDA	+5V Supply Voltage, analog
3	GNDA	Ground, analog
4	PSO	Sine Output
5	NSO	Sine Output, inverted
6	PCO	Cosine Output
7	NCO	Cosine Output, inverted
8	NERR	Error Signal, input/indication output*
9	VDD	+5V Supply Voltage, digital
10	GND	Ground, digital
11	SDA	EEPROM Interface, data line I^2C
12	SCL	EEPROM Interface, clock line I^2C

PIN FUNCTIONS

No.	Name	Function
13	D7	Par. Interface, data line
14	D6	Par. Interface, data line
15	D5	Par. Interface, data line
16	D4	Par. Interface, data line
17	D3	Par. Interface, data line
18	D2	Par. Interface, data line
19	D1	Par. Interface, data line
20	D0	Par. Interface, data line
21	NWR	Par. Interface, write signal*
22	NRD	Par. Interface, read signal*
23	NL	Par. Interface, storage signal* Ser. Interface, data acquisition*
24	NCS	Par. Interface, chip select* Ser. Interface, chip select*
25	MAI	Ser. Interface, clock input
26	SLO	Ser. Interface, data output
27	SLI	Ser. Interface, data input
28	ASLI	Absolute Data Interface, data input
29	AMAO	Absolute Data Interface, clock output
30	TMS	Test Mode Selection Input
31	NRES	Reset Signal, input/indication output*
32	n.c.	
33	T2	Test Pin
34	n.c.	
35	ADC	12-bit ADC Input, temperature sensor
36	n.c.	
37	T0	Test Pin
38	T1	Test Pin
39	n.c.	
40	NSI	Sine Input, inverted
41	PSI	Sine Input
42	VREF	Reference Voltage, input/output
43	PCI	Cosine Input
44	NCI	Cosine Input, inverted
45	n.c.	
46	n.c.	
47	n.c.	
48	n.c.	

n.c.: Pin is not connected.
*) Pin is low active.

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V(VDDA)	Voltage at VDDA		-0.3	6	V
G002	V(VDD)	Voltage at VDD		-0.3	6	V
G003	V()	Voltage at ACO, PSO, NSO, PCO, NCO, NERR, SDA, SCL, D(7...0), NWR, NRD, NL, NCS, MAI, SLO, SLI, ASLI, AMAO, TMS, NRES, ADC, PSI, NSI, VREF, PCI, NCI		-0.3	VDDA +0.3	V
G004	I(VDDA)	Current in VDDA		-100	400	mA
G005	I(VDD)	Current in VDD		-100	100	mA
G006	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ, all pins versus GNDA		2	kV
G007	Tj	Chip Temperature		-40	150	°C
G008	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Operating conditions:
VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package QFN48	-40		110	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN48 soldered to PCB according to JEDEC 51		30		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDDA, VDD	Permissible Supply Voltage		4.5	5	5.5	V
002	I(VDDA)	VDDA Supply Current			25	50	mA
003	I(VDD)	VDD Supply Current			5	50	mA
004	Vc()hi	Clamp Voltage hi at digital inputs ASLI, SLI, MAI, NCS, NL, NRD, NWR, NRES, NERR, SDA, SCL, TMS	Vc()hi = V() - V(VDD), I() = 4 mA	0.3		1.2	V
005	Vc()hi	Clamp Voltage hi at digital inputs D(7...0)	Vc()hi = V() - V(VDD), I() = 1.6 mA	0.3		1.2	V
006	Vcz()hi	Clamp Voltage hi at ACO, VDDA, PSO, NSO, PCO, NCO, AMAO, SLO, ADC, PSI, NSI, VREF, PCI, NCI	I() = 4 mA			11	V
007	Vc()lo	Clamp Voltage lo at ACO, VDDA, PSO, NSO, PCO, NCO, AMAO, SLO, ADC, PSI, NSI, VREF, PCI, NCI	I() = -4 mA	-1.2		-0.3	V
Bias Current Source, Reference Voltages, Input/Output VREF							
101	IBP	Bias Current Source	IBP calibrated to 200 µA	92.5	100	107.5	%
102	VPAH	Reference Voltage VPAH	referenced to GNDA	45	50	55	%VDDA
103	V05	Reference Voltage V05		450	500	550	mV
104	VREFI	Internal Ref. Voltage VREFI	DCPOS = 1 DCPOS = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
105	Vin()	Permissible Input Voltage at VREF	SELREF = 0x3	0.5		VDDA − 2	V
106	Rin()	Input Resistance at VREF	SELREF = 0x3, REFVOS = 0x3, UIN = 1, TUIN = 0, Rin() referenced to VREFin()	20	26	30	kΩ
107	Vref()out	Output Voltage at VREF	SELREF = 0x2, I() = 0		100		%VREFI
108	I0()	Leakage Current at VREF	SELREF = 0x0 or 0x1	-1		+1	µA
12-bit A/D Converter, Measuring Input ADC							
601	RESOadc	Converter Resolution			12		bit
602	tp()adc	Conversion Time			1.1		ms
603	Vin()FS	Maximum Full Scale Input Voltage	ADCSLOP = 0xFF ADCSLOP = 0x00		2.5 2.0		V V
604	INL()adc	Integral Nonlinearity				±10	LSB
Signal Conditioning, Inputs: PSI, NSI, PCI, NCI							
701	Vin()sig	Permissible V Mode Input Voltage	UIN = 1, TUIN = 0 UIN = 1, TUIN = 1, DCPOS = 1	0.75 -0.1		VDDA − 1.5 VDDA + 0.1	V V
702	Iin()	V Mode Input Current	UIN = 1, TUIN = 0	-100		100	nA
703	Rin()	V Mode Input Resistance	UIN = 1, TUIN = 1, vs. VREFin, Tj = 27 °C,	16.4	20	23.6	kΩ
704	Iin()sig	Permissible I Mode Input Current	UIN = 0, DCPOS = 0 UIN = 0, DCPOS = 1	-300 10		-10 300	µA µA
705	CTR()sig	Permissible Signal Contrast Ratio	current ratio of Iin()pkpk vs. Iin()dc	0.125		1	
706	Rin()	I Mode Input Resistance	Tj = 27 °C, vs. VREFin; UIN = 0, RIN = 00 UIN = 0, RIN = 01 UIN = 0, RIN = 10 UIN = 0, RIN = 11	 1.1 1.6 2.2 3.2	 1.6 2.3 3.2 4.6	 2.1 3.0 4.2 6.0	 kΩ kΩ kΩ kΩ
707	TC(Rin)	Temperature Coefficient of Rin			0.15		%/K
708	Vin()os	Offset Voltage of Input Stage	referenced to side of input; GR = 0x4, GFC = 0x1F, GFS = 0x7C0			300	µV

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
709	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(PSI) – V(NSI), respectively Vin()diff = V(PCI) – V(NCI); TUIN = 0 TUIN = 1	 20 80		 1000 4000	 mVpp mVpp
710	Vcore()	Recommended Internal Signal Level	G * Vin()diff, MODE = 0x01		6		Vpp
711	GF, GC	Selectable Gain Factors	TUIN = 0 TUIN = 1	2 0.5		100 25	
712	ΔGFdiff	Differential Gain Accuracy	referenced to fine gain range (GFS, GFC)	-1		1	LSB
713	ΔGFabs	Absolute Gain Accuracy	referenced to fine gain range (GFS, GFC), guaranteed range of monotony	-20		20	LSB
714	ΔGRabs	Gain Accuracy	referenced to coarse gain range (GR)	-8		8	%
715	VOScal1	Offset Calibration Range	measured at output, source V(ACO) = 3 V, REFVOS = 00, MODE =0x01; ORS, ORC = 00 ORS, ORC = 01 ORS, ORC = 10 ORS, ORC = 11		 ±450 ±900 ±2700 ±5400		 mV mV mV mV
716	VOScal2	Offset Calibration Range	measured at output, source V05, REFVOS = 01, MODE = 0x01; ORS, ORC = 00 ORS, ORC = 01 ORS, ORC = 10 ORS, ORC = 11		 ±1500 ±3000 ±9000 ±18000		 mV mV mV mV
717	VOScal3	Offset Calibration Range	measured at output, source V025, REFVOS = 10, MODE = 0x01; ORS, ORC = 00 ORS, ORC = 01 ORS, ORC = 10 ORS, ORC = 11		 ±750 ±1500 ±4500 ±9000		 mV mV mV mV
718	VOScal4	Offset Calibration Range	measured at output, source VDC = 125 mV, REFVOS = 11, MODE = 0x01; ORS, ORC = 00 ORS, ORC = 01 ORS, ORC = 10 ORS, ORC = 11		 ±375 ±750 ±2250 ±4500		 mV mV mV mV
719	ΔVOSdiff	Differential Linearity Error of Offset Correction		-0.5		0.5	LSB
720	ΔVOSint	Integral Linearity Error of Offset Correction		-100		100	LSB
721	PHIcal	Phase Correction Range	sine vs. cosine signal		±10.4		°
722	ΔPHIdiff	Differential Linearity Error of Phase Correction		-0.25		0.25	LSB
723	ΔPHIint	Integral Linearity Error of Phase Correction		-20		20	LSB
724	fin()max	Permissible Input Frequency	angle accuracy better 8 bit	500			kHz
725	fhc()	Input Amplifier Cut-off Frequency (-3 dB)		250			kHz

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Amplitude Control, Output ACO							
801	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(); ACOR = 00, I() = -5 mA ACOR = 01, I() = -10 mA ACOR = 10, I() = -25 mA ACOR = 11, I() = -50 mA			 1 1 1 1	 V V V V
802	Isc()hi	Short-Circuit Current hi in ACO	V() = 0 V ... VDD − 1 V; ACOR = 00 ACOR = 01 ACOR = 10 ACOR = 11	 -10 -20 -50 -100		 -5 -10 -25 -50	 mA mA mA mA
803	tr()	Rise Time Current Source ACO	I(ACO): 0 % → 90 % of setpoint		1		ms
804	tset()	Settling Time Current Source ACO	square control active, I(ACO): 50 % → 100 % of setpoint		400		µs
805	Vscq()	Regulated Mean Target Amplitude with Square Control	Vscq() = Vpp(V(PSO) - V(NSO)), respectively Vscq() = Vpp(V(PCO) - V(NCO)); ACOC = 0x19		 500		 mV
806	Vdc()	Regulated Mean Setpoint with Sum Control	ACOD = 0x00 ACOD = 0x7F		166 551		mV mV
807	It()min	Monitoring of ACO Output Current, lower threshold	referenced to current range ACOR		3		%Isc
808	It()max	Monitoring of ACO Output Current, upper threshold	referenced to current range ACOR		90		%Isc
809	Vt()min	Monitoring of Signal Level 1, lower threshold	referenced to Vscq()		40		%
810	Vt()max	Monitoring of Signal Level 2, upper threshold	referenced to Vscq()		135		%
Signal Filter							
901	fc()	Cut-off Frequency	ENF = 1, SELBP = 0; fin < 10 Hz fin > 100 kHz		15 2400		kHz kHz
902	PHI()	Phase Shift	ENF = 1, SELBP = 0, fin = 100 kHz for sine and cosine		1.5		°
Analog Outputs PSO, NSO, PCO and NCO							
A01	Vpk()max	Permissible Maximum Output Amplitude	VDDA = 4.5 V, DC level VDDA/2, RL = 50 Ω vs. VDDA/2			300	mV
A02	Vpk()	Output Amplitude with Sensor Tracking by Output ACO	ACOC = 0x19	225	250	275	mV
A03	fc	Cut-off Frequency	CL = 250 pF	500			kHz
A04	Vos	Output Offset Voltage			±200		µV
A05	Isc()hi	Short-Circuit Current hi	V() = 0 V	-40	-20	-15	mA
A06	Isc()lo	Short-Circuit Current lo	V() = VDD	15	20	40	mA
A07	SR()	Slew Rate	RLdiff = 100 Ω, CL = 25 pF		5		V/µs
A08	Rout()	Test Signal Source Resistance	MODE = 0x01 (Analog 1)		5		kΩ
A09	fout()cal	Permissible Test Signal Output Frequency	MODE = 0x01 (Analog 1), CL = 200 pF			2	kHz
Signal Monitoring							
B01	Vpp()max	AC Level Monitoring, upper threshold	referred to target amplitude of converter and analog output, see Fig. 13; ΔPHI = 0 (phase | 90°|), $(V(PSIN-NSIN))^2 + (V(PCOS-NCOS))^2$ > Vpp()max for at least 5 µs	110	130	150	%Vpp
B02	Vpp()min	AC Level Monitoring, lower threshold	referred to target amplitude of converter and analog output, see Fig. 13; ΔPHI = 0 (phase | 90°|), $(V(PSIN-NSIN))^2 + (V(PCOS-NCOS))^2$ < Vpp()min for at least 5 µs	10	35	60	%Vpp

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B03	Vpp()hys	AC Level Monitoring, Hysteresis	referred to Vpp()min, Vpp()max		30		mV
B04	Vdc()max	DC Level Monitoring, upper threshold	referred to target amplitude of converter and analog output, see Fig. 12	120	125	140	%VPAH
B05	Vdc()min	DC Level Monitoring, lower threshold	referred to target amplitude of converter and analog output, see Fig. 12	50	70	80	%VPAH
13-bit Interpolator							
C01	t_{IPO}	Conversion Time	ACQMODE = 00		2		µs
C02	AAabs	Absolute Conversion Accuracy	Vpk() = 250 mV		2		LSB
Reset Input / Reset Indication Output NRES							
K01	VDDon	VDD Turn-on Threshold	increasing voltage at VDD vs. GND	2.6		4.3	V
K02	VDDoff	VDD Turn-off Threshold (undervoltage reset)	decreasing voltage at VDD vs. GND	2.3		4.0	V
K03	VDDhys	VDD Hysteresis	VDDhys = VDDon - VDDoff	400			mV
K04	Vt()hi	Input Threshold Voltage hi				2	V
K05	Vt()lo	Input Threshold Voltage lo		0.8			V
K06	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi - Vt()lo	300	500		mV
K07	Ipu()	Pull-up Current		-750	-300	-60	µA
K08	Vs()lo	Output Saturation Voltage lo	I() = 4 mA			400	mV
K09	Isc()lo	Output Short-Circuit Current lo	V() = 0.4 V...VDD	4		80	mA
Oscillator							
M01	fosc	Internal Oscillator Frequency			15		MHz
EEPROM Interface SCL, SDA							
N01	Vs()lo	Saturation voltage lo	I() = 4 mA			400	mV
N02	Isc()	Short-Circuit Current lo		4		80	mA
N03	Vt()hi	Input Threshold Voltage hi				2	V
N04	Vt()lo	Input Threshold Voltage lo		0.8			V
N05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi - Vt()lo	100	250		mV
N06	Ipu()	Input Pull-up Current	V() = 0 V...VDD - 1 V	-750	-300	-60	µA
N07	Vpu()	Input Pull-up Voltage	Vpu() = VDD - V(), I() = -5 µA			0.4	V
N08	fclk()	Clock Frequency at SCL		100	120	130	kHz
N09	tbusy()cfg	Duration of Configuration Phase	IBP not adjusted; without EEPROM EEPROM access without I^2C read error EEPROM access with I^2C read error		0.5 4 12	1 5 15	ms ms ms
Serial I/O Interface MAI, SLO, SLI							
O01	Vt()hi	Threshold Voltage hi at SLI, MAI				2	V
O02	Vt()lo	Threshold Voltage lo at SLI, MAI		0.8			V
O03	Vt()Hys	Hysteresis at SLI, MAI	Vt()hys = Vt()hi - Vt()lo	300	500		mV
O04	Ipu()	Pull-up Current at MAI		-150	-60	-8	µA
O05	Ipd()	Pull-down Current at SLI		8	60	150	µA
O06	fclk()	Permissible Clock Frequency at MAI	SSI protocol BiSS C protocol SPI			4 10 10	MHz MHz MHz
O07	t_{P3}()	Output Propagation Delay at SLO	versus clock edge MAI; refers to timing Fig. 6	10		50	ns
O08	t_{out}()	Adaptive Slave Timeout at SLO	refers to timing Fig. 6 and 7	1/fosc		1.5*t_C + 3/fosc	
O09	Vs()hi	Saturation Voltage hi at SLO	Vs()hi = VDD - V(), I() = -4 mA			400	mV
O10	Vs()lo	Saturation Voltage lo at SLO	I() = 4 mA			400	mV
O11	Isc()hi	Short-circuit Current hi at SLO	V() = 0 V...VDD - 0.4 V	-80		-4	mA
O12	Isc()lo	Short-circuit Current lo at SLO	V() = 0.4 V...VDD	4		80	mA

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Parallel I/O Interface D(7...0), NWR, NRD, NL, NCS							
P01	Vt()hi	Threshold Voltage hi	D(7...0) as input			2	V
P02	Vt()lo	Threshold Voltage lo	D(7...0) as input	0.8			V
P03	Vt()hys	Input Hysteresis	D(7...0) as input, Vt()hys = Vt()hi - Vt()lo	300	500		mV
P04	Ipu()	Pull-up Current at D(7...0)		-70	-30	-5	µA
P05	Ipu()	Pull-up Current at NWR, NRD, NL, NCS		-150	-60	-8	µA
P06	Vs()hi	Saturation Voltage hi at D(7...0) Outputs	Vs()hi = VDD - V(), I() = -1.6 mA			400	mV
P07	Vs()lo	Saturation Voltage lo at D(7...0) Outputs	I() = 1.6 mA			400	mV
P08	Isc()hi	Short-circuit Current hi at D(7...0) Outputs	V() = 0 V...VDD - 0.4 V	-50		-1.6	mA
P09	Isc()lo	Short-circuit Current lo at D(7...0) Outputs	V() = 0.4 V...VDD	1.6		50	mA
P10	t_{P1}	Output Propagation Delay at D(7...0)	CL(D7...D0) = 10 pF, refers to timing Fig. 3; data stable after NRD hi → lo			50	ns
P11	t_{P2}	Output Hold Time at D(7...0)	CL(D7...D0) = 10 pF, refers to timing Fig. 4; data stable after NRD hi → lo			50	ns
Absolute Data Interface ASLI, AMAO							
Q01	Vt()hi	Threshold Voltage hi at ASLI				2	V
Q02	Vt()lo	Threshold Voltage lo at ASLI		0.8			V
Q03	Vt()hys	Hysteresis at ASLI	Vt()hys = Vt()hi - Vt()lo	300	500		mV
Q04	Ipu()	Pull-up Current at ASLI		-150	-60	-8	µA
Q05	Vs()hi	Saturation Voltage hi at AMAO	Vs()hi = VDD - V(), I() = -1.6 mA			400	mV
Q06	Vs()lo	Saturation Voltage lo at AMAO	I() = 1.6 mA			400	mV
Q07	Isc()hi	Short-circuit Current hi at AMAO	V() = 0 V...VDD - 0.4 V	-50		-1.6	mA
Q08	Isc()lo	Short-circuit Current lo at AMAO	V() = 0.4 V...VDD	1.6		50	mA
Q09	fclk()	Clock Frequency at AMAO	GET_ADI = 0, SSI_ADI = 1 (SSI protocol) GET_ADI = 0, SSI_ADI = 0 (BiSS C protocol)		1/16 1/2		fosc fosc
Error Signal Input/Output NERR							
R01	Vt()hi	Threshold Voltage hi				2	V
R02	Vt()lo	Threshold Voltage lo		0.8			V
R03	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi - Vt()lo	100	150		mV
R04	Ipu()	Pull-up Current		-750	-300	-60	µA
R05	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
R06	Isc()lo	Short-circuit Current lo	V() = 0.4 V...VDD	4		60	mA

OPERATING REQUIREMENTS: Absolute Data Interface (ADI)

Operating conditions: VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
BiSS Protocol (SSI_ADI = 0)						
I001	t_{frame}	Clock Frame Repetition	CYC_ADI = 1, refers to Elec. Char. M01	$8192/f_{osc}$		
I002	t_C	Clock Period	refers to Elec. Char. M01	$2/f_{osc}$		
I003	t_{L1}, t_{L2}	Clock Signal Hi/Lo Level Duration		50		% t_C
I004	t_{busy}	Permissible Processing Time	refers to clock period		253	t_C
I005	t_{P0}	Permissible Propagation Delay (Line Delay Compensation)	not featured (data is captured on next rising clock edge)	0	t_C - t_S	
I006	Δt_P	Permissible Propagation Delay Variance	not featured (refer to t_S and t_H)			% t_C
I007	t_S	Setup Time: Data stable before clock edge lo → hi	without line delay compensation (t_{P0} = 0)	50		ns
I008	t_H	Hold Time: Data stable after clock edge lo → hi	without line delay compensation (t_{P0} = 0)	10		ns
I009	t_{out}	Permissible Slave Timeout		t_C	40	µs
SSI Protocol (SSI_ADI = 1)						
I010	t_{frame}	Clock Frame Repetition	CYC_ADI = 1, refers to Elec. Char. M01	$8192/f_{osc}$		
I011	t_C	Clock Period	refers to Elec. Char. M01	$16/f_{osc}$		
I012	t_{L1}, t_{L2}	Clock Signal Hi/Lo Level Duration		50		% t_C
I013	t_S	Setup Time: Data stable before clock edge lo → hi		50		ns
I014	t_H	Hold Time: Data stable after clock edge lo → hi		10		ns
I015	t_{out}	Permissible Slave Timeout		t_C	40	µs

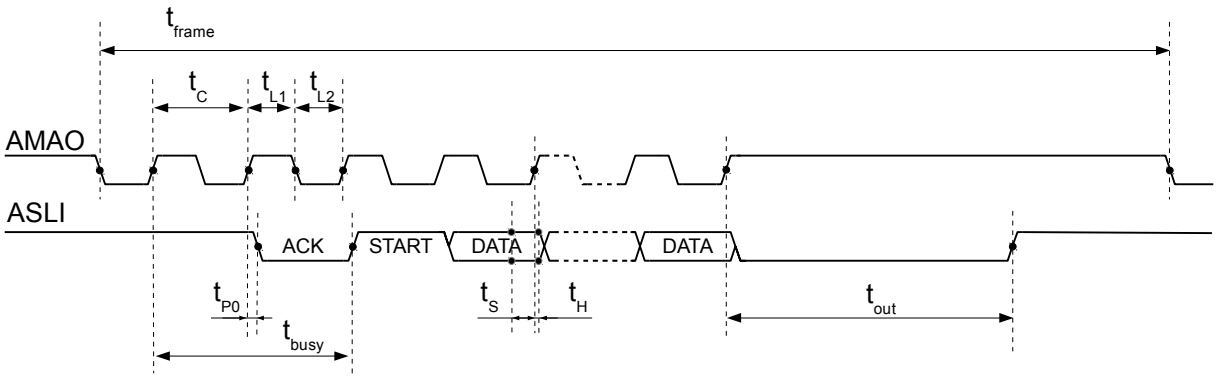


Figure 1: ADI timing with BiSS protocol

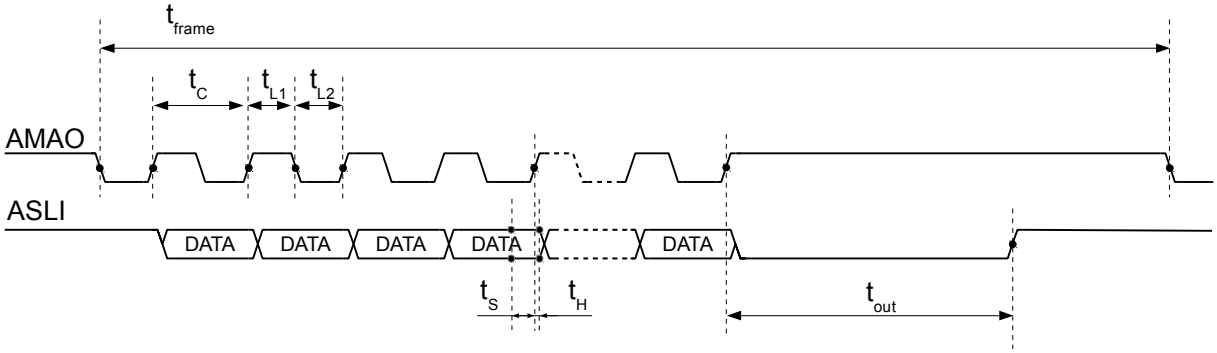


Figure 2: ADI timing with SSI protocol

OPERATING REQUIREMENTS: Parallel I/O Interface

Operating conditions: VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	t_{S1}	Setup Time: Address stable before NWR lo → hi		50		ns
I102	t_{H1}	Hold Time: Address stable after NWR lo → hi		50		ns
I103	t_{S2}	Setup Time: Data stable before NWR lo → hi		50		ns
I104	t_{H2}	Hold Time: Data stable after NWR lo → hi		50		ns
I105	t_{L1}	Write Signal Lo-Level Duration at NWR		80		ns
I106	t_{L2}	Write Signal Hi-Level Duration at NWR		80		ns
I107	t_{W1}	Wait Time between R/W Cycles: between NWR lo → hi to NRD hi → lo, and NRD lo → hi to NWR hi → lo		80		ns
I108	t_{L3}	Read Signal Lo-Level Duration at NRD		80		ns
I109	t_{L4}	Read Signal Hi-Level Duration at NRD		80		ns
I110	t_{P1}	Read Data Access Time: Data stable after NRD hi → lo		see Elec. Char. P11		
I111	t_{P2}	Read Data Hold Time: Bus outputs high impedance after NRD lo → hi		see Elec. Char. P10		
I112	t_{S3}	Setup Time: NCS hi → lo before NWR or NRD hi → lo		80		ns
I113	t_{H3}	Hold Time: NCS stable after NWR or NRD lo → hi		80		ns
I114	t_{S4}	Setup Time: NL hi → lo before NRD hi → lo		80		ns
I115	t_{H4}	Hold Time: NL stable after NRD lo → hi		80		ns

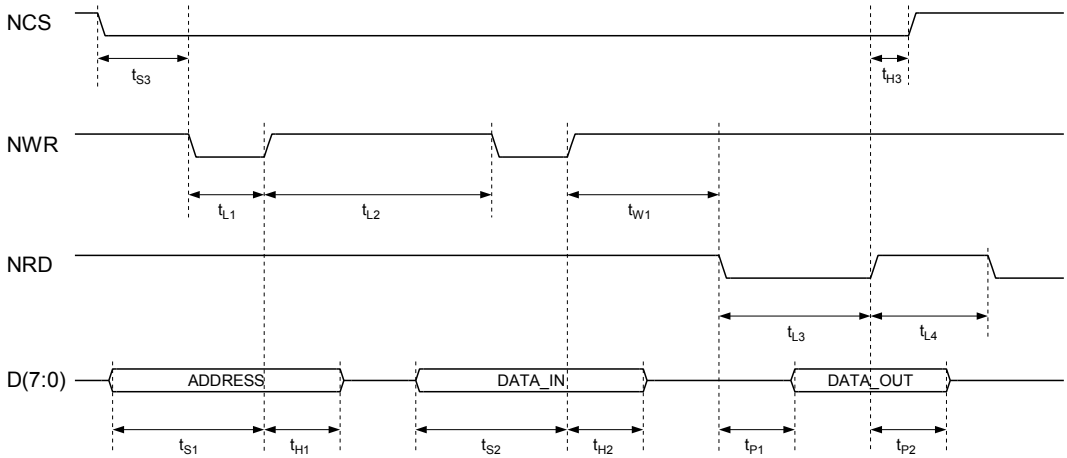


Figure 3: Parallel I/O interface timing

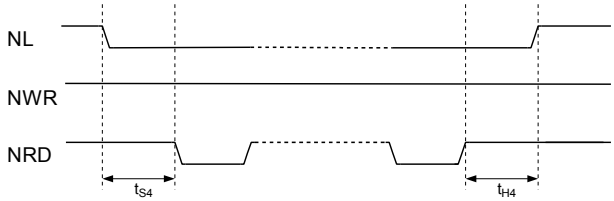


Figure 4: Parallel I/O interface timing for pin NL

OPERATING REQUIREMENTS: Serial I/O Interface: BiSS/SSI Protocol

Operating conditions: VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, IBP calibrated to 200 µA Tj = -40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI protocol (INTCFG = 00, NESSI = 0)						
I201	t_{frame}	Permissible Frame Repetition		*)	indefinite	
I202	t_C	Permissible Clock Period		250		ns
I203	t_{L1}	Clock Signal Hi-Level Duration		125		ns
I204	t_{L2}	Clock Signal Lo-Level Duration		125		ns
I205	t_{RQ}	REQ Signal Lo-Level Duration		125		ns
I206	t_{P3}	Output Propagation Delay		see Elec. Char. O07		
I207	t_{out}	Adaptive Slave Timeout		see Elec. Char. O08		
BiSS C protocol (INTCFG = 00, NESSI = 1)						
I208	t_{frame}	Permissible Frame Repetition		*)	indefinite	
I209	t_C	Permissible Clock Period		100		ns
I210	t_{L1}	Clock Signal Hi-Level Duration		50		ns
I211	t_{L2}	Clock Signal Lo-Level Duration		50		ns
I212	t_{busy}	Processing Time w/o Start Bit Delay	ACQMODE ≠ 00	$2\,t_C$		
I213	t_{busy}	Processing Time with Start Bit Delay	ACQMODE = 00, refers to Elec. Char. C01	t_{IPO}		
I214	t_{P3}	Output Propagation Delay		see Elec. Char. O07		
I215	t_{out}	Adaptive Slave Timeout		see Elec. Char. O08		
I216	t_{S1}	Setup Time: SLI stable before MAI hi → lo		25		ns
I217	t_{H1}	Hold Time: SLI stable after MAI hi → lo		10		ns

Note: *) Allow t_{out} to elapse.

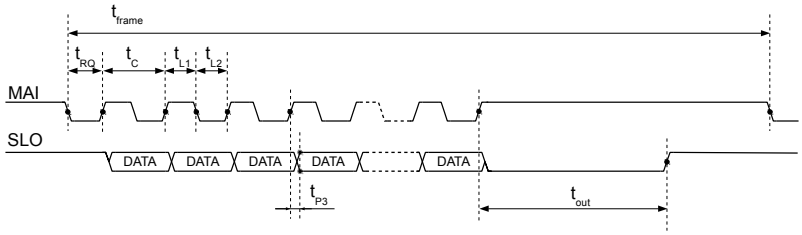


Figure 5: SSI protocol timing

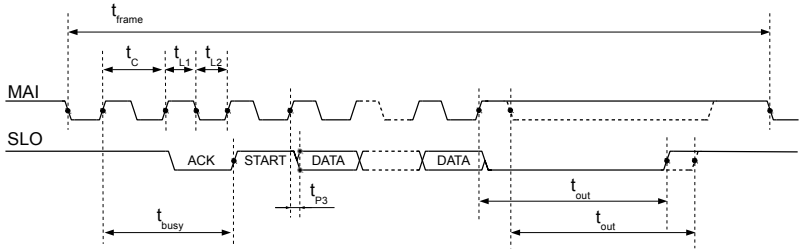


Figure 6: BiSS C protocol timing (ACQMODE ≠ 00)

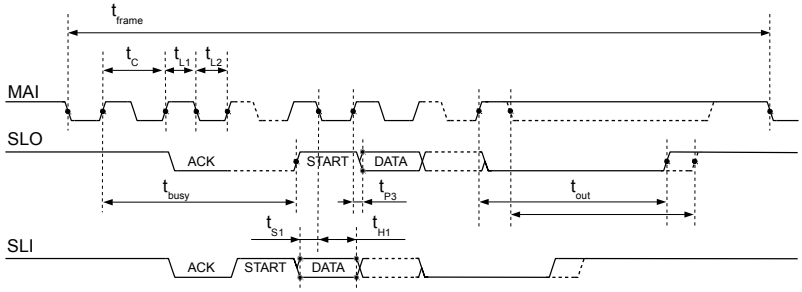


Figure 7: BiSS C protocol timing with triggered conversion (ACQMODE = 00) and chain operation

OPERATING REQUIREMENTS: Serial I/O Interface: SPI Protocol

Operating conditions: VDDA = VDD = 4.5...5.5 V, GNDA = GND = 0 V, IBP calibrated to 200 µA Tj = -40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI protocol (INTCFG = 10)						
I301	t_C	Permissible Clock Period		100		ns
I302	t_{L1}	Clock Signal Hi-Level Duration		50		ns
I303	t_{L2}	Clock Signal Lo-Level Duration		50		ns
I304	t_{S1}	Setup Time: NCS lo before MAI hi → lo		50		ns
I305	t_{H1}	Hold Time: NCS lo after MAI lo → hi		100		ns
I306	t_{W1}	Wait Time between Cycles: between NCS lo → hi to NCS hi → lo		100		ns
I307	t_{S2}	Setup Time: SLI stable before MAI lo → hi		25		ns
I308	t_{H2}	Hold Time: SLI stable after MAI lo → hi		10		ns
I309	t_{P3}, t_{P4}	Output Propagation Delay: SLO stable after MAI hi → lo		see Elec. Char. P10		

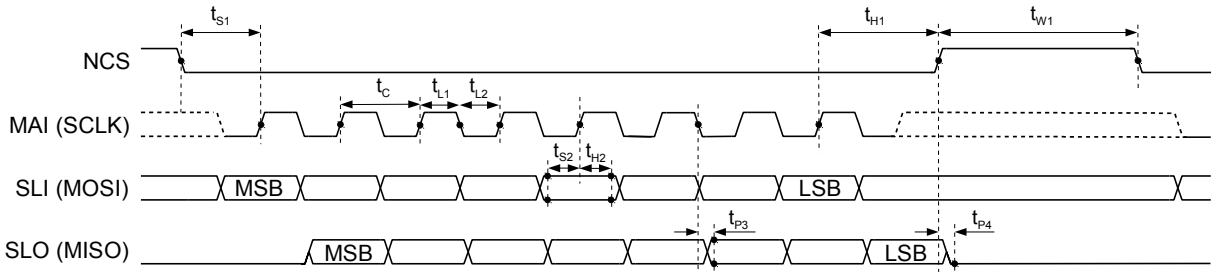


Figure 8: SPI protocol timing

CONFIGURATION PARAMETERS

REGISTER MAP

Configuration and output data register								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Amplitude control (configuration)								
0x00	ACOT(0)	ACOR(1:0)		ACOC(4:0)				
0x01	ACOD(6:0)							ACOT(1)
Signal conditioning (configuration)								
0x02	GFS(3:0)				LCMODE	GR(2:0)		
0x03	-	GFS(10:4)						
0x04	GFC(7:0)							
0x05	MPS(3:0)				-	GFC(10:8)		
0x06	-	-	MPS(9:4)					
0x07	MPC(7:0)							
0x08	-	-	ORS(1:0)		-	-	MPC(9:8)	
0x09	OFS(7:0)							
0x0A	0	-	ORC(1:0)		-	OFS(10:8)		
0x0B	OFC(7:0)							
0x0C	PH(3:0)				NEFDR	OFC(10:8)		
0x0D	SELREF(1:0)		PH(9:4)					
0x0E	INMODE	DCPOS	REFVOS(1:0)		TUIN	RIN(1:0)		UIN
0x0F	CFGBIAS(3:0)				SELBP	ENF	MODE(1:0)	
0x10	0	0	1	1	0	0	0	0
12-bit A/D converter and temperature monitoring (configuration)								
0x11	ADCSLOP(7:0)							
0x12	ADCOFF(7:0)							
0x13	ADCOFF(15:8)							
0x14	TEMPLO(7:0)							
0x15	TEMPLO(15:8)							
0x16	TEMPHI(7:0)							
0x17	TEMPHI(15:8)							
Interfaces (configuration)								
0x18	INTCFG(1:0)		FULL_CYC	GET_ADI	STP_ADI	CYC_ADI	SSIRING	SSIERR
0x19	ACQMODE(1:0)		ENLC	NESSI	ENXCRC	TMPSCD	SSIMODE(1:0)	
0x1A	DL_ADI(4:0)					SYNC_ADI(1:0)		SSI_ADI
Offset & interpolator (configuration)								
0x1B	STOFF(1:0)		0	0	0	DIR	CODERES(1:0)	
0x1C	STOFF(9:2)							
0x1D	STOFF(17:10)							
0x1E	STOFF(25:18)							
0x1F	MTOFF(7:0)							
0x20	MTOFF(15:8)							
0x21	MTOFF(23:16)							
Mask register for error and warning (configuration)								
0x22	EMSK_EXT	EMSK_ABS	EMSK_IPO	EMSK_KNF	EMSK_SYN	EMSK_TMP	EMSK_AMP	EMSK_RGL
0x23	WMSK_EXT	WMSK_ABS	WMSK_IPO	WMSK_KNF	WMSK_SYN	WMSK_TMP	WMSK_AMP	WMSK_RGL
Data resolution (configuration)								
0x24	MTRESO(2:0)			STRESO(4:0)				

Configuration and output data register								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Safety register (configuration)								
0x25	NRDOK	SEC_HI(6:0)						
0x26	CFG_E2P(1:0)		SEC_LO(5:0)					
CRC configuration (configuration)								
0x27	0	RES_ERR	CHK_ADI	0	0	0	0	0
0x28	CRCS(15:8)							
0x29	CRCS(7:0)							
Extended configuration								
0x2A	0	0	0	0	0	0	0	0
0x2B	0	0	0	0	THR_FAMP(1:0)		TO_FAMP	EN_FAMP
0x2C	0	0	0	0	0	0	0	0
. . .								
CRC sum (EEPROM) (configuration)								
0x2E	CRCCFG(15:8)							
0x2F	CRCCFG(7:0)							
. . .								
Bank select (configuration)								
0x40	-			BSEL(4:0)				
Device data (configuration)								
0x41	EDSBANK(7:0)							
0x42	PROFILE(15:8) (Position)							
0x43	PROFILE(7:0) (Position)							
0x44	SERIAL_ID(31:24)							
0x45	SERIAL_ID(23:16)							
0x46	SERIAL_ID(15:8)							
0x47	SERIAL_ID(7:0)							
0x48	PROFILE(15:8) (Temperature)							
0x49	PROFILE(7:0) (Temperature)							
. . .								
Diagnostic data (output data)								
0x5A	RG_MAX	AMP_MAX	DC_MAX	CMP_MAX	RG_MIN	AMP_MIN	DC_MIN	CMP_MIN
0x5B	reserved							
0x5C	reserved							
0x5D	reserved							
0x5E	reserved							
0x5F	reserved							
Status register / Command register (output data)								
0x60	INIT	ERR	WARN	EWKH	EWKL	BUSY	ADV	PDV
Position (output data)								
0x61	ST(1:0)		-					
0x62	ST(9:2)							
0x63	ST(17:10)							
0x64	ST(25:18)							
0x65	MT(7:0)							
0x66	MT(15:8)							
0x67	MT(23:16)							

Configuration and output data register								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Life counter (output data)								
0x68	LC(7:0)							
Error register (output data)								
0x69	ERR_EXT	ERR_ABS	ERR_IPO	ERR_KNF	ERR_SYN	ERR_TMP	ERR_AMP	ERR_RGL
Temperature (output data)								
0x6A	TEMP(7:0)							
0x6B	TEMP(15:8)							
CRC sum of output data (output data)								
0x6C	CRCPOS(7:0)							
0x6D	CRCPOS(15:8)							
. . .								
Device data (configuration)								
0x72	DEV_ID(47:40) (Temperature)							
0x73	DEV_ID(39:32) (Temperature)							
0x74	DEV_ID(31:24) (Temperature)							
0x75	DEV_ID(23:16) (Temperature)							
0x76	DEV_ID(15:8) (Temperature)							
0x77	DEV_ID(7:0) (Temperature)							
0x78	DEV_ID(47:40) (Position)							
0x79	DEV_ID(39:32) (Position)							
0x7A	DEV_ID(31:24) (Position)							
0x7B	DEV_ID(23:16) (Position)							
0x7C	DEV_ID(15:8) (Position)							
0x7D	DEV_ID(7:0) (Position)							
0x7E	MNFCT_ID(15:8)							
0x7F	MNFCT_ID(7:0)							

Table 8: Register map

OPERATING MODES

In order to calibrate iC-MR, to adjust the input signals, as well as to test iC-MR the operation mode must be altered. The operating mode can be selected by using the register MODE. The output functions of PSO, NSO, PCO and NCO change according to the various operating modes.

MODE(1:0) **MODE(4:2)**		**ADR 0x0F; bit 1:0** **ADR 0x10; bit 2:0**			
Code	Operating mode	Pin PSO	Pin NSO	Pin PCO	Pin NCO
0x00	Normal operation *	PSO	NSO	PCO	NCO
0x01	Analog 1	PS_W	NS_W	PC_W	NC_W
0x02	Analog 2	SVDC	CVDC	VREFI	IBP
0x03	Bypass	PSI	NSI	PCI	NCI
0x04	iC-Haus internal				
...					
0x1F	iC-Haus internal				
Note: *) Measurement condition: ENOCC = 1, ENOCM = 1, TIIN = 0, TIPOL = 0, TLDOS = 0					

Table 9: Operating mode

Calibration modes

In operation mode *Analog 1* the adjusted sine and cosine signals are being provided (PS_W, NS_W, PC_W and NC_W). In operation mode *Analog 2* bias current source (IBP), reference potential input (VREFI), as well as center potentials of calibration circuits for sine (SVDC) and cosine (CVDC) can be measured.

BIAS CURRENT SOURCE AND SIGNAL FILTER

Bias current source

The calibration of the bias current source in operating mode *Analog 2* is required for adherence to the given Electrical Characteristics and instrumental in the determination of the chip timing (e.g. SCL clock frequency). For adjusting the bias current source, the voltage drop is being measured using a 10 kΩ resistor from pin NCO to pin GNDA. The setpoint of 200 µA is reached with a measurement voltage of 2 V.

CFGBIAS	Addr 0x0F, bit 7:4		
Code k (signed)	$IBP \sim \frac{31}{31-k}$	Code k (signed)	$IBP \sim \frac{31}{31-k}$
0x0	100 %	0x8	79 %
0x1	103 %	0x9	81 %
0x2	107 %	0xA	84 %
0x3	111 %	0xB	86 %
0x4	115 %	0xC	88 %
0x5	119 %	0xD	91 %
0x6	124 %	0xE	94 %
0x7	129 %	0xF	97 %

Table 10: Bias calibration

Signal filter

In order to decrease the adjusted analog signals' noise iC-MR uses a signal filter which can be activated through register bit ENF.

ENF	Addr 0x0F, bit 2
Code	Function
0	Signal filter deactivated
1	Signal filter active

Table 11: Signal filter activation

Low pass cutoff frequencies can be adjusted using SELBP.

SELBP	Addr. 0x0F; bit 3
Code	Function
0	7.5 kHz (@ fin < 10 Hz)
1	15 kHz (@ fin < 10 Hz)

Table 12: Signal filter cutoff frequency

The filter's dead band can be activated using NEFDR.

NEFDR	Addr. 0x0C; bit 3
Code	Function
0	Filter dead band active
1	Filter dead band deactivated

Table 13: Signal filter dead band

SIGNAL CONDITIONING

Input configuration

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Referenced input signals can be processed by applying the input signals' reference voltage to negative inputs.

Signal adjustment is possible only in operating modes *Analog 1* and *Analog 2*. Figure 9 shows the sine channel's conditioning unit; the cosine channel's set-up is equivalent to it.

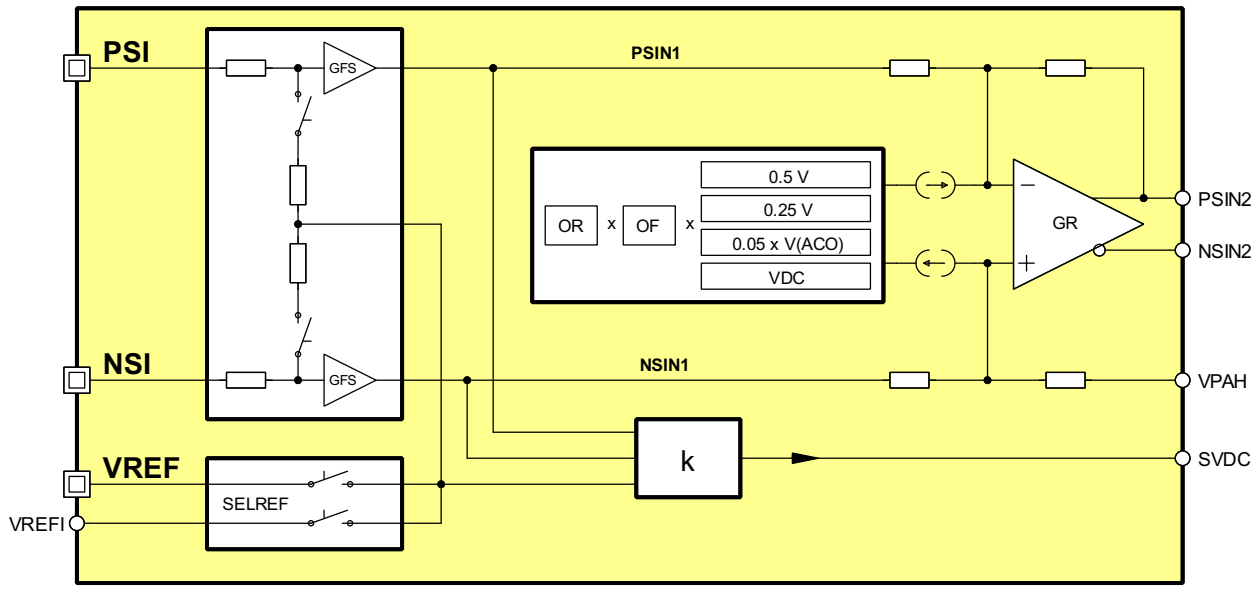


Figure 9: Signal-conditioning unit (sine channel)

INMODE	Addr 0x0E, bit 7
Code	Function
0	Differential input signals
1	Single-ended input signals

Table 14: Differential/single-ended signal mode

Both voltage and current signals can be accepted as input signals. For selection use register bit UIN.

UIN	Addr 0x0E, bit 0
Code	Function
0	Current input
1	Voltage input

Table 15: Current/voltage signal mode

In current mode an input resistor Rin() becomes active at each input pin, converting the current signal into a voltage signal. The input resistance Rin() consists of a pin resistor and the resistor Rui(), which is connected to the adjustable bias source VREFI. Tab. 16 shows the selection options. Indicated values of Rin() are typical, refer to Electrical Characteristics for tolerances.

The input resistance should be set so that center potentials SVDC and CVDC are between 125 mV and 250 mV (testable in operating mode Analog 2).

RIN	Addr 0x0E, bit 2:1		
Code	Nominal Rin()	Internal Rui()	Mode
00	1.7 kΩ	1.6 kΩ	Current input
01	2.5 kΩ	2.3 kΩ	Current input
10	3.5 kΩ	3.2 kΩ	Current input
11	4.9 kΩ	4.6 kΩ	Current input

Table 16: Input resistance

In voltage mode a voltage divider can be selected for high input amplitudes. This voltage divider reduces the input signal's amplitude to about 25%. The internal circuit corresponds to the circuit in current mode, just the resistor connecting the pin is altered.

TUIN	Addr 0x0E, bit 3		
Code	Nominal Rin()	Internal Rui()	Mode
0	high impedance	high impedance	Voltage input
1	20 kΩ	5 kΩ	Voltage input

Table 17: Input voltage divider

DCPOS	Addr 0x0E, bit 6	
Code	VREFI	Sensor type
0	2.5 V	Lowside current drain (I Mode)
1	1.5 V	Highside current source (I Mode)

Table 18: Reference voltage and current polarity

Parameter DCPOS determines the input reference voltage. In the generation of center potentials SVDC and CVDC it also determines whether the reference voltage VREFin() is being subtracted from the sum of the particular input signals or the sum is being subtracted from VREFin().

Parameter SELREF configures the input voltage reference.

SELREF	Addr 0x0D, bit 7:6	
Code	VREFin()	Pin function VREF
0x0, 0x1	internal	high impedance
0x2	internal	Output*: output of VREFI
0x3	external	Input**: external reference replaces VREFI
Notes	*) Do not load, buffer recommended. **) See Elec.Char. No.105 for permissible input voltage.	

Table 19: Reference source

Gain settings SIN and COS
The gain is set in four steps:

1. The sensor supply controller is shut down and the constant current source for the ACO output set to a suitable output current (register ADJ; current value close to the later operating point).

2. The coarse gain range is selected so that differential signal amplitudes of ca. 6 Vpp are produced at the core of the converter (signal PS_W versus NS_W and PC_W versus NC_W).

Note: The signals at the converter core output in calibration mode *Analog 1* are amplified by factor 3.

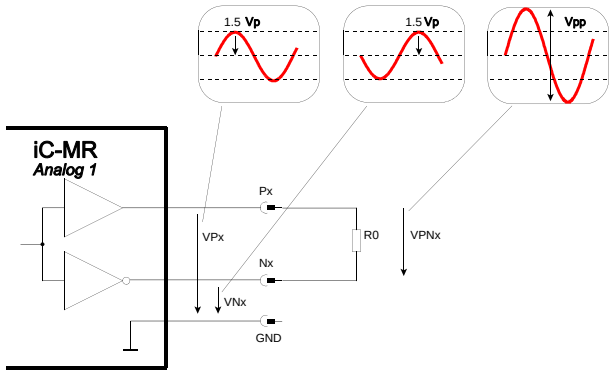


Figure 10: Measuring the differential signal amplitudes

3. Using fine gain factor GFS the sine signal amplitude is then adjusted to 6 Vpp.

4. The cosine signal amplitude can then be adjusted to the sine signal amplitude using fine gain factor GFC.

GR	Addr 0x02, bit 2:0
Code	Factor
0x0	2.0
0x1	4.1
0x2	5.3
0x3	6.7
0x4	8.7
0x5	10.5
0x6	13.2
0x7	16.0

Table 20: Coarse gain

GFS **GFC**	Addr 0x03, bit 6:0, Addr 0x02, bit 7:4 Addr 0x05, bit 2:0, Addr 0x04, bit 7:0
Code	Factor
0x000	1.0
0x001	1.0009
...	$6.25^{(GFx/1984)}$
0x7FF	6.6245

Table 21: Fine gain sine, cosine

Offset calibration SIN and COS
In order to calibrate the offset the reference source must first be selected using register REFVOS. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which provide stable, self-regulated signals.

So that photosensors can be operated in optical encoders iC-MR tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled sensor current source for LED

supply (output ACO). The VDC potential automatically tracks higher photocurrents. In order to use this function intermediate potentials SVDC and CVDC have to be adjusted to a minimal AC ripple using the selectable k factor of parameters MPS and MPC (see Table 23). If the gain setting is altered, this calibration has to be repeated. When single-ended operating mode is selected via register bit INMODE (see Table 14) MPS and MPC have no impact and the applied voltage at the negative input replaces the configurable sum voltage in the VDC generation.

The feedback of pin voltage V(ACO) fulfills the same task as source VDC when MR bridge sensors are supplied by the controlled sensor current source. In this case the justification of intermediate potentials MPS and MPC is unnecessary.

REFVOS	Addr 0x0E, bit 5:4
Code	Source type
0x0	Feedback of pin voltage V(ACO): V(ACO)/20 for supply-dependent diff. voltage signals for Wheatstone measuring bridges to measure VDDS
0x1, 0x2	Fixed reference: 0x1 = V05 of 500 mV, 0x2 = V025 of 250 mV for single-ended current or voltage signals for single-ended or differential stabilized signals (regulated sensors, frequency generator)
0x3	Self-tracking sources VDC1, VDC2 (125...250 mV) for differential current signals for differential voltage signals*
Note	*) Requires SELREF = 0x3 and the supply of pin VREF with the sensor's reference potential (see Elec. Char. No. 105 for acceptable input voltage).

Table 22: Offset reference source

MPS	Addr 0x06, bit 5:0, Addr 0x05, bit 7:4
MPC	Addr 0x08, bit 1:0, Addr 0x07, bit 7:0
Code	$VDC = k * VPi + (1 - k) * VNi$
0x000	$k = 0.33$
0x001	$k = 0.33032$
...	... $k = 0.33 + Code \cdot 0.00032$
0x200	$k = 0.50$ (center setting)
...	...
0x3FF	$k = 0.66$
Note	Adjustment required only if VOSREF = 0x3

Table 23: Center potentials sine, cosine

The offset calibration range is dependent on the selected REFVOS source and is adjusted using registers ORS and ORC. The actual offset calibration happens through adjusting factors OFS and OFC after having selected the calibration range. The calibration target is reached when the DC rate of the differential signals V(PSO)-V(NCO) and V(PCO)-V(NCO) is zero.

ORS	Addr 0x08, bit 5:4
ORC	Addr 0x0A, bit 5:4
Code	Range
0x0	maxVOS = 3 * VOSREF
0x1	maxVOS = 6 * VOSREF
0x2	maxVOS = 18 * VOSREF
0x3	maxVOS = 36 * VOSREF
Note	The maximum offset calibration range refers to the internal calibrated signals (calibration mode Analog 1, see page 19)

Table 24: Offset calibration range sine, cosine

The principle interpolation accuracy of the sine/cosine signals in dependency with the selected calibration range as well as the size of an LSB are exemplarily illustrated for some values in the following table.

Range x Source	maxVOS	Cal. step size (LSB)	Limitation of angle precision @ 100 % (6 Vpp) @ 50 % (3 Vpp)
3 x 0.25 V	750 mV	733 µV	none (>13 bit) none (>13 bit)
6 x 0.25 V	1.5 V	1466 µV	0.03°, >13 bit 0.06°, ca. 12 bit
6 x 0.5 V	3 V	2933 µV	0.06°, ca. 12.5 bit 0.11°, ca. 11.7 bit
18 x 0.5 V	9 V	8798 µV	0.17°, ca. 11 bit 0.34°, ca. 10 bit

Table 25: Offset calibration and impact on the angle precision

OFS	Addr 0x09, bit 7:0, Addr 0x0A, bit 2:0		
OFC	Addr 0x0B, bit 7:0, Addr 0x0C, bit 2:0		
Code	Factor OF	Code	Factor OF
0x000	0	0x400	0
0x001	0.00098	0x401	−0.00098
...	$0.00098 * OFx$	...	$-0.00098 * OFx$
0x3FF	1	0x7FF	−1

Table 26: Offset calibration sine, cosine

The calibrated offset is generated through
$VOS() = maxVOS * OF$

Phase correction SIN vs. COS

The phase shift between sine and cosine can be adjusted using register value PH. If the phase error is too high, some calibration parameters may have to be adjusted again (those are amplitudes, intermediate potentials and offset voltages).

PH	Addr 0x0D, bit 5:0, Addr 0x0C, bit 7:4		
Code	Correction angle	Code	Correction angle
0x000	+0	0x200	−0
0x001	+0.0204	0x201	−0.0204
...	+0.0204 ∗ *PH*	...	−0.0204 ∗ *PH*
0x1FF	+10.42	0x3FF	−10.42

Table 27: Phase correction sine vs. cosine

AMPLITUDE CONTROL

iC-MR allows the amplitude of the output signals at pins PSO, NSO, PCO, and NCO to be kept constant - regardless of temperature and ageing effects - by tracking the sensor supply. For this purpose iC-MR has a controlled current source at pin ACO which can power the external sensor. The driver capability of this current source is selected by ACOR, the control mode by ACOT.

ACOR	Addr 0x00, bit 6:5
Code	Function
00	5 mA - range
01	10 mA - range
10	25 mA - range
11	50 mA - range

Table 28: ACO Output current range (for control operation and constant current source)

ACOT	Addr 0x01, bit 0; Addr 0x00, bit 7
Code	Function
00	SIN/COS square control
01	Sum control
10	Combined Sum and SIN/COS square control
11	Constant current source

Table 29: ACO Output control principle

LCMODE	Addr 0x02, bit 3
Code	Function
0	Optimized control
1	Standard control

Table 30: Control mode

In sum control mode the sine and cosine DC values (SVDC and CVDC) are added together and regulated to the setpoint. The setpoint is configured using register ACOD.

ACOD	Addr 0x01, bit 7:1
Code	**Sum mode** ACOT = 01
0x00	VDC1 + VDC2 ≈ 166 mV
0x01	VDC1 + VDC2 ≈ 167 mV
...	VDC1 + VDC2 ≈ 166 mV $\frac{109}{109-(0.6*Code)}$
0x7F	VDC1 + VDC2 ≈ 551 mV

Table 31: DC Setpoint sum control

Square control mode keeps the sum of the sine/cosine amplitude squares at a constant value. Register ACOC adjusts the setpoint for analog output ACO.

ACOC	Addr 0x00, bit 4:0
Code	**Square mode** ACOT = 00
0x00	Vpp() ≈ 300 mV (60 %)
0x01	Vpp() ≈ 305 mV (61 %)
...	Vpp() ≈ 300 mV $\frac{77}{77-(1.25*Code)}$
0x19	Vpp() ≈ 500 mV (98 %)
...	...
0x1F	Vpp() ≈ 600 mV (120 %)

Table 32: AC Setpoint square control

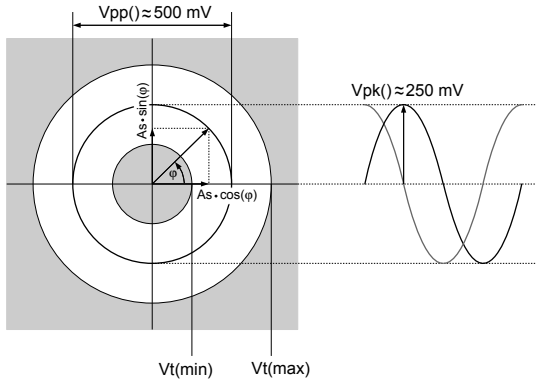


Figure 11: Control monitoring according to setpoint of square control (example: ACOC = 0x19; for Vt()min or Vt()max; see Elec. Char. Nos. 809 and 810).

As opposed to square mode, sum mode gives a higher accuracy. However, at higher signal frequencies it cannot compensate for a reduction in the signal amplitude caused by the amplifier cut-off frequency of the sensors. The device thus has a combined control mode which utilizes both control modes, sum and square (see Table 29). In this mode sum control is applied at low frequencies, with square control coming into play at frequencies exceeding the cut-off frequency of the sensor's amplifiers. So that this control mode functions correctly, the set signal amplitude for square control mode must be lower than that for sum control.

The control's operating range and the input signal amplitudes supplied to the control unit are both monitored. Should any error occur during monitoring, these can be output.

So that the signals at the input pins PSO, NSO, PCO, and NCO can be calibrated without control interference, the current source at pin ACO can be set to a constant current (Table 29).

ACOC	Addr 0x00, bit 4:0
Code	**Constant current source** ACOT = 11
0x00	I(ACO) ≈ 3.125 % Isc(ACO)
0x01	I(ACO) ≈ 6.250 % Isc(ACO)
...	I(ACO) ≈ 3.125 % * (Code + 1) * Isc(ACO)
0x1F	I(ACO) ≈ 100 % Isc(ACO)
Note	Refer to Elec. Char. No. 802 for Isc(ACO).

Table 33: Setpoint current source (ACO output current)

SIGNAL MONITORING

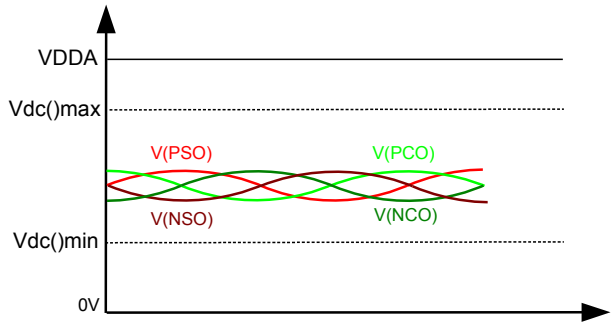


Figure 12: DC level monitoring: max. and min. voltage thresholds according to Elec. Char. Nos. B04 and B05.
For error messaging refer to diagnosis register, page 47.

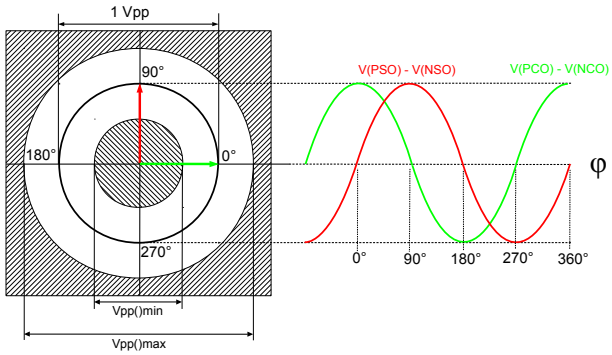


Figure 13: AC level monitoring: differential voltage thresholds according to Elec. Char. Nos. B01 and B02.
For error messaging refer to diagnosis register, page 47.

The signal monitoring circuit verifies that all four analog signal lines show an acceptable DC voltage (within approx. 1.75 V to 3.12 V typically) and that both differential signals, sine and cosine, show an acceptable AC amplitude (within approx. 0.35 Vpp to 1.3 Vpp typically).

The AC monitoring circuit uses an analog multiplier and evaluates the Lissajous figure derived from the square sum signal of sine and cosine $(\sin(wt)^2 + \cos(wt)^2)$.

Independent comparators for DC and AC monitoring thresholds then stipulate the signal error messages DC_MAX, DC_MIN and CMP_MAX, CMP_MIN (refer to diagnosis register, page 47).

Note: If a fractured cable needs to be detected, each analog input may require an external pull-down resistor to drag the DC potential into the error range.

12-BIT A/D CONVERTER

The IC features a 12-bit A/D converter, which output data is stored in the TEMP register and can be read out from here through the interfaces. The A/D converter operates constantly, updating the data in register TEMP after each conversion. The TEMP register cannot be read by bytewise access to addresses 0x6A and 0x6B, as otherwise it is not guaranteed that a contiguous data word is read out. The temperature data must be read out by the cyclic telegram.

The A/D converter can be calibrated using registers ADCSLOP and ADCOFF. Register ADCSLOP has 8 bits and is used to set the maximum voltage the converter can process at pin ADC. The allocation of the register data in ADCSLOP to the maximum voltage is expressed in Table 34. Using the second calibration register ADCOFF, which has 16 bits, an offset can be added to the converter's digital output data.

ADCSLOP	Addr. 0x11; bit 7...0	R/W
Code	Full scale level for VDDA = 5V	
0x00	2.0 V	
0x01	2.00196 V	
...	2.0 V + 1.96 mV * ADCSLOP	
0xFF	2.5 V	

Table 34: Maximum ADC input voltage

ADCOFF	Addr. 0x12...0x13;	R/W
Code	Function	
0x7FFF	TEMP = TEMP(int) + 32767	
...		
0x0001	TEMP = TEMP(int) + 1	
0x0000	TEMP = TEMP(int)	
0xFFFF	TEMP = TEMP(int) - 1	
...		
0x8000	TEMP = TEMP(int) - 32768	

Table 35: Digital temperature offset

Registers TEMPHI and TEMPLO define the upper and lower thresholds for error output. If the current converter value is above TEMPHI or below TEMPLO, the ERR_TMP alarm bit is set in the error register. The internal ADC can be utilized to continuously record an external temperature, for which a temperature-dependent voltage is applied at pin ADC. This can be generated by a KTY temperature sensor. A temperature monitor can be created using thresholds TEMPHI and TEMPLO. By way of example, the following describes the evaluation of temperature sensor KTY 84.

TEMPLO	Addr. 0x14...0x15;	R/W
TEMPHI	Addr. 0x16...0x17;	R/W
Code	Temperature threshold	
0x7FFF	+3276.7 °C	
...	...	
0x07D0	+200.0 °C	
...	...	
0x0001	+0.1 °C	
0x0000	0.0 °C	
0xFFFF	-0.1 °C	
...	...	
0xFE70	-40 °C	
...	...	
0x8000	-3276.8 °C	
Note	Thresholds for example KTY 84	

Table 36: Temperature thresholds

Figure 14 shows a schematic circuit diagram for the evaluation of the KTY. A resistor of approximately 2.3 kΩ is switched in series with the KTY sensor to linearize the voltage supplied by the KTY. This results in a linear temperature voltage.

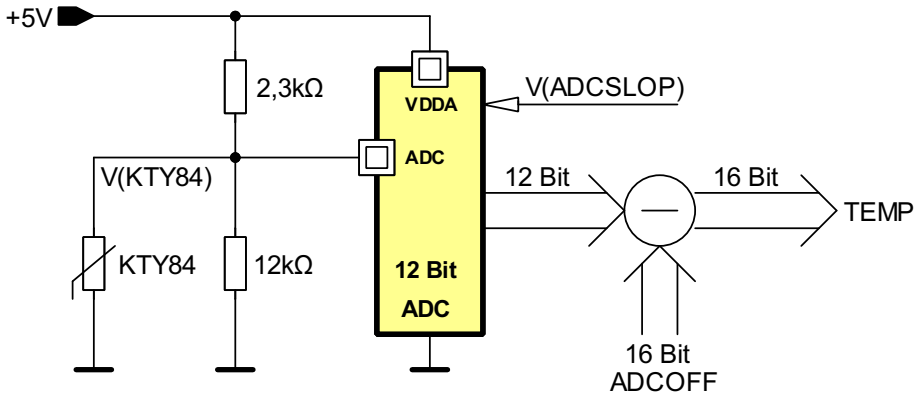


Figure 14: Schematic circuit diagram for the evaluation of KTY sensors.

The temperature is output according to Table 37 as a 16-bit value in two's complement format with a resolution of 1/10°C.

TEMP	Addr 0x6B, 0x6A, bits: 15..8, 7..0	
Code	Temperature	Validity
0x7FFF ...	+3276.7 °C ...	Out of measuring range
0x07D0 ... 0x0001 0x0000 0xFFFF ... 0xFE70	+200.0 °C ... +0.1 °C 0.0 °C -0.1 °C ... -40 °C	Measuring range
... 0x8000	... -3276.8 °C	Out of measuring range

Table 37: Temperature data

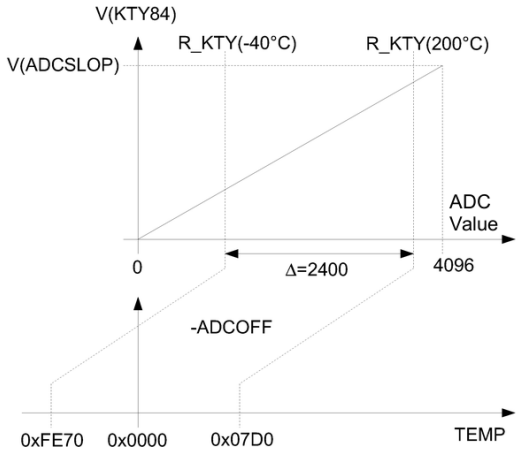


Figure 15: Calibrating the temperature sensor to the output format

To obtain the output given in Table 37 the evaluation circuitry is calibrated as follows:

1. The maximum convertible voltage is set and thus the increase in the converter using register ADCSLOP. ADCSLOP's register is set so that there is a difference of 2,400 between the converter values at R(KTY84) = 359 Ω and R(KTY84) = 1,722 Ω.
2. To map ADC's output onto the range of values given in Table 37, an offset is added through register ADCOFF. The data in register ADCOFF is set so that 0xFE70 is read at R(KTY84) = 359 Ω and, correspondingly, 0x07D0 at R(KTY84) = 1,722 Ω.
   (a) Read out converter data from register TEMP with ADCOFF = 0x0000 at R(KTY84) = 359 Ω.
   (b) Calibration data = converter data + 400
   (c) Write the calibration data to register ADCOFF.

INTERPOLATION AND CYCLE COUNTING

The configurable 37-bit cycle counter compares the sine and cosine signals in order to count cycles independent of requests for position data.

The interpolator resolves one signal cycle of the calibrated sine and cosine signals to 13 bits for each position data request. It then synchronizes this with the cycle counter in order to ensure a consistent position data word at all times.

Using register CODERES, it is possible to adapt the bit length of the cycle counter to the output format. If, for example, a total data length of 48 bits is required at 13-bit interpolation, the value ’10’ is used as the configuration for CODERES.

CODERES	Addr. 0x1B; bit 1...0			R/W
Code	Cycle Counting	Multiturn	Singleturn	Interpol.
00	37 bit	24 bit	13 bit	13 bit
01	36 bit	24 bit	12 bit	13 bit
10	35 bit	24 bit	11 bit	13 bit
11	34 bit	24 bit	10 bit	13 bit

Table 38: Cycle counter length

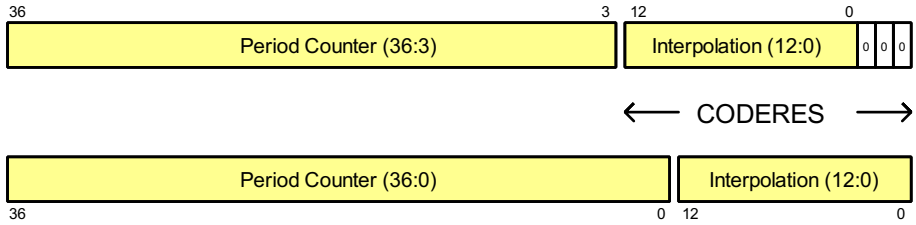


Figure 16: Adjusting the counter depth

Adjustment of data direction
Parameter DIR selects between an increasing or decreasing data direction for the adaption of the position data to the mechanical movement.

DIR	Addr. 0x1B; bit 2	R/W
Code	Code direction	
0	Code direction not inverted	
1	Code direction inverted	

Table 39: Code direction

Position preset by offset correction
An offset for singleturn (STOFF) and multiturn (MTOFF) data can be defined to adapt the absolute position data to a mechanical position. These offsets are subtracted from the existing data.

STOFF	Addr. 0x1E; bit 7...0 Addr. 0x1D; bit 7...0 Addr. 0x1C; bit 7...0 Addr. 0x1B; bit 7...6	R/W
Code	Function	
0x00 0x3FFFFFF	Offset value	

Table 40: Singleturn offset

MTOFF	Addr. 0x21; bit 7...0 Addr. 0x20; bit 7...0 Addr. 0x1F; bit 7...0	R/W
Code	Function	
0x00 0xFFFFFF	Offset value	

Table 41: Multiturn offset

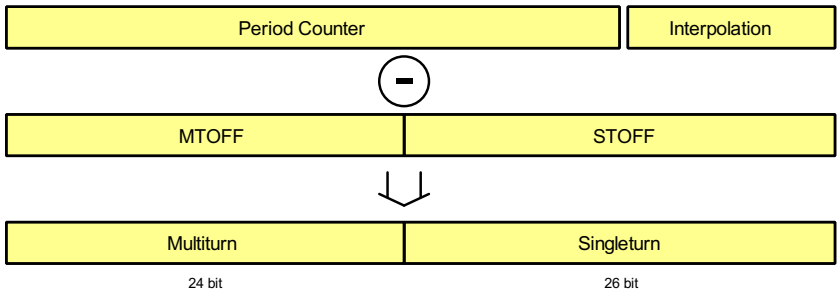


Figure 17: Position data generation with offset correction

Multiturn data length
MTRESO selects the resolution of the multiturn data for the parallel I/O interface and the SPI interface. For BiSS and SSI protocols, selected data lengths are assigned depending on the MTRESO setting.

If the MT resolution is reduced, the multiturn data is right justified and the upper bits are zeroed. The total output data length can be longer depending on the selected output interface.

MTRESO	Addr. 0x24; bit 7...5		R/W
Code	MT resolution: serial SPI or parallel	MT resolution: BiSS or ext. SSI	MT resolution: 13-bit / 25-bit SSI
0x0	24 bit	24 bit	0 bit / 12 bit
0x1	20 bit	24 bit	0 bit / 12 bit
0x2	16 bit	24 bit	0 bit / 12 bit
0x3	12 bit	12 bit	0 bit / 12 bit
0x4	8 bit	12 bit	0 bit / 12 bit
0x5	4 bit	12 bit	0 bit / 12 bit
0x6	0 bit	0 bit	0 bit / 12 bit
0x7	0 bit	0 bit	0 bit / 12 bit

Table 42: Multiturn resolution

Singleturn data length
STRESO selects the resolution of the singleturn data for the parallel I/O interface and the SPI interface. For BiSS and SSI protocols, a fixed data length is assigned.

If the ST resolution is reduced, the data is left justified. If the output data length is longer, depending on the selected output interface, the data is filled with zeros. This generates a permanently contiguous position data word from the right-aligned multiturn data and the left-aligned singleturn data.

The interpolator data resolution of 13 bit is fixed; only its position in the data word can be shifted by CODERES (Table 38).

STRESO	Addr. 0x24; bit 4...0		R/W
Code	ST resolution: serial SPI or parallel	ST resolution: BiSS or ext. SSI	ST resolution: 13-bit / 25-bit SSI
0x00	26 bit	26 bit	13 bit / 13 bit
0x01	25 bit	26 bit	13 bit / 13 bit
0x02	24 bit	24 bit	13 bit / 13 bit
...	...	...	...
0x0D	13 bit	24 bit	13 bit / 13 bit
0x0E	12 bit	24 bit	13 bit / 13 bit
...	...	...	...
0x19	1 bit	24 bit	13 bit / 13 bit
0x1A	0 bit	24 bit	13 bit / 13 bit
...	...	...	...
0x1F	0 bit	24 bit	13 bit / 13 bit

Table 43: Singleturn resolution

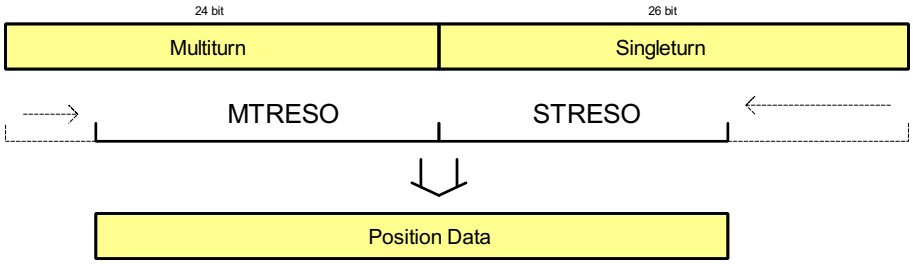


Figure 18: Reduction of data length

Position data acquisition modes
There are three different operating modes for acquiring position data which are selected by ACQMODE.

In **normal conversion** mode, new data is generated on each request for position data and then output after end of conversion.

ACQMODE	Addr. 0x19; bit 7...6	R/W
Code	Function	
00	Normal conversion with processing time	
01	Pipeline conversion without processing time	
10	Continuous conversion without processing time	
11	Continuous conversion with interpolation of interim values *	
Note	*) Only for serial I/O interface with SSI protocol	

Table 44: Position data acquisition

In **pipeline conversion** mode, data is also generated on each request, however, with each new request the data from the last conversion is output in order to hide the processing time. In this mode, the PDV bit is set statically in the status register and the ERR_IPO bit in the error register continues to signal the status or processing time of the interpolator. Pipeline mode is available in both the parallel and the serial I/O interfaces with the SSI and BiSS C protocol.

In **continuous conversion** mode, position data is updated automatically regardless of external requests in intervals of 64 clock cycles (approx. each 4.3 µs for an oscillator frequency of 15 MHz). The data output comes from the most recent conversion with the advantage of immediate availability, just slightly asynchronous to the external request.

In **continuous conversion with interpolation** of interim values, interpolated intermediate position data can be output at any time. This conversion mode is only available with the serial I/O interface in SSI, as SSI limits the acquisition time depending on the clock rate.

If a continuous conversion mode is active (ACQMODE = 10 or 11), conversion can be temporarily interrupted by pin NL using the enable acquire function.

NL (Enable Acquire Function)	
Level	Function
1	Convert as soon as the interpolator is free
0	Do not convert

Table 45: Special function of pin NL

ABSOLUTE DATA INTERFACE (ADI)

Through the serial absolute data interface (ADI) the cycle counter can be preloaded to a required value. Pin AMAO outputs the master clock and the slave's data is taken back at pin ASLI. The interface consists of a BiSS master which can be configured for BiSS C or SSI by SSI_ADI.

SSI_ADI	Addr. 0x1A; bit 0	R/W
Code	Function	
0	BiSS C protocol	
1	SSI protocol	

Table 46: Protocol of absolute data interface

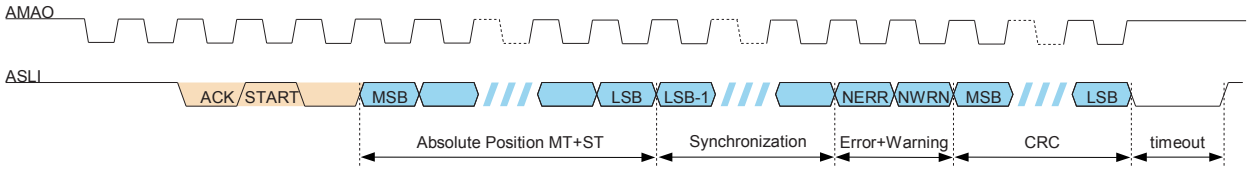


Figure 19: ADI data frame with BiSS protocol

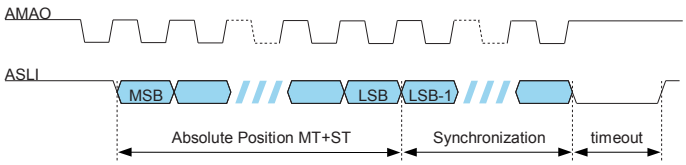


Figure 20: ADI data frame with SSI protocol

BiSS Master Performance		
Parameter	Symbol	Description
Clock Rate	t_C	7.5 MHz (@ f_{osc} = 15 MHz)
Line Delay	t_{P0}	Not adaptive, 80 ns max. accepted
Process.T.	t_{busy}	Compensated to 34 µs max.
Timeout	t_{out}	Accepted between 200 ns to 40 µs
Control Data Channel		
Bit/cycle	ID	Description
1	CDS	Not evaluated by iC-MR
Single Cycle Data Channel		
Bit/cycle	ID	Description
0...48	DATA	Adjustable to absol. position data of: MT 0, 8, 12, 16, 24 bit ST 0 to 24 bit with sync. by 0 to 3 bit
1	nE	Error bit (low active) Reported by ERR_ABS of error reg.
1	nW	Warning bit (low active) Not forwarded or evaluated by iC-MR.
6	CRC	Polynomial 0x43 ($x^6 + x^1 + x^0$), start value 0x00 (bit inverted transmission)

Table 47: BiSS master performance (ADI)

SSI Master Performance		
Parameter	Symbol	Description
Clock Rate	t_C	940 kHz (@ f_{osc} = 15 MHz)
Timeout	t_{out}	Accepted between 1 µs to 40 µs
Single Cycle Data Channel		
Bit/cycle	ID	Description
0...48	DATA	Adjustable to absol. position data of: MT 0, 8, 12, 16, 24 bit ST 0 to 24 bit with sync. by 0 to 3 bit

Table 48: SSI master performance (ADI)

The following parameters define further interface functions. Bit STP_ADI controls the readin of absolute data during startup. If set, and after the EEPROM has been successfully read out, absolute data is read in by the ADI and presets the cycle counting. Alternatively, absolute data can be read in at a later stage by command.

STP_ADI	Addr. 0x18; bit 3	R/W
Code	Function	
0	Startup without reading absolute data	
1	Startup with reading absolute data and preset of cycle counting	
Note	The cycle counter starts from zero if no data is read or an error occurs (refer to status bit ADV, page 45).	

Table 49: Startup with absolute data

Bit CYC_ADI controls the cyclic readin of absolute data. If set, absolute data is read in intervals of approx. 550 µs, provided the absolute data interface is not busy.

CYC_ADI	Addr. 0x18; bit 2	R/W
Code	Function	
0	No cyclic reading of absolute data	
1	Cyclic reading of absolute data: for counter verification (CHK_ADI = 1) or counter initialization (CHK_ADI = 0)	

Table 50: Cyclic reading of absolute data

CHK_ADI is used to check the counted value versus a cyclically read absolute value. If the two values differ, error bit ERR_ABS will be set.

CHK_ADI	Addr. 0x27; bit 5	R/W
Code	Function	
0	No counter verification	
1	Cyclic counter verification versus ADI absolute data	

Table 51: Cyclic check of absolute data

Register DL_ADI defines the data length read in by the absolute data interface.

DL_ADI	Addr. 0x1A; bit 7...3	R/W
Code	Data Length*	Application Example
0x00	0 bit	
0x01	1 bit	0 bit MT / 1 bit ST*
...	...	
0x0C	12 bit	0 bit MT / 12 bit ST*
...	...	
0x17	23 bit	0 bit MT / 23 bit ST*
0x18	24 bit	0 bit MT / 24 bit ST*
0x19	32 bit	8 bit MT / 24 bit ST*
0x1A	36 bit	12 bit MT / 24 bit ST*
0x1B	40 bit	16 bit MT / 24 bit ST*
0x1C	48 bit	24 bit MT / 24 bit ST*
...	...	
0x1F	48 bit	
Note	*) Includes the bits used for synchronization.	

Table 52: Data length absolute data interface

Register SYNC_ADI sets the number of synchronization bits used to synchronize the data on the internal cycle counter.

SYNC_ADI	Addr. 0x1A; bit 2...1	R/W
Code	Function	
00	Use 0 bit for synchronization	
01	Use 1 bit for synchronization	
10	Use 2 bit for synchronization	
11	Use 3 bit for synchronization	

Table 53: Synchronization of absolute data

Note: A read access by the parallel I/O interface will be answered suitably delayed if the absolute data interface would be busy; a read access by the serial I/O interface running the BiSS protocol would be answered with zero data (all data bits including error/warning are zero, all CRC bits are one).

If the serial I/O interface is operated in SPI mode in conjunction with the cyclic readin of absolute data, position values must be inquired by pin NL.

Direct communication with the sensor at ADI

In order to access the BiSS C sensor connected up to the absolute data interface, bit GET_ADI permits the interface signals to be looped through to the absolute data interface.

To this end the master clock received at clock input MAI is forwarded to clock output AMAO, and the data read at ASLI is used internally in place of input SLI. The sensor connected up to the ADI is then allocating slave ID 0, and iC-MR is taking slave ID 1.

When routing signals in this manner it is not possible to read in the absolute data of the connected sensor for internal calculation. Bit GET_ADI must first be disabled.

GET_ADI	Addr. 0x18; bit 4	R/W
Code	Function	
0	Normal operation, no loop through of BiSS signals	
1	BiSS signal routing altered (readout of absolute data not possible)	

Table 54: Absolute data interface daisy chain

STARTUP AND I/O INTERFACE SELECTION

Startup with EEPROM

Upon power-up and undervoltage reset, iC-MR accesses the external EEPROM to source its CRC-protected configuration data.

If the configuration data is not confirmed by its CRC in the first trial (for example when an EEPROM is connected up that has not yet been programmed), all configuration registers are zeroed, the error bit ERR_KNF is set, and the serial I/O interface is activated with the SSI protocol.

Additionally, data output SLO is kept permanently high (at VDD level) to block the transmission of invalid position data.

Note: A locked output SLO can only be resolved by a successful CRC verification over renewed configuration data. For this purpose iC-MR evaluates the BiSS control bit CDM even during SSI.

Startup without EEPROM

In lack of an EEPROM, or if after three attempts no successful I^2C communication has been established with the EEPROM (lack of acknowledge would indicate that the EEPROM is faulty or not connected), all configuration registers are zeroed and the error bit ERR_KNF is set.

In this case the pin levels of SCL and SDA are evaluated and preset register INTCFG:
INTCFG(1) is set by the pin level of SCL and
INTCFG(0) by the pin level of SDA.

Startup without EEPROM		
SCL level	SDA level	Activated interface
1	1	Parallel I/O interface
1	0	Serial I/O interface with SPI protocol
0	0	Serial I/O interface with SSI protocol
0	1	Not permissible
NB: Configuration error ERR_KNF will be set in any case.		

Table 55: Interface selection without EEPROM

I/O Interface Selection

Register INTCFG selects if the parallel or the serial I/O interface is used, and which serial communication protocol (BiSS, SSI, or SPI). Only one of the two interfaces may be active.

During startup register INTCFG is usually configured by the connected EEPROM. However, during operation it is possible to edit INTCFG without an immediate impact on the function. The change then needs to be stored to the EEPROM and comes into play after cycling power.

INTCFG	Addr. 0x18; bit 7...6	(R/W)
Code	Function	
11	Parallel I/O interface	
10	Serial I/O interface with SPI protocol	
00	Serial I/O interface with BiSS protocol (NESSI = 1) or SSI protocol (NESSI = 0)	
01	Not permissible	

Table 56: Interface selection

PARALLEL I/O INTERFACE

The parallel I/O interface enables sensor and register data to be read out through pins NCS, NRD, NWR, NL, and D0 to D7. After a reset or when inactive the interface is in read mode (data pins D(7:0) are tristate, address transfer is expected). If the internal data bus is busy due to an EEPROM readout after the reset, for instance (i.e. if the BUSY bit is active in the status byte), all read accesses are answered by the status byte through the parallel I/O interface.

Note: The parallel I/O interface can not be simultaneously operational with a serial I/O interface.

Reading out registers

iC-MR's parallel I/O interface enables internal registers to be accessed for readout. To this end the required register address must first be written to, after which the data at this address can be read out.

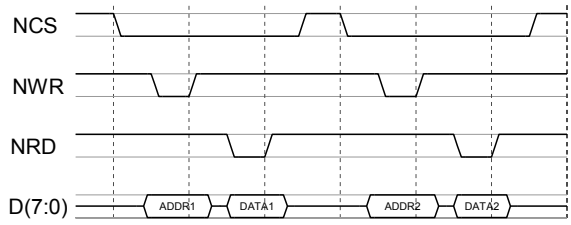


Figure 21: Readout process

Writing to registers

The internal registers can be written through the parallel I/O interface. To this end the required register address and then the relevant data word must be written to. Write mode is selected by NWR = 0. The first write access sets the register address and has no effect on the register content. The second write access writes the data at the bus to the addressed register.

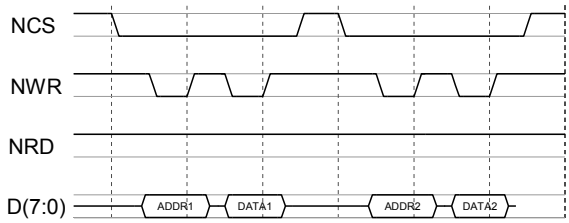


Figure 22: Write process

A simultaneous low signal for NRD and NWR is not permissible; the interface behavior is not defined for this configuration.

Reading out position data

Position data can be requested through the parallel I/O interface in two different ways:

- by an implemented command
- by a low signal through pin NL.

To read out position data on an implemented command, command register CMD must be written with the request command 0x00. Depending on the set configuration, singleturn, multiturn, and interpolator data is then provided for readout. Each request command increases the life counter by one.

Position data is marked as valid by bit PDV being set in the status register. Only after this has occurred position data should be read out at the relevant register addresses. Here, data is read out on a normal read register access.

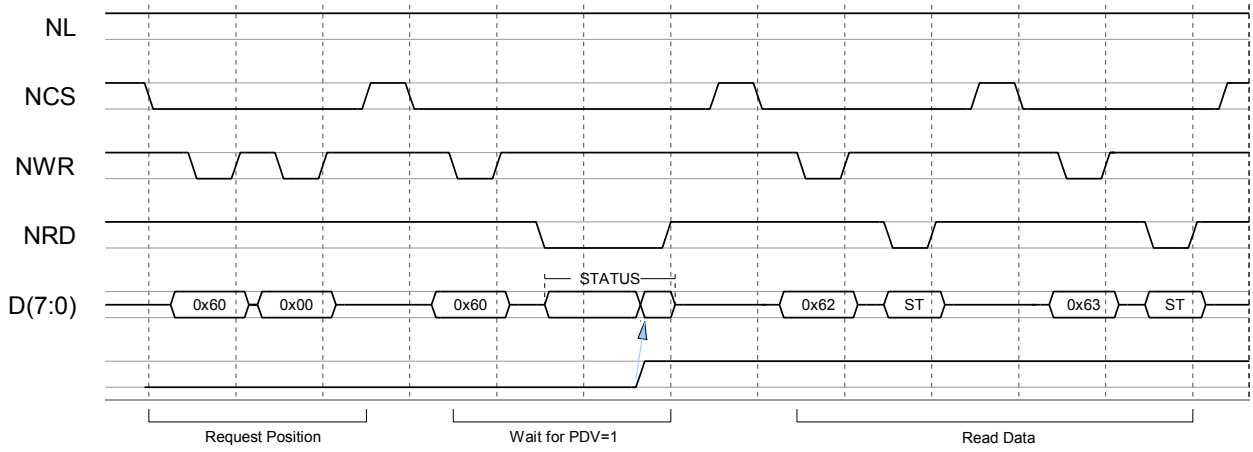


Figure 23: Position data output at request by command

If it is not possible to extend the NRD pulse to wait for data validity, the status register must be continually read out anew until pin D0 supplies a high (PDV = 1). After this, the position data can be read out on a read register access.

As the position data registers are read out individually following a request for position data by command, no CRC is formed across the position data. The life counter function continues to be active, however.

When reading out position data through pin NL, the request is made directly on the falling edge at pin NL. While NL = low, the status and position data are output on consecutive read accesses (NRD = high → low → high).

It is not necessary to write to the register addresses in this operating mode, as this is only used for the fast readout of sensor data.

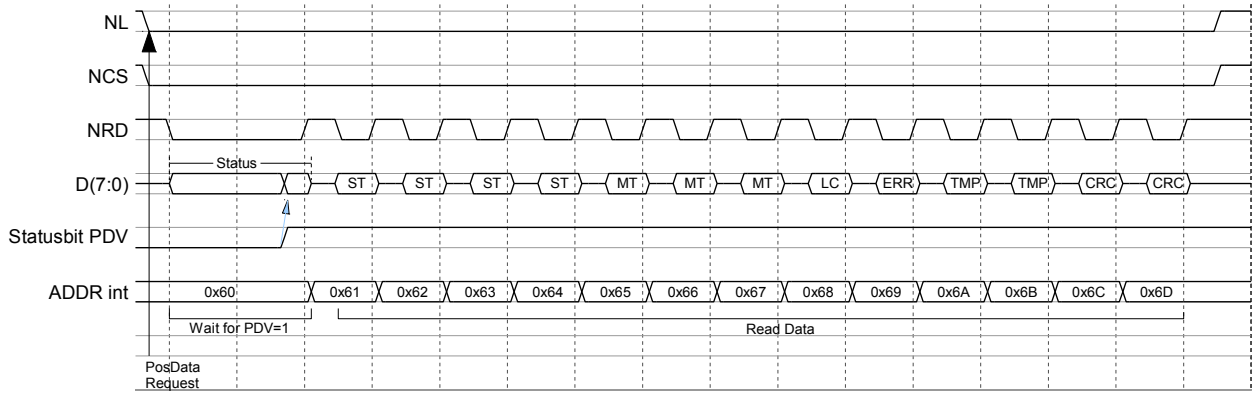


Figure 24: Position data output at request by pin NL

The status register data is output first. During the status register readout NRD should remain low until pin D0 (in this case, PDV) switches to high, as this indicates the validity of the position data.

On each rising edge at NRD the internal address is increased, after which the position data can be read out with each low signal at NRD.

The various ways of outputting position data in this operating mode are set in register FULL_CYC. If bit FULL_CYC is set (Table 57), registers 0x60-0x6D are output on each cyclic access. If this bit is disabled,

registers 0x61 and 0x67 are bypassed; only 24 bits of singleturn and 16 bits of multiturn data are output.

FULL_CYC	Addr. 0x18; bit 5	R/W
Code	Function	
0	24-bit ST / 16-bit MT	
1	26-bit ST / 24-bit MT	

Table 57: Cyclic telegram length

A CRC is formed across the output data *(with the polynomial* $x^{16} + x^{14} + x^{11} + x^{10} + x^9 + x^7 + x^5 + x^3 + x^1 + 1$ *(0x14EAB), start value 0xFFFF)*. The check sum is reformed for each cyclic transmission and is only valid for the duration of this transmission. The following sequence applies to the shortened output format (FULL_CYC = 0):

Data sequence shortened format (FULL_CYC = 0)			
Byte No.	Data	Register	Address
1	Status byte	STAT(7:0)	0x60
2	Singleturn Lo byte	ST(9:2)	0x62
3	Singleturn Mid byte	ST(17:10)	0x63
4	Singleturn Hi byte	ST(25:18)	0x64
5	Multiturn Lo byte	MT(7:0)	0x65
6	Multiturn Mid byte	MT(15:8)	0x66
7	Life counter	LC(7:0)	0x68
8	Error byte	ERR(7:0)	0x69
9	Temperature Lo byte	TEMP(7:0)	0x6A
10	Temperature Hi byte	TEMP(15:8)	0x6B
11	CRC Lo byte	CRC(7:0)	0x6C
12	CRC Hi byte	CRC(15:8)	0x6D

Table 58: Data sequence shortened output format

If more bytes are read out in cyclic operation, a zero is always output. In full output format (FULL_CYC = 1) the data is output in the following order:

Data sequence complete format (FULL_CYC = 1)			
Byte No.	Data	Register	Address
1	Status byte	STAT(7:0)	0x60
2	Singleturn Ext byte	ST(1:0)	0x61
3	Singleturn Lo byte	ST(9:2)	0x62
4	Singleturn Mid byte	ST(17:10)	0x63
5	Singleturn Hi byte	ST(25:18)	0x64
6	Multiturn Lo byte	MT(7:0)	0x65
7	Multiturn Mid byte	MT(15:8)	0x66
8	Multiturn Hi byte	MT(23:16)	0x67
9	Life counter	LC(7:0)	0x68
10	Error byte	ERR(7:0)	0x69
11	Temperature Lo byte	TEMP(7:0)	0x6A
12	Temperature Hi byte	TEMP(15:8)	0x6B
13	CRC Lo byte	CRC(7:0)	0x6C
14	CRC Hi byte	CRC(15:8)	0x6D

Table 59: Data sequence complete output format

SERIAL I/O INTERFACE: BiSS C

The serial I/O interface operates in BiSS C protocol and allows sensor data to be transmitted in repeated and uninterrupted cycles (data channel SCD1, and optional SCD2). Simultaneously, parameters can be exchanged through bidirectional register communication (data channel CD).

Depending on the configuration, the sensor data output by iC-MR contains the cycle counter and interpolation data of up to 50 bits, two error bits, a life counter of 6 bits, and 6 or 16 CRC bits. Another SCD channel can be linked in to transmit the temperature data from the 12-bit A/D converter at a length of 16 bits. BiSS device data (registers PROFILE and DEV_ID) can be programmed separately for both single-cycle data channels.

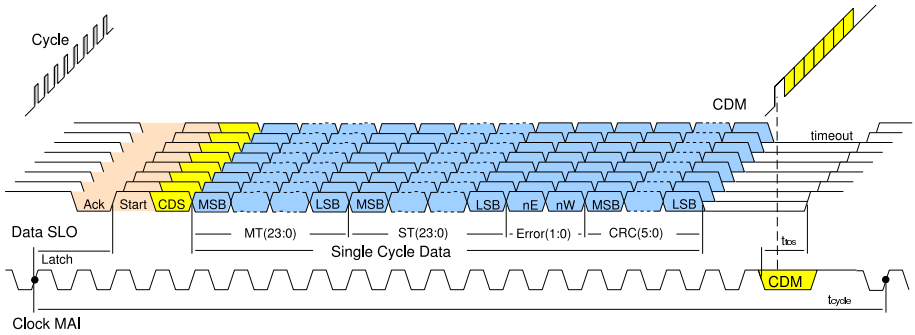


Figure 25: Example of line signals (BiSS C)

BiSS Slave Performance		
Parameter	Symbol	Description
Clock Rate	t_C	10 MHz max.
Process.T.	t_{busy}	typ. 2 µs
Timeout	t_{out}	adaptive (typ. 0.35 µs @ 10 MHz)
Inp. Buffer		15 bit max. for SLI data buffering
SCD Channel 1: Position Data		
Bit/cycle	ID	Description
0 (12) (24)	MT	Multiturn Data
24 (26)	ST	Singleturn Data
1	nE	Error bit ERR (low active transmission)
1	nW	Warning bit WARN (low active transmission)
(6)	LC	Life Counter
6 (16)	CRC	Polynomial 0x43 (0x190D9), adjustable start value (bit inverted transmission)
SCD Channel 2: Temperature Data		
Bit/cycle	ID	Description
16	TEMP	Temperature Data
5	CRC	Polynomial 0x25, start value zero (bit inverted transmission)
Control Data Channel		
Bit/cycle	ID	Description
1	CD	Full support of bidirectional register access and selected commands

Table 60: BiSS slave performance

Configuration

The following parameters define the serial I/O interface in BiSS C protocol:

NESSI	Addr 0x19, bit 4	
Code	Protocol	Information
0 1	SSI BiSS C	BiSS INTERFACE www.biss-interface.com

Table 61: BiSS/SSI protocol selection

ENLC	Addr. 0x19; bit 5	R/W
Code	Function	
0	Life counter disabled	
1	Output of 6-bit life counter	

Table 62: Life counter enable

ENLC enables the life counter to be transmitted on the single-cycle data channel. The counter data is sent directly after the nE and nW bit.

ENXCRC selects the CRC polynomial used and the number of CRC bits transmitted. Here, CRCS allows a free start value to be programmed for CRC calculation. If the 6-bit CRC is chosen, only CRCS bits 5 to 0 are applied.

ENXCRC	Addr. 0x19; bit 3	R/W
Code	Function	
0	6-bit CRC with polynomial 0x43 = $x^6 + x^1 + 1$	
1	16-bit CRC with polynomial 0x190D9 = $x^{16} + x^{15} + x^{12} + x^7 + x^6 + x^4 + x^3 + 1$	

Table 63: CRC polynomial

CRCS(15:8) **CRCS(7:0)**	Addr. 0x28; bit 7...0 Addr. 0x29; bit 7...0	R/W
Code	Function	
0x00 ... 0xFF	Start value for CRC calculation	
Note	For ENXCRC = '0' only CRCS(5:0) is applied.	

Table 64: CRC start value

TMPSCD	Addr. 0x19; bit 2	R/W
Code	Function	
0	Temperature data disabled	
1	SCD Channel 2 enabled for output of temperature data with 5-bit CRC (polynomial 0x25 = $x^5 + x^2 + 1$; start value 0x00)	

Table 65: Temperature data enable

If enabled by TMPSCD, temperature data is transmitted in an additional single-cycle data channel.

The timeout is always formed adaptively and thus does not require configuration.

Register communication

According to the BiSS C protocol, slave registers are directly addressed in a reserved address area (0x40 to 0x7F). Other memory areas are addressed dynamically and in blocks. For this purpose BiSS addresses 0x00 to 0x3F aim at a register block of 64 bytes, whose physical storage address is determined by bank selection n. iC-MR supports up to 32 memory banks, enabling a 16-kbit EEPROM to be fully exploited. This means that there is sufficient storage space for an ID plate (EDS) and OEM data.

Page 43 provides information on memory allocation and addressing through BiSS.

Note: If the internal data bus is busy (due to CRC verification, configuration being written to the EEPROM, or absolute data being read through the ADI, for example), the BiSS C single-cycle data channel returns only zeroes (i.e. the error bit is active).

BiSS Commands

The following BiSS interface commands are implemented. These commands cannot be listed in the broadcast.

BiSS CMD	Function
10	Readout new data via absolute data interface
11	CRC verification of internal configuration

Table 66: BiSS commands

Configuration examples

Singleturn data		
Bits	ID	Description
24	ST	Singleturn value ST(23:0)
2	nE, nW	Error nE and warning nW
6	CRC	Polynomial 0x43
Config.	NESSI = 1, ENLC = 0, TMPSCD = 0, ENXCRC = 0, STRESO = 0x02, MTRESO = 0x7	

Table 67: Format example 1 for BiSS profile BP1

Single- and multiturn data		
Bits	ID	Description
24	MT	Multiturn value MT(23:0)
24	ST	Singleturn value ST(11:0) & x"000"
2	nE, nW	Error nE and warning nW
6	CRC	Polynomial 0x43
Config.	NESSI = 1, ENLC = 0, TMPSCD = 0, ENXCRC = 0, STRESO = 0x0E, MTRESO = 0x0	

Table 68: Format example 2 for BiSS profile BP1

Single- and multiturn data with life counter		
Bits	ID	Description
12	MT	Multiturn value MT(11:0)
26	ST	Singleturn value ST(25:0)
2	nE, nW	Error nE and warning nW
6	LC	Life counter LC
16	CRC	Polynomial 0x190D9
Temperature data		
16	TEMP	Temperature value TEMP(15:0)
5	CRC	Polynomial 0x25
Config.	NESSI = 1, ENLC = 1, TMPSCD = 1, ENXCRC = 1, STRESO = 0x00, MTRESO = 0x3	

Table 69: Format example 3

SERIAL I/O INTERFACE: SSI

iC-MR can transmit position data in SSI protocol, for which purpose the following parameters give the necessary settings and options. In addition, register accesses in write form are possible in SSI mode. As in BiSS mode, the timeout is formed adaptively and thus does not require configuration.

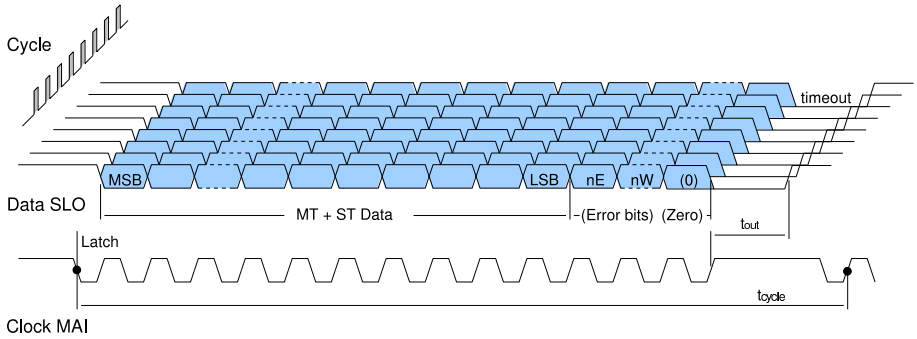


Figure 26: Example of line signals (SSI)

SSI Slave Performance		
Parameter	Symbol	Description
Clock Rate	t_C	4 MHz max.
Timeout	t_{out}	adaptive (typ. 1.7 µs @ 1 MHz)
13-bit Standard SSI		
Bit/cycle	ID	Description
13	ST	Singleturn Data
(1)	nE	Error bit ERR (low active transmission)
25-bit Standard SSI		
Bit/cycle	ID	Description
12	MT	Multiturn Data
13	ST	Singleturn Data
(1)	nE	Error bit ERR (low active transmission)
Extended SSI		
Bit/cycle	ID	Description
0 (12) (24)	MT	Multiturn Data
24 (26)	ST	Singleturn Data
1	nE	Error bit ERR (low active transmission)
1	nW	Warning bit WARN (low active transm.)
(6)	LC	Life Counter
6 (16)	CRC	Polynomial 0x43 (0x190D9), adjustable start value (bit inverted transmission)
(16)	TEMP	Temperature Data
(5)	CRC	Polynomial 0x25, start value zero (bit inverted transmission)

Table 70: SSI slave performance

In 13-bit or 25-bit SSI mode the error bit can be attached to the data by SSIERR.

SSI ring mode can be activated by SSIRING.

NESSI	Addr 0x19, bit 4	
Code	Protocol	Information
0 1	SSI BiSS C	BiSS INTERFACE www.biss-interface.com

Table 71: BiSS/SSI protocol selection

SSIRING	Addr. 0x18; bit 1	R/W
Code	Function	
0	SSI ring mode deactivated	
1	SSI ring mode activated	
SSIERR	Addr. 0x18; bit 0	R/W
0	Standard SSI output without error bit	
1	Standard SSI output with error bit	
SSIMODE	Addr. 0x19; bit 1...0	R/W
00	13-bit SSI protocol	
01	25-bit SSI protocol	
10	Extended SSI protocol (from 8...95 bit)	

Table 72: SSI Configuration

Configuration

SSIMODE(1:0) sets the data length of the serial I/O interface in SSI protocol. Possible values are a 13-bit SSI, a 25-bit SSI, or an extended mode with data contents as described for the BiSS C protocol.

Configuration examples

Singleturn data		
Bits	ID	Description
13	ST	Singleturn value ST(23:11)
Config.	NESSI = 0, ENLC = 0, TMPSCD = 0, ENXCRC = 0, SSIERR = 0, SSIMODE = 00, STRESO = 0x0D, MTRESO = 0x7	

Table 73: Format example 1 for 13-bit SSI

Single- and multiturn data		
Bits	ID	Description
12	MT	Multiturn value MT(11:0)
13	ST	Singleturn value ST(23:11)
1	nE	Error nE
Config.	NESSI = 0, ENLC = 0, TMPSCD = 0, ENXCRC = 0, SSIERR = 1, SSIMODE = 01, STRESO = 0x0D, MTRESO = 0x3	

Table 74: Format example 2 for 25-bit SSI

Single- and multiturn data with life counter		
Bits	ID	Description
24	MT	Multiturn value MT(23:0)
26	ST	Singleturn value ST(25:0)
2	nE, nW	Error nE and warning nW
6	LC	Life counter
16	CRC	Polynomial 0x190D9
Temperature data		
16	TEMP	Temperature value TEMP(15:0)
5	CRC	Polynomial 0x25
Config.	NESSI = 0, ENLC = 1, TMPSCD = 1, ENXCRC = 1, SSIERR = 0, SSIMODE = 10, STRESO = 0x00, MTRESO = 0x0	

Table 75: Format example 3 for extended SSI

SERIAL I/O INTERFACE: SPI

If SPI is selected for the serial I/O interface, iC-MR operates as an SPI slave supporting modes 0 and 3 (meaning clock input MAI ('SCLK') can be 0 or 1 during idle time).

Data at input SLI ('MOSI' line) is always accepted with the rising clock edge of MAI ('SCLK'), whereas data output at SLO ('MISO' line) changes with the falling clock edge of MAI ('SCLK').

The idle state of output SLO ('MISO' line) is 0.

Data is sent byte by byte with the MSB (most significant bit) first.

Note: For a parallel SPI bus configuration, an external tri-state buffer must be used because iC-MR drives a '0' at SLO ('MISO' line) during the idle state.

Register access

The access mode is initiated by the very first bit received, the CYC bit, selecting between register access and cyclic readout.

CYC	
Code	Function
0	Register access
1	Cyclic readout

Table 76: SPI access mode

For CYC = 0, register access is initiated which consists of a 3-byte transmission. CYC is followed by a 7-bit address completing the first byte.

The next byte contains the opcode for the transmission: with one bit for register read (RD), one bit for register write (WR), and 4 bit addressing the command register (CMD).

If the internal data bus should be busy, due to an EEPROM readout after reset for instance, all read accesses are answered by the status byte (with bit BUSY set).

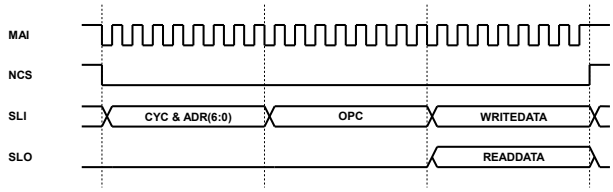


Figure 27: Register access

OPC				
Code				Function
–	RD	WR	CMD	
00	0	0	0000	Request of new position data
00	0	0	0001	Write configuration to EEPROM
00	0	0	0010	Read new data via ADI interface
00	0	0	0011	Trigger software reset
00	0	0	0100	Verify CRC of internal configuration
00	0	0	0101	Error simulation: activate ERR bit
00	0	0	0110	Error simulation: deactivate ERR bit
00	0	1	0000	Register write access
00	1	0	0000	Register read access

Table 77: Transmission opcodes (SPI commands)

The third and final byte concludes the transmission for register access, with which either write data (WRITEDATA) is taken over at pin SLI, or read data (READDATA) is output at pin SLO.

To execute a command which does not require an exchange of data, the transmission can be terminated after the second byte representing the opcode.

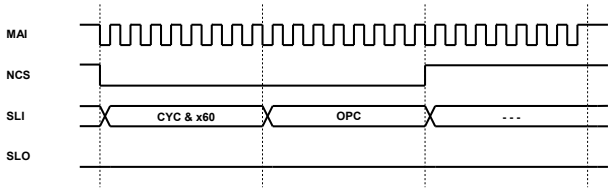


Figure 28: Command access

Cyclic readout

For CYC = 1, cyclic readout is initiated for reading out position data in a sequence covering the address range from 0x60 up to 0x6D (from STATUS to CRC).

In order to generate new position data in advance

- pin NL (assigned to the parallel I/O interface) can be used, or
- the command register must be addressed by opcode 0x00 (prior to the cyclic readout: request for new position data).

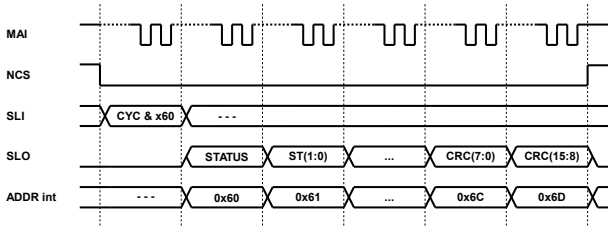


Figure 29: Cyclic readout

A CRC is formed across the output data *(with the polynomial* $x^{16} + x^{14} + x^{11} + x^{10} + x^9 + x^7 + x^5 + x^3 + x^1 + 1$ *(0x14EAB), start value 0xFFFF)*. The check sum is reformed for each cyclic transmission and is only valid for the duration of this transmission.

EEPROM INTERFACE

iC-MR addresses EEPROMs by an 8 bit register address plus 3 block selection bits as part of the I²C device address. If addressing a memory of 1 kbit or 2 kbit, the block selections bits are zero and thus the I²C device address is 0x50 (for '1010 000' without the R/W bit), respectively 0x0A (for '1010 0000' with the R/W bit on zero).
It is not relevant if the EEPROM's internal page buffer is 8 or 16 bytes.
EEPROMs beyond 16 kbit can not be used as those require a 2 byte addressing.

ATTENTION: EEPROMs which consider block selection bits as don't care should not be used. Check especially 5-pin devices as there are no A2, A1, A0 pins.
Be aware of potential conflicts:
If a user addresses memory beyond the 2 kbit range, iC-MR configuration data will be overwritten.
If further I²C slave devices are operated on the same bus, higher device addresses may be occupied.
iC-MR is not multi-master capable; do not connect another I²C master.

Minimal requirements for serial EEPROM

- 3.3 V to 5 V operation
- Standard I²C, 100 kHz clock
- Min. size 1 kbit, 128x8 (for configuration only)
- Max. size 16 kbit, 8x 256x8
- 11 bit address range max.

Memory Addressing

The address space of iC-MR is divided into three consecutive areas:

- CONF: iC-MR configuration data
- EDS: **E**lectronic **D**ata **S**heet
- USER: User section

The CONF section includes addresses 0x00-0x7F, i.e. memory banks 0 and 1. The length of area EDS can be configured using register CFG_E2P. The USER section comes directly after the EDS area. The allocation thereof is described in Figure 30.

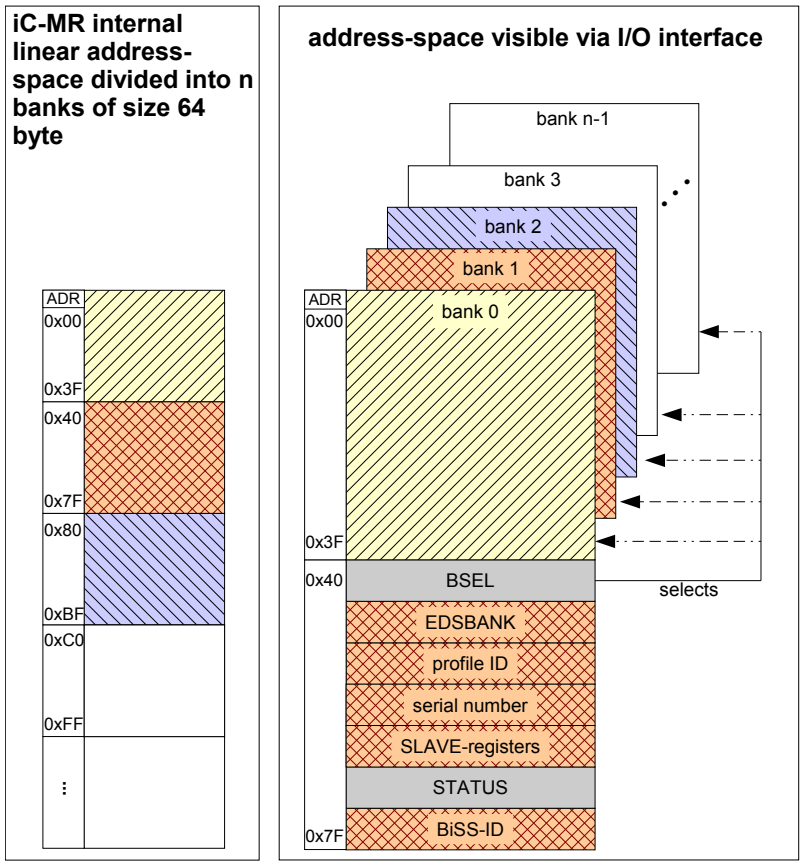


Figure 30: Bankwise memory addressing

Memory areas CONF and EDS are protected by separate write-protection mechanisms (see Safety Features). The memory banks beyond the selected EDS area (USER section) are not write-protected.

CFG_E2P	Addr. 0x26; bit 7...6				R/W
		Banks per range (64 byte each)			
Code	Bytes	CONF	EDS	USER	EEPROM, Type
00	128	2	-	-	1 kbit, as of C01
00	256	2	1	1	2 kbit, as of C02
01	512	2	4	2	4 kbit, as of C04
10	1024	2	12	2	8 kbit, as of C08
11	2048	2	24	6	16 kbit, as of C016

Table 78: EDS range selection

The BSEL register is used to switch to other memory banks on the external EEPROM. After an iC-MR startup bank 0 is selected which mirrors the internal registers. If a different memory bank is selected to provide access to EEPROM data, this is displayed at addresses 0x00-0x3F.

BSEL	Addr. 0x40; bit 4...0	R/W
Code	Bank at addresses 0x00...0x3F	
00000	Bank 0*	
00001	Bank 1	
00010	Bank 2	
...	...	
11111	Bank 31	
Note	*) Corresponds to internal registers	

Table 79: Bank selection

Accessing external memory banks

Register banks 2 to 31 store data in an external EEPROM. If an address is accessed which is not physically present on iC-MR (see Figure 30), communication with the external EEPROM is initiated. If the parallel I/O interface or serial I/O interface is active in SPI mode, the end of I²C communication can be recognized by reading out the status register (address 0x60, bit 2 BUSY). Only after this is it possible to again access the internal registers or external EEPROM registers. When the serial I/O interface is run in BiSS protocol, iC-MR automatically requests the processing time necessary for EEPROM access.

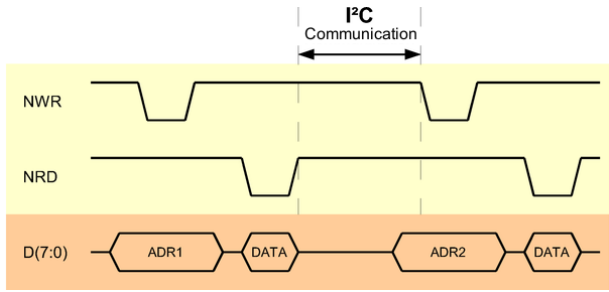


Figure 31: EEPROM read access

Two read accesses are needed to read out data from an address on the EEPROM (for the parallel I/O interface and serial I/O interface in SPI mode only). The first read access initiates communication with the EEPROM; at the end of communication the read data is stored in a temporary register on iC-MR. This temporary register data is supplied on the next read access to an external address. At the same time communication with the EEPROM is again started on this access. This enables a large area to be read out quickly, as the next readout address can already be created to read out the temporary register.

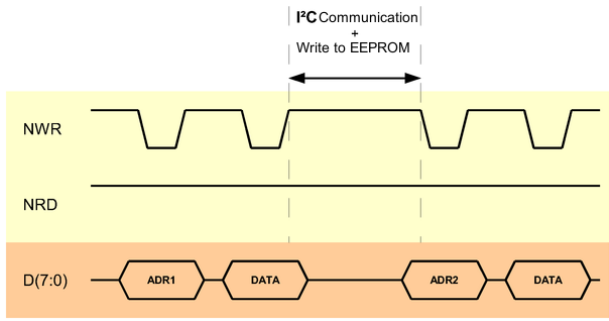


Figure 32: EEPROM write access

Read and write accesses to data in the external EEPROM may only be made if an EEPROM is connected up when iC-MR is started. Autoincrement accesses to external addresses are not possible. Error bit ERR_KNF is updated following each external access (e.g. it is set if the storage time on the EEPROM is undershot, or cancelled if access was successful).

COMMAND AND STATUS REGISTER

Command register

On write access register 0x60 acts as a command register.

CMD	Addr. 0x60; bit 7...0	W
Code	Function	
0x00	Request of new position data	
0x01	Write current configuration to EEPROM	
0x02	Read new data via absolute data interface	
0x03	Trigger software reset	
0x04	Verify CRC of internal configuration	
0x05	Error simulation: activate ERR status	
0x06	Error simulation: delete ERR status	

Table 80: Command register

If command 0x00 is written, new position data is requested. As long as this new data is not available, the PDV (position data valid) bit in the status register shows a zero.

Command 0x01 writes the current configuration to the EEPROM: configuration registers 0x00 up to 0x2D plus **a newly generated check sum** are written. For the duration of this write process the status register indicates BUSY and the error register indicates configuration error ERR_KNF. If an error occurs during writing, error ERR_KNF is not deleted at the end of the process.
If no EEPROM is connected up on startup, commend 0x01 has no effect.

Command 0x02 triggers a new reading of absolute data by the absolute data interface. If the execution is successful, the cycle counter is set (or zeroed if not). In any case, status bit ADV and error bit ERR_ABS will be updated.

Command 0x03 initiates a software reset which is also indicated by a low signal at pin NRES.

Command 0x04 triggers a CRC of the internal configuration, during which all configuration registers are reviewed and verified by the check sum in registers 0x2E-0x2F. During this process the status register indicates BUSY and the error register indicates configuration error ERR_KNF. The error ERR_KNF is only cancelled if the process ends successfully.

Commands 0x05 and 0x06 simulate errors for the ERR bit in the status register, with 0x05 setting the bit and 0x06 deleting it.

Software reset

As if cycling power (undervoltage reset), upon a software reset command the I/O pin NRES indicates a short low pulse (for 3 clock cycles, approx. 200 ns). With the rising edge of NRES iC-MR starts to access the external I^2C-EEPROM to read its CRC protected configuration data (see section Startup with EEPROM, page 33).

If there is no EEPROM, the internal registers are zeroed and the pin state of SDA and SCL is evaluated to select the interface (see section Startup without EEPROM, page 33).

Status register

A read access to register 0x60 returns the current system status.

STATUS	Addr. 0x60; bit 7...0	R
Bit	Status message	
INIT	Configuration completed	
ERR	Error message (as selected by EMASK)	
WARN	Warning message (as selected by WMASK)	
EWKH	Write access permitted to memory area CONF	
EWKL	Write access permitted to memory area EDS	
BUSY	Internal data bus busy	
ADV	Absolute data valid	
PDV	Position data valid	
Logic	1 = true, 0 = false	

Table 81: Status register

INIT indicates that the configuration registers have been successfully CRC veryfied, and that absolute data has been correctly read by the absolute data interface.

ERR and WARN indicate error messages which are selected by the mask registers EMASK and WMASK.

EWKH and EWKL signal an active write protection for memory areas CONF, respectively EDS.

BUSY indicates the internal data bus is busy, such as when data is being read out from or written to the EEPROM.

ADV indicates that absolute data has been loaded successfully through the absolute data interface. If SSI is configured, data is always accepted. If BiSS is configured, data is accepted only if the CRC is correct and the error bit inactive.

PDV signals that the current position data is valid.

Error masking for ERR and WARN status
Registers EMASK and WMASK define which messages of the error register are to be reported to the error bit or warning bit of the status register.

EMASK	Addr. 0x22; bit 7...0
Bit	Message
EM_EXT	System Error
EM_ABS	Absolute Data Error
EM_IPO	Interpolation Error
EM_KNF	Configuration Error
EM_SYN	Synchronization Error
EM_TMP	Temperature Error
EM_AMP	Signal Error
EM_RGL	Control Error
Logic	1 = enabled, 0 = disabled

Table 82: Error masking for status bit ERR

WMASK	Addr. 0x23; bit 7...0
Bit	Message
WM_EXT	System Error
WM_ABS	Absolute Data Error
WM_IPO	Interpolation Error
WM_KNF	Configuration Error
WM_SYN	Synchronization Error
WM_TMP	Temperature Error
WM_AMP	Signal Error
WM_RGL	Control Error
Logic	1 = enabled, 0 = disabled

Table 83: Error masking for status bit WARN

MONITORING AND SAFETY FEATURES

Error register

The error register at address 0x69 signals internal and external errors, whereas most error bits are stored until a reset action.

ERROR	Addr. 0x69; bit 7...0	R
Bit	Error message	
ERR_EXT	**System Error** (latched*) Pin NERR was forced low by the external system.	
ERR_ABS	**Absolute Data Error** - ADI received BiSS data with CRC error - ADI received BiSS data with error bit nE low active Note that this error remains zero if ADI is not configured or if using SSI.	
ERR_IPO	**Interpolation Error** Conversion was not finished at time of read access.	
ERR_KNF	**Configuration Error** This error will be indicated in case of: - startup without EEPROM - CRC error on startup with EEPROM - CRC error after CRC verification on command - temporarily during CRC verification on command - temporarily during write access to EEPROM - the EEPROM is not responding	
ERR_SYN	**Synchronization Error** (latched*) Internal synchronization failure between cycle counter and interpolator.	
ERR_TMP	**Temperature Error** (latched*) The upper or lower temperature monitoring threshold was exceeded.	
ERR_AMP	**Signal Error** (latched*) Or-gated summary of DC_MAX, DC_MIN, CMP_MAX, CMP_MIN	
ERR_RGL	**Control Error** (latched*) Or-gated summary of RG_MAX, RG_MIN, AMP_MAX, AMP_MIN	
Logic	0 = no error, 1 = error is active or latched *) Register reset is required to delete the message.	

Table 84: Error register

RES_ERR selects which action resets the error register. If readout of position data is selected, the error register is reset after each position reading cycle. Alternatively, the error register can be maintained until it is read out by a register read access to address 0x69.

RES_ERR	Addr. 0x27; bit 6	R/W
Code	Function	
0	Reset upon reading out position data	
1	Reset after a read access to the error register	

Table 85: Error register reset action

Diagnosis register

The diagnosis register at address 0x5A further resolves the messages summarized by signal error ERR_AMP and control error ERR_RGL.

DIAG	Addr. 0x5A; bit 7...0	R
Bit	Name	Description
Signal Errors under ERR_AMP		
5	DC_MAX	DC level monitoring: maximum offset (refers to Elec.Char. No. B04)
1	DC_MIN	DC level monitoring: minimum offset (refers to Elec.Char. No. B05)
4	CMP_MAX	AC level monitoring: maximum amplitude (refers to Elec.Char. No. B01)
0	CMP_MIN	AC level monitoring: minimum amplitude (refers to Elec.Char. No. B02)
Control Errors under ERR_RGL		
7	RG_MAX	ACO control error: maximum current (refers to Elec.Char. No. 808)
3	RG_MIN	ACO control error: minimum current (refers to Elec.Char. No. 807)
6	AMP_MAX	Signal level monitoring: maximum amplitude (refers to Elec.Char. No. 810)
2	AMP_MIN	Signal level monitoring: minimum amplitude (refers to Elec.Char. No. 809)
Note: For a description of signal and control error monitoring refer to page 25.		

Table 86: Diagnosis register

Signal error filtering

Error messaging to ERR_AMP can be assigned with a digital filter enabled by EN_FAMP. The filter is implemented as an integrator with an adjustable timeout (TO_FAMP) to reset, respectively restart, the integration time. The filter threshold THR_FAMP determines how long a signal error must be active until it is passed on to the error register.

EN_FAMP	Addr. 0x2B; bit 0	R/W
Code	Function	
0	No filtering	
1	Filtering active on ERR_AMP	

Table 87: Signal error filtering

TO_FAMP	Addr. 0x2B; bit 1	R/W
Code	Function	
0	Reset each 273 µs typ.	
1	Reset each 546 µs typ.	

Table 88: Filter timeout

THR_FAMP	Addr. 0x2B; bit 3...2	R/W
Code	Function	
0x0	approx. 17 µs	
0x1	approx. 34 µs	
0x2	approx. 51 µs	
0x3	approx. 68 µs	

Table 89: Filter threshold

Life counter

The 8-bit life counter register is incremented by one with each request for new position data. Its reset value of zero is never output as it is bypassed during normal operation (counting order 0xFE, 0xFF, 0x01, 0x02 ...).

LC(7:0)	Addr. 0x68; bit 7...0	R
Code	Value	
0x00	Initial value after power-up and reset	
0x01	Value on first request for new position data and follow-up value on the maximum	
...	...	
0x3F	Max. value for BiSS/SSI protocol (limited to 6 bit)	
0xFF	Max. value for parallel and SPI interface	

Table 90: Life counter

Configuration data CRC

If an EEPROM is available, the configuration data and its check sum is read upon power up (for details refer to chapter EEPROM Interface, page 43). The check sum fills register CRCCFG at addresses 0x2E-0x2F and is then used to confirm the contents of the configuration RAM.

If no EEPROM is connected or if the check sum does not match, the configuration RAM is zeroed and must be rewritten including its check sum, followed by a CRC verification on command.

If configuration data is written to the EEPROM on command, the check sum in addresses 0x2E-0x2F is newly calculated and transferred to the EEPROM.

CRCCFG(15:8)	Addr. 0x2E; bit 7...0	R/W
CRCCFG(7:0)	Addr. 0x2F; bit 7...0	
Code	Function	
0x0000	Check sum for address range 0x00 to 0x2D; CRC polynomial 0x1021 $x^{16} + x^{12} + x^5 + 1$ (CRC-16)	
...	start value 0x0000	
0xFFFF		

Table 91: Configuration data CRC

Example of CRC calculation routine:

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x1021;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 0; // start value !!!
for (iReg = 0; iReg<46; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

Register protection

If safety register SEC_HI does not equal 0x00, the status register shows zero for EWKH and NRDOK defines if write or read/write protection is active for memory area CONF. In the latter case the configuration registers can then be neither read out nor overwritten. On read access 0x00 is output.

Safety register SEC_HI can be reset and protection deleted only if the current register key data is again written.

NRDOK	Addr. 0x25; bit 7	R/W
Code	Function	
0	Write protection for CONF memory	
1	Read and write protection for CONF memory	

Table 92: Read/write protection for CONF memory

SEC_HI	Addr. 0x25; bit 6...0	R/W
Code	Function	
0x00	Register protection disabled	
Otherwise	Register protection according to NRDOK	

Table 93: Safety register for CONF memory

If safety register SEC_LO does not equal 0x00, the status register shows zero for EWKL and write protection is active for memory area EDS. All registers in this area can be read out but not overwritten.

Safety register SEC_LO can be reset and protection deleted only if the current register key data is again written.

SEC_LO	Addr. 0x26; bit 5...0	R/W
Code	Function	
0x00	Register protection disabled	
Otherwise	Write protection for EDS memory	

Table 94: Safety register for EDS memory

DESIGN REVIEW: Notes On Chip Functions

iC-MR Y1		
No.	Function, parameter/code	Description and application notes
1	NEFDR, LCMODE, CHK_ADI	These functions are not available. Mandatory programming of the corresponding register bits is zero.
2	RES_ERR, THR_FAMP, TO_FAMP, EN_FAMP	These functions are not available. Mandatory programming of the corresponding register bits is zero.
3	PROFILE(15:0), Addr 0x48, 0x49	These addresses are not assigned. The recommended programming value is zero.
4	DEV_ID(47:0), Addr 0x72 to 0x77	These addresses are not assigned. The recommended programming value is zero.
5	I/O Interface selection: INTCFG, Addr 0x18	The I/O interface configured by EEPROM can not be altered during operation. Use an external programmer to redefine the EEPROM setup, or remove the EEPROM and wire the SDA/SCL pins to set the desired interface.
6	Signal Monitoring: Elec. Char. B01, B02	Conditions not applicable, values differ.

Table 95: Notes on chip functions regarding iC-MR chip release Y1

iC-MR X		
No.	Function, parameter/code	Description and application notes
1	CYC_ADI, CHK_ADI	CYC_ADI = 1 always initializes the period counting independently of the CHK_ADI setting. Note that if a reading error occurs on the ADI, the period counter will be zeroed (e.g. upon a CRC error, an active error bit (nE), an interrupted data line). Therefore, updating the period counter should be initiated by command: BiSS Opcode 10, or CMD = 0x02.
2	I/O Interface selection: INTCFG, Addr 0x18	If an EEPROM is missing on startup, it can not be accessed after insertion.

Table 96: Notes on chip functions regarding iC-MR chip release X

REVISION HISTORY

Rel	Rel.Date	Chapter	Modification	Page
A1	2013-11-21		Initial release (prelim.)	all

Rel	Rel.Date	Chapter	Modification	Page
B1	2015-4-22	BLOCK DIAGRAM	Update of block diagram to include S&H circuit, change of block name to Signal Monitoring	1
		DESCRIPTION	Correction of SPI clock rate to 10 MHz	2
		ELECTRICAL CHARACTERISTICS	Item 604: name and max value Item B01, B02: update of conditions, typ. values supplemented Item B04, B05: max. values, typ. values supplemented Item N09: conditions and values updated Fig. 1 and 2 moved to chapter Signal Monitoring	6ff
		OPERATING CONDITIONS: Absolute Data Interface (ADI)	Timing description supplemented	11
		OPERATING CONDITIONS: Parallel I/O Interface	Timing figures updated and all items adapted	12
		OPERATING CONDITIONS: Serial I/O Interface	Timing figures for BiSS/SSI and SPI updated, all items adapted	13ff
		CONFIGURATION PARAMETERS	Update of table: name of parameters, new order according to chapters	15
		REGISTER MAP	Corrections in Addr 0x27 and 0x2B	16ff
		SIGNAL CONDITIONING	Table 14, 15, 18, 19, 23: name of parameter	20ff
		SIGNAL MONITORING	New chapter supplemented	25
		INTERPOLATION AND CYCLE COUNTING	New subtitles, description of MT and ST data length updated Table 39, 43, 44: update of contents	28ff
		ABSOLUTE DATA INTERFACE (ADI)	Chapter reworked: Fig. 19+20 supplemented for BiSS and SSI data frames, headlines supplemented, description added for occupied ADI interface Tab. 48, 49, 50, 51: update of description	31
		STARTUP and I/O INTERFACE SELECTION	New chapter supplemented; description of INTCFG taken over from chapter EEPROM interface	33
		SERIAL I/O INTERFACE: BiSS C, SSI	Chapters reworked: Tab. 63: name of parameter, Tab. 60 and 70 added	37ff
		SERIAL I/O INTERFACE: SPI	Chapter reworked; update of Figures	41ff
		EEPROM INTERFACE	Update of description: new section on EEPROM selection	43
		COMMAND AND STATUS REGISTER	Chapter reworked, contents separated	45ff
		MONITORING and SAFETY FEATURES	Chapter reworked, subtitles supplemented, Tab. 84 and 86: updated contents, Tab. 90 supplemented for life counter	47ff
		DESIGN REVIEW: Application notes	Item 5 and 6 added for iC-MR Y1, iC-MR X supplemented	49

ORDERING INFORMATION

Type	Package	Order Designation
iC-MR Evaluation Board	48-pin QFN 7x7 mm	iC-MR QFN48 iC-MR EVAL MR1D

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