iC-MFP

8-FOLD FAIL-SAFE P-FET DRIVER

target specification

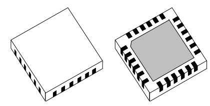
FEATURES

- 8-fold level shift up to 40 V output voltage
- Inputs compatible with TTL and CMOS levels, 40 V voltage proof
- Voltage swing configurable to 5 V, 10 V or supply voltage
- Short-circuit-proof push-pull current sources for driving FETs slowly
- Safe high output state with single errors
- Ground and supply voltage monitor
- Status output for error and system diagnostics
- Temperature range from -40 to 125 °C
- Protective ESD circuitry

APPLICATIONS

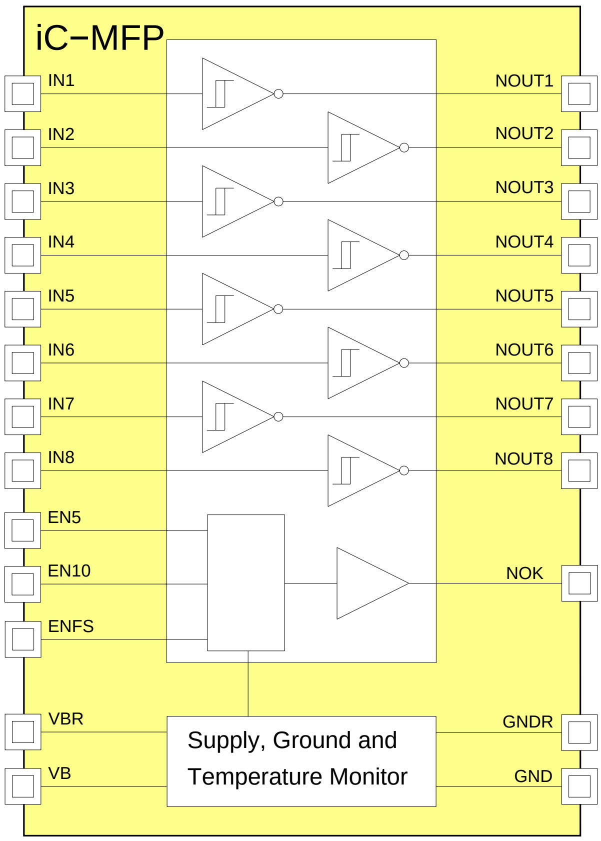
- Operation of P-FETs from 1.8 V, 2.5 V, 3.3 V or 5 V systems

PACKAGES



QFN24

BLOCK DIAGRAM



DESCRIPTION

iC-MFP is a monolithically integrated, 8-channel inverting level adjustment device which drives P-channel FETs. The internal circuit blocks have been designed in such a way that with single errors, such as open pins (VB, VBR, GND, GNDR) or the short-circuiting of two outputs, iC-MFP's output stages switch to a predefined, safe high state. Externally connected P-channel FET are thus shut down safely in the event of a single error.

The inputs of the eight channels consist of a Schmitt trigger with a pull-down current source and are compatible with TTL and CMOS levels and are voltage-proof up to 40 V. The eight channels have a current-limited push-pull output stage and a pull-up resistor at the output. The hi-level at one of the inputs EN5, EN10 or ENFS defines the output lo-level VB - 5 V, VB - 10 V or GND voltage and enables the outputs. The output lo-level is disabled with the lo-level at all inputs EN5, EN10 and ENFS or with the hi-level at more than one input.

iC-MFP monitors the supply voltage at VB and VBR pin and the voltages at the two ground pins GND and GNDR. Both power supply pins VB and VBR and both pins GND and GNDR must be connected together externally in order to guarantee the safe high state of the output stages in the event of error.

Should the supply voltage at VB undershoot a predefined threshold, the voltage monitor causes the outputs to be actively tied to VB via the highside transistors. If the supply voltage ceases to be applied to VB, the outputs are tied to VBR by pull-up resistors.

If the connection between the ground potential and the GND or GNDR pin is disrupted, the highside transistors are activated.

Pull-down currents provide the safe lo-level at open inputs IN1...8, EN5, EN10 and ENFS. The pull-down currents have two stages in order to minimize power dissipation with enhanced noise immunity.

When two outputs of different logic states are short circuited, the driving capability of the highside driver predominates, keeping the connected P-channel FETs in a safe shutdown state.

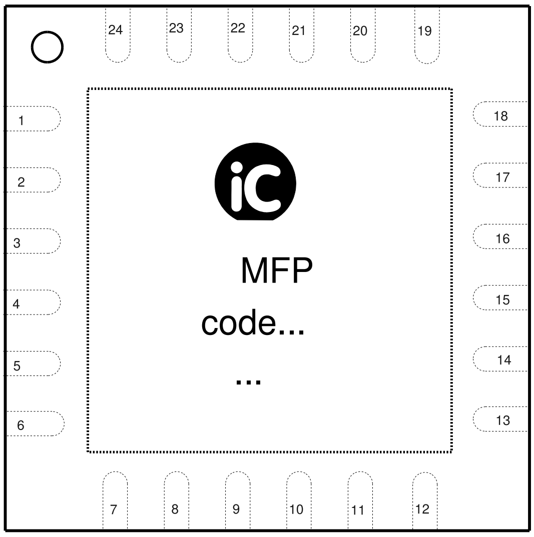
The status of the device is indicated with the Open-Drain pin NOK and can be used for system diagnostics.

Temperature monitoring protects the device from too high power dissipation.

The device is protected against destruction by ESD.

PACKAGES QFN24 4 mm x 4 mm to JEDEC

PIN CONFIGURATION QFN24
(top view)



PIN FUNCTIONS

No.	Name	Function
1	NOUT1	Output channel 1
2	VB	Supply Voltage
3	VBR	Supply Voltage (R)
4	EN5	Enable input lo-level = VB-5V
5	EN10	Enable input lo-level = VB-10V
6	IN1	Input channel 1
7	IN2	Input channel 2
8	IN3	Input channel 3
9	IN4	Input channel 4
10	IN5	Input channel 5
11	IN6	Input channel 6
12	IN7	Input channel 7
13	IN8	Input channel 8
14	NOK	Output inverted status
15	ENFS	Enable input full scale lo-level = GND
16	GNDR	Ground (R)
17	GND	Ground
18	NOUT8	Output channel 8
19	NOUT7	Output channel 7
20	NOUT6	Output channel 6
21	NOUT5	Output channel 5
22	NOUT4	Output channel 4
23	NOUT3	Output channel 3
24	NOUT2	Output channel 2
	TP	Thermal-Pad

The *Thermal Pad* is to be connected to a ground plane on the PCB. Connections between GND, GNDR and the ground plane should be conciled to system FMEA aspects.

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VB, VBR	Supply Voltage		-0.3	40	V
G002	V()	Voltage at NOUT1...8, NOK		-0.3	40	V
G003	V()	Voltage at IN1...8, EN5, EN10, ENFS		-0.3	40	V
G004	V(GNDR)	Voltage at GNDR referenced to GND		-0.3	0.3	V
G005	V(GND)	Voltage at GND referenced to GNDR		-0.3	0.3	V
G006	V(VBR)	Voltage at VBR referenced to VB		-0.3	0.3	V
G007	V(VB)	Voltage at VB referenced to VBR		-0.3	0.3	V
G008	Imx()	Current in NOUT1...8, NOK, IN1...8, EN5, EN10, ENFS		-10	10	mA
G009	Imx()	Current in VB, VBR		-10	80	mA
G010	Imx()	Current in GND, GNDR		-80	10	mA
G011	Vd()	ESD susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G012	Tj	Operating Junction Temperature		-40	140	°C
G013	Ts	Storage Temperature Range		-55	125	°C

THERMAL DATA

Operating Conditions: VB = VBR = 4.5. . . 40 V, GND = GNDR = 0 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip/Ambient	SMD assembly, no additional cooling areas.			75	K/W

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = VBR = 4.5...40 V, GND = GNDR = 0 V, Tj = -40...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VB	Permissible Supply Voltage				4.5		40	V
002	I(VB)	Supply Current in VB	No load, EN5 = lo, EN10 = lo, ENFS = lo			1.2		3.6	mA
003	I(VB)	Supply Current in VB	No load, EN5 = hi, EN10 = lo, ENFS = lo, IN1...8 = hi, VB = 8...40 V			3.2		6.6	mA
004	I(VB)	Supply Current in VB	No load, EN5 = lo, EN10 = hi, ENFS = lo, IN1...8 = hi, VB = 13...40 V			3.2		6.8	mA
005	I(VB)	Supply Current in VB	No load, EN5 = lo, EN10 = lo, ENFS = hi, IN1...8 = hi, VB = 4.5...40 V			1.3		6.6	mA
006	I(VBR)	Supply Current in VBR	No load, all NOUTx = lo				tbd		mA
007	I(GND)	Current in GND	No load			-7			mA
008	I(GNDR)	Current in GNDR	No load				tbd		mA
Current Driver NOUT1...8									
101	Vc()hi	Clamp Voltage hi	I() = 10 mA			42		60	V
102	Vc()lo	Clamp Voltage lo referenced to the lower voltage of GND, GNDR	I() = -10 mA			-2		-0.4	V
103	Vs()hi	Saturation Voltage hi referenced to VB	Vs()hi = VB – V(); I() = -0.5 mA I() = -2 mA					 0.2 0.8	 V V
104	Vs()lo	Saturation Voltage lo referenced to GND	ENFS = hi, INx = hi; I() = 0.5 mA I() = 2 mA					0.2 0.8	V V
105	Vr()	Output Voltage regulated, no load	Vr() = V() – VB, EN5 = hi, INx = hi, I() = 0 mA			-5.3	-5	-4.7	V
106	Vr()	Output Voltage regulated, no load	Vr() = V() – VB, EN10 = hi, INx = hi, I() = 0 mA			-10.6	-10	-9.4	V
107	Ri()	Output Resistance	EN10 = hi or EN5 = hi, INx = hi, I() = $\pm$ 2 mA			80		300	Ω
108	Vl(NOUTx)	Output Voltage	I(NOUTX)= -2 µA, Vl() = VBR – V(), VB open					600	mV
109	Ipu()	Pull-Up Current	VBR-V(NOUTx) = 1 V, VB open			-10		-3	µA
110	Rpu()	Pull-Up Resistor at NOUTx referenced to VBR	VBR-V(NOUTX) = 10 V, VB open			140	200	300	kΩ
111	Rpu()	Pull-Up Resistor at NOUTx referenced to VBR	VBR-V(NOUTX) = 40 V, VB open			200	400	600	kΩ
112	Isc()lo	Short circuit current lo	V() = 0.8 V...VB			2	3	10	mA
113	Isc()hi	Short circuit current hi	V() = 0...VB – 0.8 V			-10	-3.6	-2	mA
114	Vsh()	Output Voltage at short circuit of two outputs	Vsh() = V() – VB; EN5 = hi At two different input signals hi and lo			-1			V
115	Vsh()	Output Voltage at short circuit of two outputs	Vsh() = V() – VB; EN10 = hi or ENFS = hi At two different input signals hi and lo			-1.3			V
116	Vt()hi	Threshold Voltage hi monitoring comparator	Vt() = Vr() + VB – V() or Vt() = V()					2.2	V
117	Vt()lo	Threshold Voltage lo monitoring comparator	Vt() = Vr() + VB – V() or Vt() = V()			0.8			V
118	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo			50		300	mV

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = VBR = 4.5. . . 40 V, GND = GNDR = 0 V, Tj = -40...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Input IN1...8, EN5, EN10, ENFS									
201	Vc()hi	Clamp Voltage hi	I() = 10 mA			42		60	V
202	Vc()lo	Clamp Voltage lo referenced to the lower voltage of GND, GNDR	I() = -10 mA			-2		-0.4	V
203	Vt()hi	Threshold Voltage hi				1.15		1.4	V
204	Vt()lo	Threshold Voltage lo				0.8		1.05	V
205	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo			200		400	mV
206	Ipd1()	Pull-Down Current 1	0.4 V < V() < Vt()hi		5	75	225	350	µA
207	Ipd2()	Pull-Down Current 2	V() > 1.4 V		5	20	45	70	µA
208	Cin()	Input Capacitance						20	pF
209	Il()	Leakage Current	VB, VBR = 0 V, V() = 0..40 V			-10		10	µA
Supply and Temperature Monitor									
301	VBon	Turn-On Threshold VB				3.8		4.3	V
302	VBoff	Turn-Off Threshold VB	Decreasing voltage VB			3.4		4.0	V
303	VBhys	Hysteresis	VBhys = VBon – VBoff			200			mV
304	Toff	Turn-Off Temperature	Increasing temperature			145	160	180	°C
305	Ton	Turn-On temperature	Decreasing temperature			130	147	170	°C
306	Thys	Hysteresis	Thys = Toff – Ton				13		°C
Ground Monitor GND, GNDR									
401	Vt()hi	Threshold Voltage hi GND Monitor	Referenced to GNDR					270	mV
402	Vt()lo	Threshold Voltage hi GND Monitor	Referenced to GNDR			50			mV
403	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo			5		100	mV
404	Vt()hi	Threshold Voltage hi GNDR Monitor	Referenced to GND					270	mV
405	Vt()lo	Threshold Voltage lo GNDR Monitor	Referenced to GND			50			mV
406	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo			10		100	mV
407	Vc()hi	Clamp Voltage GNDR hi referenced to GND	I() = 1 mA			0.4		2	V
408	Vc()lo	Clamp Voltage GNDR lo referenced to GND	I() = -1 mA			-2		-0.4	V
Status Output NOK									
501	Vc(NOK)hi	Clamp Voltage hi	I() = 10 mA			42		60	V
502	Vc(NOK)lo	Clamp Voltage lo referenced to the lower voltage of GND, GNDR	I() = -10 mA			-2		-0.4	V
503	Il(NOK)	Leakage Current	GND < V(NOK) < VB			-20		20	µA
504	Vs(NOK)lo	Saturation Voltage lo referenced to GND	I() = 0.5 mA I() = 2 mA					0.2 0.8	V V
505	Isc(NOK)lo	Short circuit current lo	V() = 0.8 V...VB			2	3	10	mA
Supply Monitor VB, VBR									
601	Vt(VB)hi	Threshold Voltage hi VB Monitor	Referenced to VBR					270	mV
602	Vt(VB)lo	Threshold Voltage lo VB Monitor	Referenced to VBR			50			mV
603	Vt(VB)hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo			5		100	mV
604	Vt(VBR)hi	Threshold Voltage hi VBR Monitor	Referenced to VB					270	mV
605	Vt(VBR)lo	Threshold Voltage lo VBR Monitor	Referenced to VB			50			
606	Vt(VBR)hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo			5		100	mV
607	Vc(VBR)hi	Clamp Voltage hi	I() = 1 mA, Vc() = V(VBR) - V(VB)			0.4		2	V
608	Vc(VBR)lo	Clamp Voltage lo	I() = -1 mA, Vc() = V(VBR) - V(VB)			-2		-0.4	

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = VBR = 4.5. . . 40 V, GND = GNDR = 0 V, Tj = -40...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Testmode EN5, EN10, ENFS									
701	Vt()hi	Threshold Voltage hi disable test	EN5 = EN10 = ENFS					-60	mV
702	Vt()lo	Threshold Voltage lo enable test	EN5 = EN10 = ENFS			-320			mV
703	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo			50		160	mV
Regulator lo-level									
801	Vt(VB)hi	Threshold Voltage hi enable regulator	EN5 = hi			5.5		6.2	V
802	Vt(VB)lo	Threshold Voltage lo disable regulator	EN5 = hi			5.3		6	V
803	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo			100		300	mV
804	Vt(VB)hi	Threshold Voltage hi enable regulator	EN10 = hi			10.6		11.7	V
805	Vt(VB)lo	Threshold Voltage lo disable regulator	EN10 = hi			10.3		11.3	V
806	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo			200		600	mV
Timing									
901	tp(NOUTx)	Propagation delay INx, EN5 → NOUTx	({IN, EN5}lo → hi) → 10 %NOUT ({IN, EN5}hi → lo) → 90 %NOUT CLoad() = 100 pF		1	0.45		1.1	µs
902	tp(NOUTx)	Propagation delay INx, EN5 → NOUTx	({IN, EN5}lo → hi) → 10 %NOUT ({IN, EN5}hi → lo) → 90 %NOUT CLoad() = 1 nF		1	1.3		2.4	µs
903	tp(NOUTx)	Propagation delay INx, EN5 → NOUTx	({IN, EN5}lo → hi) → 10 %NOUT ({IN, EN5}hi → lo) → 90 %NOUT CLoad() = 2 nF		1	2.2		3.7	µs
904	tp(NOUTx)	Propagation delay INx, EN5 → NOUTx	({IN, EN5}lo → hi) → 10 %NOUT ({IN, EN5}hi → lo) → 90 %NOUT CLoad() = 5 nF		1	5		8.1	µs
905	tp(NOUTx)	Propagation delay INx, EN10 → NOUTx	({IN, EN10}lo → hi) → 10 %NOUT ({IN, EN10}hi → lo) → 90 %NOUT CLoad() = 100 pF		1	0.7		1.6	µs
906	tp(NOUTx)	Propagation delay INx, EN10 → NOUTx	({IN, EN10}lo → hi) → 10 %NOUT ({IN, EN10}hi → lo) → 90 %NOUT CLoad() = 1 nF		1	2.3		4.1	µs
907	tp(NOUTx)	Propagation delay INx, EN10 → NOUTx	({IN, EN10}lo → hi) → 10 %NOUT ({IN, EN10}hi → lo) → 90 %NOUT CLoad() = 2 nF		1	3.9		7.1	µs
908	tp(NOUTx)	Propagation delay INx, EN10 → NOUTx	({IN, EN10}lo → hi) → 10 %NOUT ({IN, EN10}hi → lo) → 90 %NOUT CLoad() = 5 nF		1	9		16	µs
909	tp(NOUTx)	Propagation delay INx, ENFS → NOUTx	({IN, ENFS}lo → hi) → 10 %NOUT ({IN, ENFS}hi → lo) → 90 %NOUT CLoad() = 100 pF		1	1.4		3.1	µs
910	tp(NOUTx)	Propagation delay INx, ENFS → NOUTx	({IN, ENFS}lo → hi) → 10 %NOUT ({IN, ENFS}hi → lo) → 90 %NOUT CLoad() = 1 nF		1	5.2		9.8	µs
911	tp(NOUTx)	Propagation delay INx, ENFS → NOUTx	({IN, ENFS}lo → hi) → 10 %NOUT ({IN, ENFS}hi → lo) → 90 %NOUT CLoad() = 2 nF		1	9.2		16.7	µs
912	tp(NOUTx)	Propagation delay INx, ENFS → NOUTx	({IN, ENFS}lo → hi) → 10 %NOUT ({IN, ENFS}hi → lo) → 90 %NOUT CLoad() = 5 nF		1	20		35	µs
913	dV()/dt	Slew rate	VB = 24 V, CLoad() = 100 pF			7		18	V/µs
914	dV()/dt	Slew rate	VB = 24 V, CLoad() = 1 nF			2.2		4.5	V/µs
915	dV()/dt	Slew rate	VB = 24 V, CLoad() = 2 nF			1.2		2.5	V/µs
916	dV()/dt	Slew rate	VB = 24 V, CLoad() = 5 nF			0.5		1.2	V/µs

ELECTRICAL CHARACTERISTICS: Diagrams

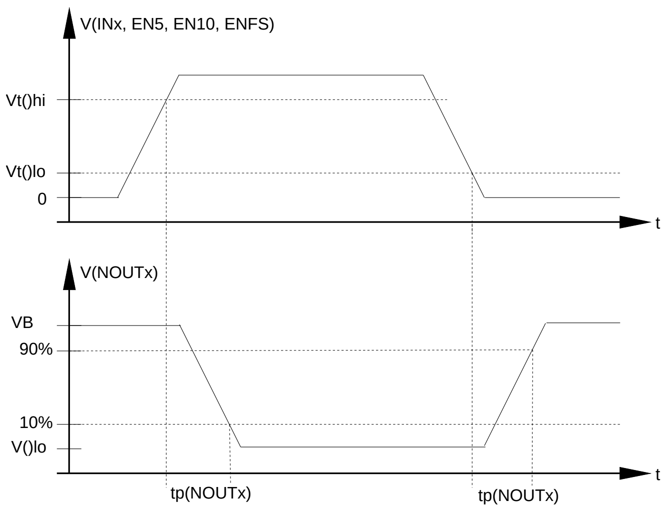


Figure 1: Propagation delays

DESCRIPTION OF FUNCTIONS

Lo-level output configuration

The device iC-MFP has three adjustable lo-levels for driving P-channel fets. The configured lo-level is common to all outputs NOUTx and the minimum level is GND potential. The lo-level configuration inputs are used simultaneous for enabling the lo-level at the outputs NOUTx. The hi-level at exactly one input EN5, EN10 or ENFS configure the voltage of lo-level and enable the outputs. If more than one of these inputs have hi-level the outputs remains disabled. The lo-level VB - 5 V (configured with EN5 = hi) and VB - 10 V (configured with EN10 = hi) are internally generated by a voltage reference and regulated. The lo-level GND (configured with ENFS = hi) is an unregulated connection to GND. In this case the voltage swing depends directly from the power supply VB.

Output characteristics of the highside transistor

The highside output transistors at the eight channels demonstrate a resistive behavior with low voltage (VB – V(NOUTx)) and behave as a current source with finite output resistance with higher voltages.

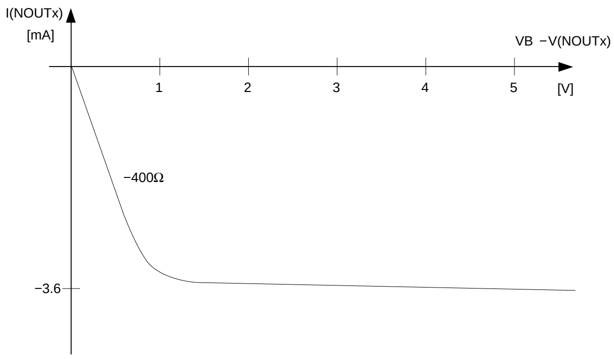


Figure 2: Output characteristic of the highside transistor at NOUTx

Output characteristic of the regulated push-pull-output at NOUTx

The lo-level VB - 5 V and VB - 10 V is generated with a regulatetd push-pull output and demonstrate a resistive behavior with low voltage changes and behave as a current source with finite output resistance with higher voltage changes.

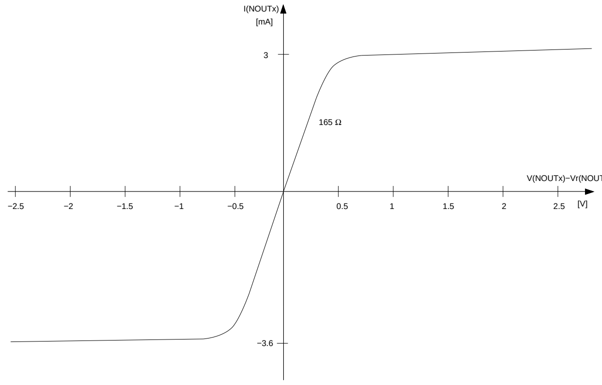


Figure 3: Output characteristic of the regulated push-pull-output at NOUTx

Output characteristic of the lowside transistor

The lowside output transistors at the eight channels demonstrate a resistive behavior with low voltage V(NOUTx) and behave as a current sink with finite output resistance with higher voltages.

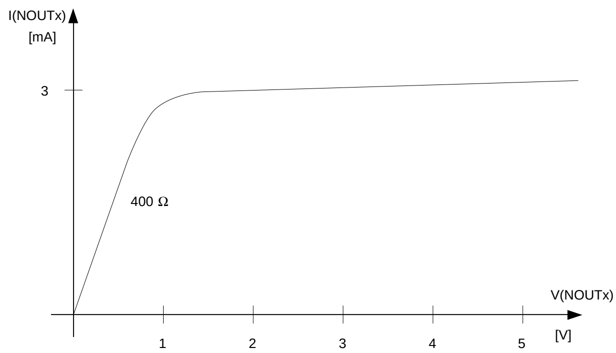


Figure 4: Output characteristic of the lowside transistor at NOUTx

Status output NOK

The status output NOK is a current limited 40 V proof open-drain output. The output transistor is switched on if the lo-level of the outputs NOUTx are enabled with exactly one pin ENx, the outputs have reached the voltage levels defined by the inputs INx, the power supply voltage is above the power-on threshold, the temperature is below the switch off temperature and all power supply pins are connected.

Pull-down currents
In order to enhance noise immunity with limited power dissipation at inputs INx, EN5, EN10 und ENFS the pull-down currents at these pins have two stages. With a rise in voltage at input pins INx, EN5, EN10 und ENFS the pull-down current remains high until Vt()hi (Electrical Characteristics No. 203); above this threshold the device switches to a lower pull-down current. If the voltage falls below Vt()lo (Electrical Characteristics No. 204), the device switches back to a higher pull-down current.

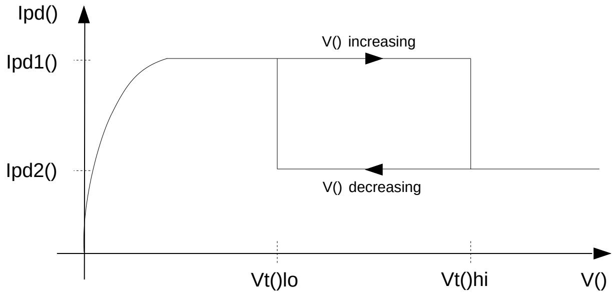


Figure 5: Pull-down currents at INx, EN5, EN10 and ENFS

DETECTING SINGLE ERRORS

If single errors are detected, safety-relevant applications require externally connected switching transistors to be specifically shut down. Single errors can occur when a pin is open (due to a disconnected bonding wire or a bad solder connection, for example) or when two pins are short-circuited.

When two output of different logic levels are short-circuited, the driving capability of the highside driver will predominate, keeping the connected P-channel FETs in a safe shutdown state.

With open pins VB, VBR, GND or GNDR iC-MFP switches the output stages to a safe, predefined high state via pull-up resistors and current sources at the outputs, subsequently shutting down any externally connected P-channel FETs.

Loss of VBR potential
If power supply potential is no longer applied to the VBR-pin, the output stage lowside drivers are shut down and the outputs actively tied to VB via the highside drivers.

Loss of GND potential
If ground potential is no longer applied to the GND-pin, the output stage lowside drivers are shut down and the outputs actively tied to VB via the highside drivers.

Loss of GNDR potential
If ground potential is no longer applied to the GNDR-pin, the output stage lowside drivers are shut down and the outputs actively tied to VB via the highside drivers.

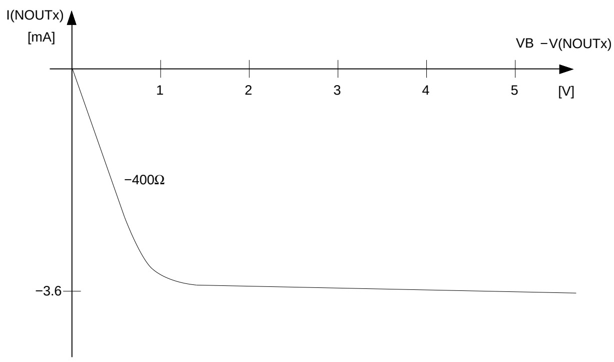


Figure 6: Output characteristics at NOUTx with loss of VBR, GND or GNDR

Loss of VB potential
If power supply potential is not longer applied to VB, the output stages are shut down and the outputs tied to VBR via internal pull-up resistors with a typical value of 200 kΩ.

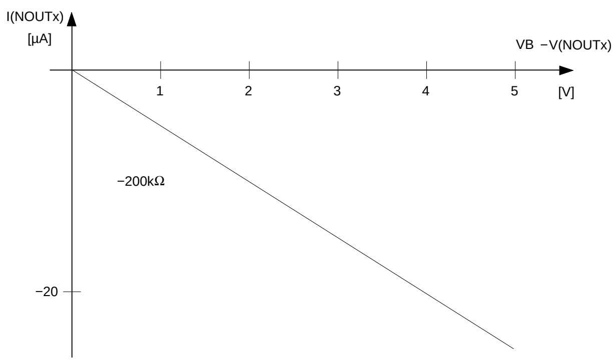


Figure 7: Output characteristics at NOUTx with loss of VB

APPLICATION NOTES

Driving an P-channel MOSFET

One typical field of application for iC-MFP is in the operation of P-FETs with microprocessor output signals, as shown in Figure 8.

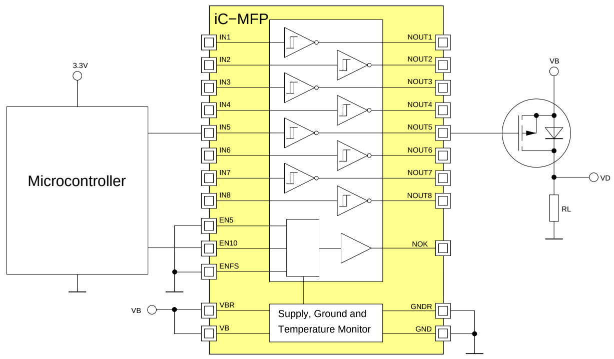


Figure 8: Driving an P-channel MOSFET

Slowly switching of a transistor is done with a current limited driver. Figure 9 shows the different phases of a turn on process with resitive load. In Section t0 to t1 the gate of the transistors is loaded to the threshold voltage Vth(FET) and is a dead time. In section t1 to t2 the gate voltage keeps nearly constant (miller-plateau) during the drain voltage slope. The slew rate is depending on the current of the driver and the gate-drain capacitor of the transistor. In section t2 to t3 the gate voltage reach the static value. The transistor thus goes low ohmic and minimizes the power dissipation. The equations 1 to 4 are simplified and give an estimation of the timing on the basis of data from the specifications of the device iC-MFP and the used transistor. The turn off looks similar to the turn on but with reverse run trough.

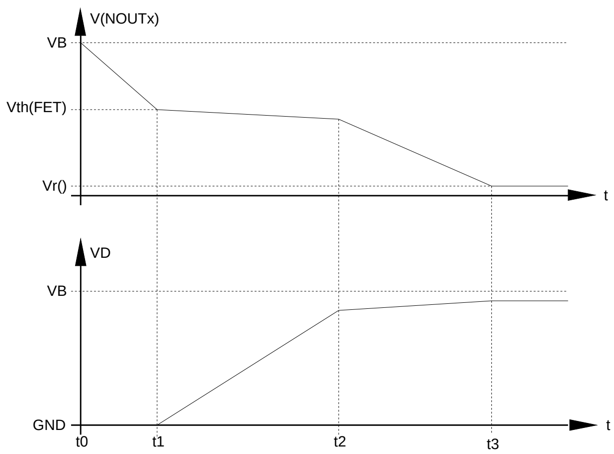


Figure 9: On switching of a transistor

$$t_{t0..t1}[\mu s] = C_{iss}@(V_{ds} = hi) \times \frac{V_{th}(FET)}{-Isc(NOUTx)lo} \qquad (1)$$

$$t_{t1..t2}[\mu s] = C_{rss}@(V_{ds} = hi) \times \frac{VB}{-Isc(NOUTx)lo} \qquad (2)$$

$$t_{t2..t3}[\mu s] = C_{iss}@(V_{ds} = lo) \times \frac{Vr(NOUTx) - V_{th}(FET)}{-Isc(NOUTx)lo} \qquad (3)$$

$$t_{on} = t_{t0..t1} + t_{t1..t2} + t_{t2..t3} \qquad (4)$$

$C_{iss} = C_{gs} + C_{gd}$ = voltage dependent gate-source and gate-drain capacitor [nF]
$C_{rss} = C_{gd}$ = voltage dependent gate-drain capacitor [nF]
$Isc(NOUTx)lo$ = short circuit current lo at NOUTx [mA]
$t_{t0..t1}$ = dead time [µs]
$t_{t1..t2}$ = slope time at drain (Miller-Plateau) [µs]
$t_{t2..t3}$ = time to reach static gate voltage [µs]
t_{on} = overall turn on time [µs]
VB = power supply VB [V]
$Vr(NOUTx)$ = configured static turn on voltage at NOUTx [V]
$V_{th}(FET)$ = threshold of the transistor [V]

Example

Turn on calculation with following estimations:
$C_{iss}@(V_{ds} = -24\ V)$ = 1.5 nF
$C_{iss}@(V_{ds} = -1\ V)$ = 3 nF
$C_{rss}@(V_{ds} = -24\ V)$ = 0.3 nF
$Isc(NOUTx)lo$ = 4 mA
VB = 24 V
$Vr(NOUTx)$ = -10 V
$V_{th}(FET)$ = -3 V
From this follows:
$t_{t0..t1}$ = 1.13 µs
$t_{t1..t2}$ = 1.8 µs
$t_{t2..t3}$ = 5.25 µs
t_{on} = 8.18 µs
The slew rate at the drain of transistor is: 13.3 V/µs

Figure 10 shows the turn on and off at one channel with pin INx. The pulse duration at pin NOK, especially at turn on, can be used for monitoring the connected transistor and the load.

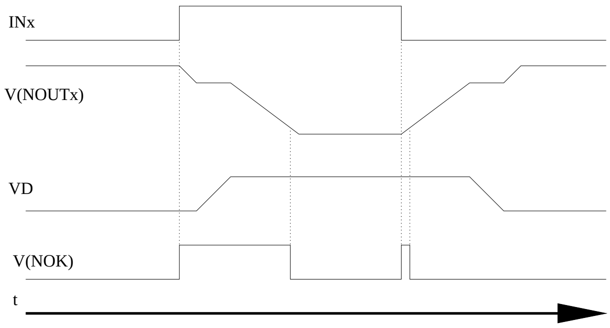


Figure 10: Turn on and off one channel with INx

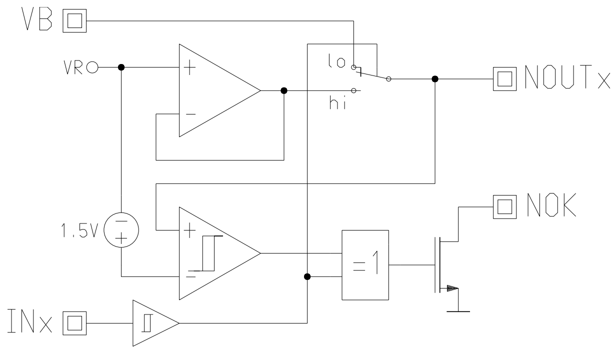


Figure 11: Circuit diagram one channel with monitoring comparator

ORDERING INFORMATION

Type	Package	Order Designation
iC-MFP	QFN24 4 mm	iC-MFP QFN24

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