iC-TW11 10-BIT ULTRA LOW POWER MAGNETIC ABSOLUTE ROTARY ENCODER

preliminary

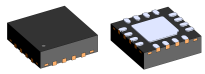
FEATURES

- 10-bit angle resolution
- Split power supplies for 1.8 V I/O applications
- Sampling initiated via SPI command or dedicated pin
- 4 kHz maximum sampling frequency
- 21 µA typical supply current at 10 Hz sampling frequency
- Low power mode reduces current to 3 µA at 10 Hz
- Automatic power-down to 100 nA between samples
- Standard 4-wire SPI communication
- Automatic Hall array gain control (AGC)
- Digital filter to reduce measurement noise
- Operational temperature range of -40 to +125 °C
- Space-saving, RoHS compliant 4x4 mm QFN16 package

APPLICATIONS

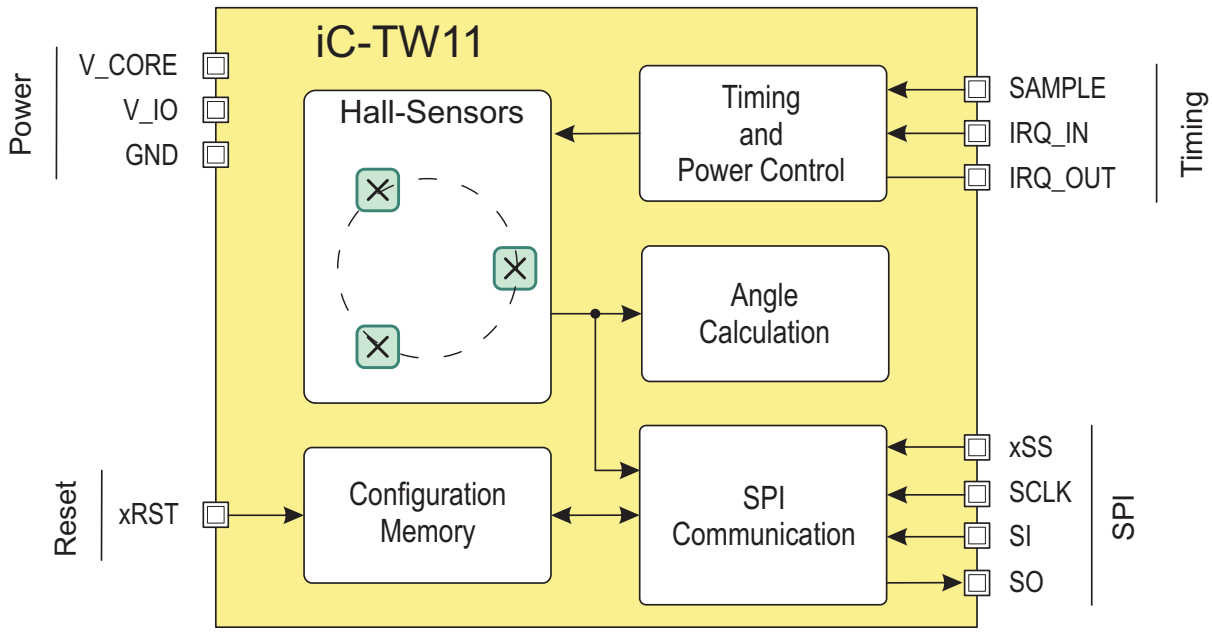
- Battery-powered equipment
- Digital potentiometers
- Front panel controls
- Servo or stepper motor control
- Assembly robots and autonomous vehicles
- Office equipment and household appliances

PACKAGES



16-pin QFN
4 mm x 4 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The iC-TW11 is a single-chip magnetic rotary encoder for low voltage (1.8-3.3 V) and low-power end-of-shaft applications. It includes three Hall elements, automatic power management features, and offers 10-bit resolution in a space-saving 4x4 mm QFN package with 16 pins. Built-in automatic gain control (AGC) assures optimum analog-to-digital conversion under all conditions with no setup. A noise filter improves measurement stability, and can be disabled to reduce power consumption.

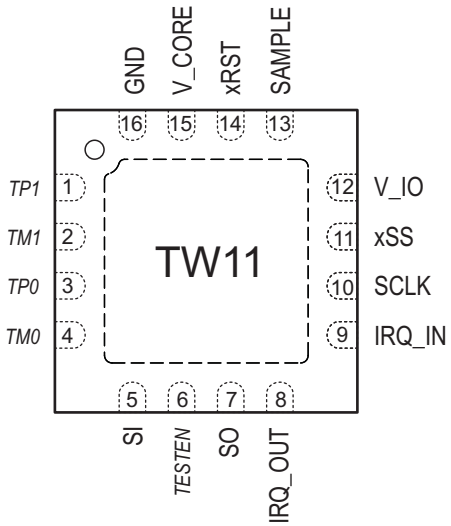
The iC-TW11 supports a maximum conversion rate of 4 kHz (4 000 samples per second) with power consumption proportional to the conversion rate. Low power mode reduces the supply current by a factor of 7 while increasing the maximum sampling rate to 20 kHz. Sampling is initiated over the SPI interface or via a dedicated pin for application versatility.

Communication and control of the iC-TW11 is via a 4-wire SPI interface and multiple devices can be chained together for efficient usage. Absolute position angle, angle-equivalent sine and cosine values, and the three raw Hall element voltages can all be read over the SPI interface allowing both simple and sophisticated applications to be implemented easily.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION QFN16-4x4 (top view)



PIN FUNCTIONS

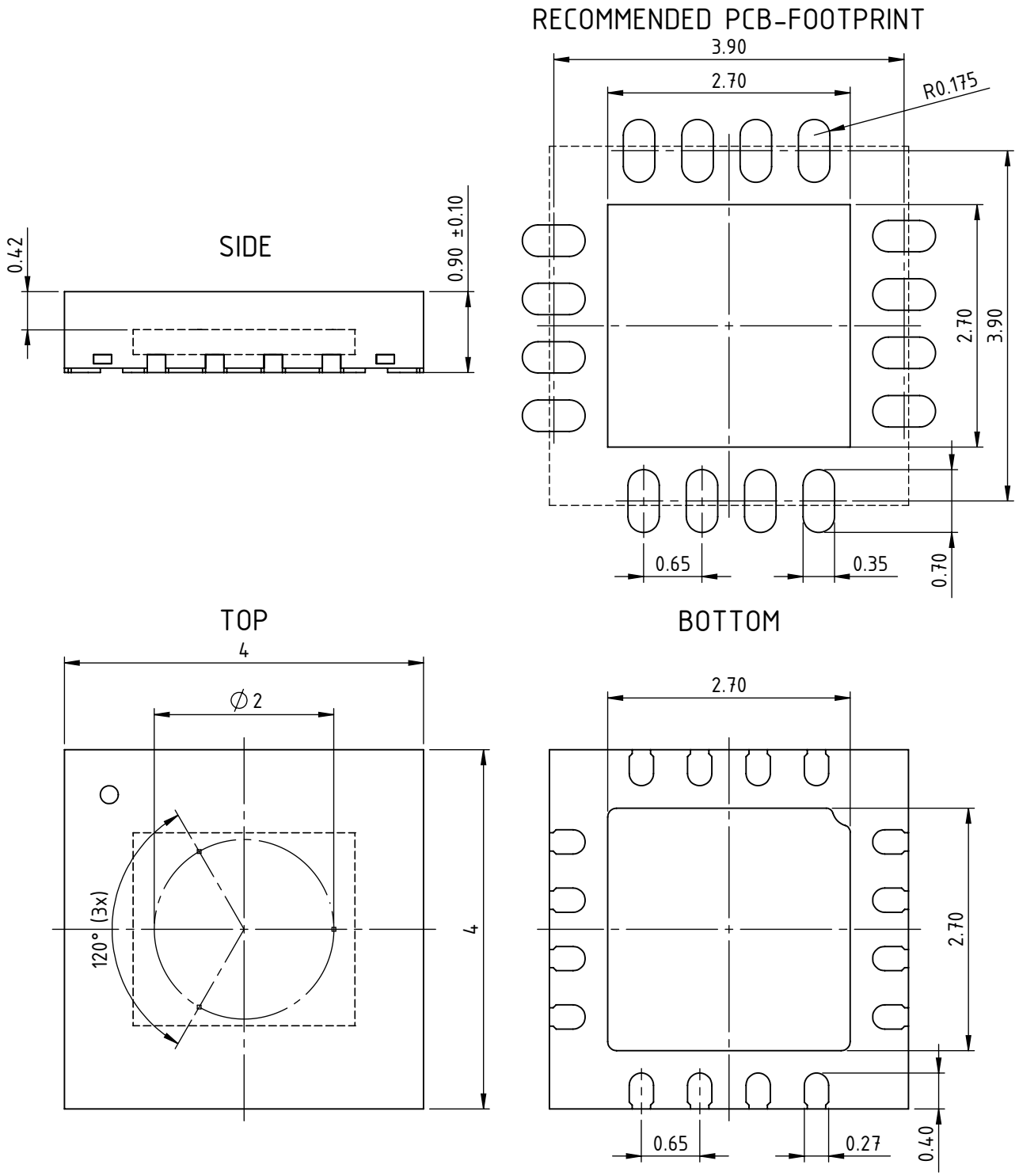
No.	Name	Function
12	V_IO	+1.8 V to +3.3 V IO Power Supply
15	V_CORE	+3.3 V Main Power Supply
16	GND	Ground
	EP[1)]	Exposed Pad

1) The backside paddle may have a single link to GND. A current flow across the paddle is not permissible.

PIN FUNCTIONS

No.	Name	I/O	Function	Description
1	TP1	Analog I/O	Test Pin	Do not use. Connect to GND for normal operation.
2	TM1			
3	TP0			
4	TM0			
5	SI	Digital Input	SPI Slave Input	Connect to SPI Master Output (MOSI).
6	TESTEN	Digital Input	Test Enable	Do not use. Connect to GND for normal operation.
7	SO	Digital Output	SPI Slave Output	Connect to SPI Master Input (MISO).
8	IRQ_OUT	Digital Output	Interrupt Request Output	Connect to host input or IRQ_IN of another iC-TW11.
9	IRQ_IN	Digital Input	Interrupt Request Input	Used only in multiple iC-TW11 device chains. Connect to GND for single device operation.
10	SCLK	Digital Input with hysteresis	SPI Clock Input	Connect to SPI Master clock output.
11	xSS	Digital Input (active low)	SPI Slave Select Input	Connect to SPI Master slave (chip) select output.
12	V_IO	Supply	IO Power Supply	+1.8 V to +3.3 V power supply input. Determines the operating voltage of all iC-TW11 digital I/O.
13	SAMPLE	Digital Input	External Sample Input	Initiates sampling and conversion of magnet position. Connect to GND if using SPI sampling.
14	xRST	Digital Input (active low)	Reset Input	Connect to host output or other reset source. iC-TW11 is in low-power sleep mode if xRST is low.
15	V_CORE	Supply	Main Power Supply	+3.3 V power supply input. Connect to 3.3 V power supply.
16	GND	Ground	Power Supply Common	Circuit common for all I/O.

PACKAGE DIMENSIONS QFN16 4x4



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±0.1mm / ±1° (with respect to backside pad).

dra_qfn16-4x4-2_tw11_c2_pack_1, 15:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these values damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at V_CORE		-0.3	4	V
G002	V()	Voltage at V_IO		-0.3	4	V
G003	V()	Voltage at any pin		-0.3	V_IO + 0.3	V
G004	I()	Input Current at any pin (except V_CORE or V_IO)		-10	10	mA
G005	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G006	Tj	Junction Temperature		-40	150	°C
G007	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN16 surface mounted to PCB according to JEDEC 51		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: V_CORE = 3.0 to 3.6 V_IO = 1.7 to V_CORE, Tj = -40 to +125 °C.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	V_CORE	Main Supply Voltage		3.0	3.3	3.6	V
002	V_IO	I/O Supply Voltage		1.7	1.8	V_CORE	V
003	I(V_CORE)	Main Supply Current	not including I/O current, xRST high and conversion in progress		10		mA
004	I(V_CORE)	Main Supply Current, normal mode	not including IO current, CONFIG.lpwr = 0; fs = 10 Hz fs = 1 kHz fs = 4 kHz		 21 2100 8200		 µA µA µA
005	I(V_CORE)	Main Supply Current, low power mode	not including IO current, CONFIG.lpwr = 1; fs = 10 Hz fs = 1 kHz fs = 20 kHz		 2.6 260 5200		 µA µA µA
006	I(V_CORE)	Main Supply Current, sleep mode	not including IO current, xRST low or no conversion in progress; Tj = 25 °C Tj = 125 °C			 100 500	 nA nA
Hall Sensors and Angle Calculation							
101	Hext	Permissible Magnetic Field Strength	at chip surface	25		150	kA/m
102	dsens	Diameter of Hall Sensor Circle	center to center of Hall plates		2		mm
103	RES	Angle Resolution			10		bits
104	AAabs	Absolute Angle Accuracy	Bomatec BMN-35H diametric NdFeB magnet of Ø4x4mm, centered on package at 0.5 mm airgap, quasi static		±1		°
105	tconv	Conversion Time	normal mode: CONFIG.lpwr = 0 low power mode: CONFIG.lpwr = 1		225 40	300 54	µs µs
Digital Inputs (SI, IRQ_IN, SCLK, xSS, SAMPLE, xRST)							
301	Vt()hi	Threshold Voltage hi	V(V_IO) = 3.0...3.6 V V(V_IO) = 1.7...2.0 V			2.48 1.44	V V
302	Vt()lo	Threshold Voltage lo	V(V_IO) = 3.0...3.6 V V(V_IO) = 1.7...2.0 V	0.82 0.36			V V
303	fin(SCLK)	Permissible Clock Frequency at SCLK Pin				16	MHz
304	tw (SAMPLE)	Permissible Pulse Width at SAMPLE Pin		10			ns
Digital Outputs (SO, IRQ_OUT)							
401	Vs()hi	Saturation Voltage hi	Vs()hi = V(V_IO) − V(); V(V_IO) > 3.0 V, I() = -4 mA V(V_IO) > 1.7 V, I() = -2 mA			 0.8 0.7	 V V
402	Vs()lo	Saturation Voltage lo	V(V_IO) > 3.0 V, I() = 4 mA V(V_IO) > 1.7 V, I() = 2 mA			0.4 0.4	V V
Reset and Start-Up							
501	tstart	Startup Time	device operational after xRST lo → hi			1	µs

OPERATING REQUIREMENTS: SPI Interface

Operating conditions: V_CORE = 3.0 to 3.6 V, V_IO = 1.7 to V_CORE, Tj = -40 to +125 °C.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI Interface Timing						
I001	t_{C1}	Permissible Clock Cycle Time	see Elec. Char. No.: 303	1/f(SCLK)		
I002	t_{D1}	Clock Signal Lo Level Duration		15		ns
I003	t_{D2}	Clock Signal Hi Level Duration		15		ns
I004	t_{S1}	Setup Time: xSS lo before SCLK lo → hi		50		ns
I005	t_{H1}	Hold Time: xSS lo after SCLK hi → lo		50		ns
I006	t_{W1}	Wait Time: between xSS lo → hi and xSS hi → lo	sup = 1 (no measurement) sup = 0 (refer to Table 22)		5 300	µs µs
I007	t_{S2}	Setup Time: SI stable before SCLK lo → hi		5		ns
I008	t_{H2}	Hold Time: SI stable after SCLK lo → hi		10		ns
I009	t_{P1}	Propagation Delay: SO stable after xSS hi → lo			25	ns
I010	t_{P2}	Propagation Delay: SO high impedance after xSS lo → hi			25	ns
I011	t_{P3}	Propagation Delay: SO stable after SCLK hi → lo			25	ns

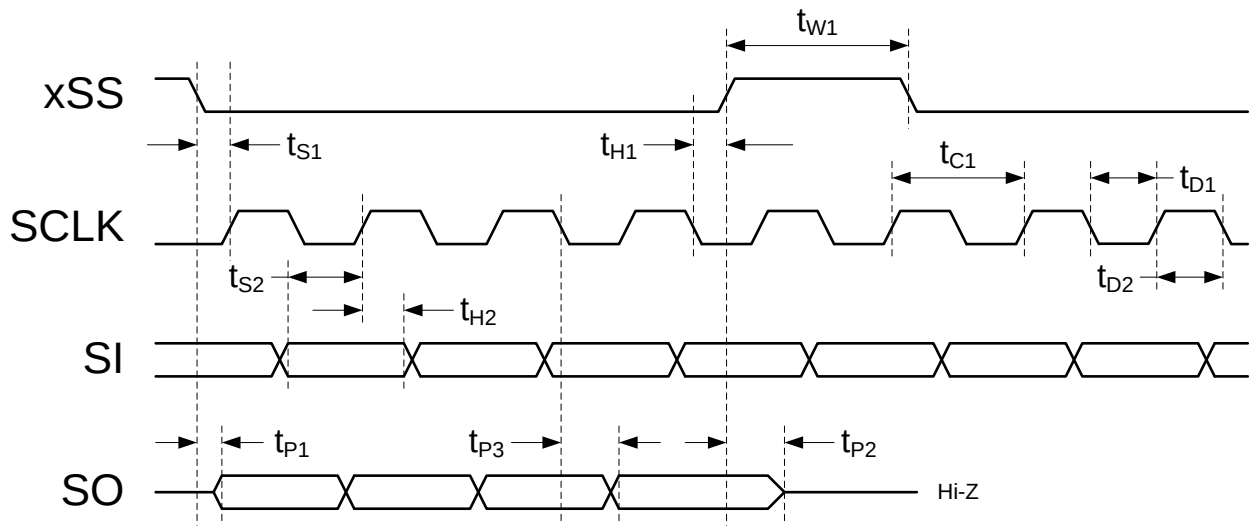


Figure 1: SPI Timing

FUNCTIONAL BLOCK DIAGRAM

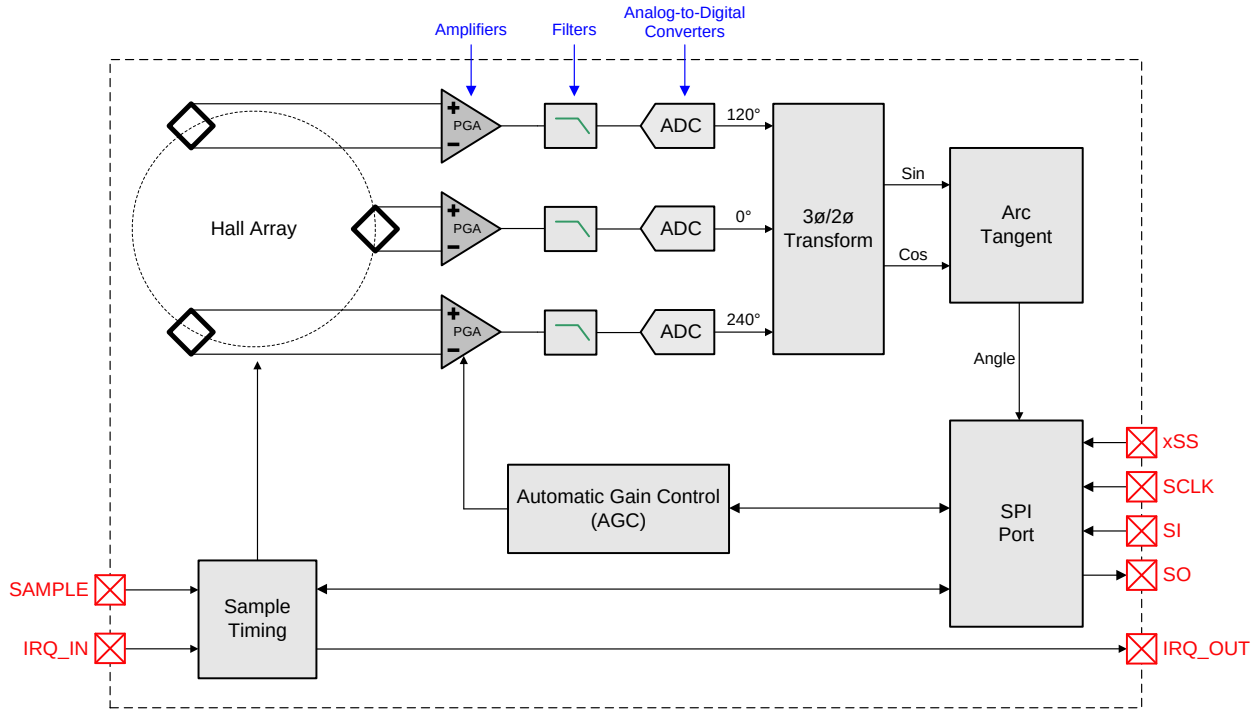


Figure 2: Block diagram

Hall Array

Three Hall effect sensors are integrated into the iC-TW11 to directly sense the angular position of a dipole permanent magnet positioned over the chip. The three sensors are equally spaced (120° apart) on a Ø 2 mm circle centered on the 4x4 mm package.

Programmable Gain Amplifiers

Three programmable gain amplifiers condition and amplify the signals from the three Hall sensors. 18 gain values in steps of approximately 1.5 dB are available to properly match the sensor voltages to the ADCs for highest conversion accuracy.

Filters

The three conditioned Hall signals are each filtered by first-order 10 kHz filters to reduce sampling noise and improve measurement stability and accuracy. These filters can be disabled to lower power consumption and to allow faster sampling rates.

Analog-to-Digital Converters (ADCs)

Three ADCs convert the conditioned and filtered Hall signals into 10-bit digital values. The remainder of the signal path is completely digital.

3Ø/2Ø Transform

The three-phase Hall signals are next converted to equivalent sine and cosine values using a Clarke transform algorithm.

Arc-Tangent

Finally, a CORDIC arc-tangent algorithm calculates the angular position of the permanent magnet based on the converted sin and cos values.

SPI Port

The iC-TW11 uses a standard SPI (serial peripheral interface) slave port for all communication. This includes sampling and reading the angular position as well as reading and writing internal registers.

Automatic Gain Control

By default, the iC-TW11 automatically sets and maintains the optimum gain value for all three Hall channels to ensure accurate conversion. The AGC can be disabled and the gain set manually via SPI commands if required for special applications.

Sample Timing

By default, sampling is initiated by a rising edge on the xSS pin or a falling edge on the SAMPLE pin. Sampling powers up the Hall array and analog circuitry,

measures the three Hall voltages, calculates the angle, adjusts the gain and offset values (for the next measurement) as required, signals that the conversion is complete by asserting an interrupt request on the IRQ_OUT pin, and then powers down the Hall array and analog circuitry.

By default, the interrupt input (IRQ_IN) and output (IRQ_OUT) pins are active-low and the interrupt logic is **AND**. This means that the IRQ_IN pin must be active (low) AND the sampling complete to assert the interrupt output (IRQ_OUT low). The sense of the interrupt logic can be changed to **OR** via SPI commands.

ELECTRICAL CONNECTIONS

The basic electrical connections for the iC-TW11 are shown in Figure 3. Only a host microprocessor or microcontroller and a few passive components are required for operation.

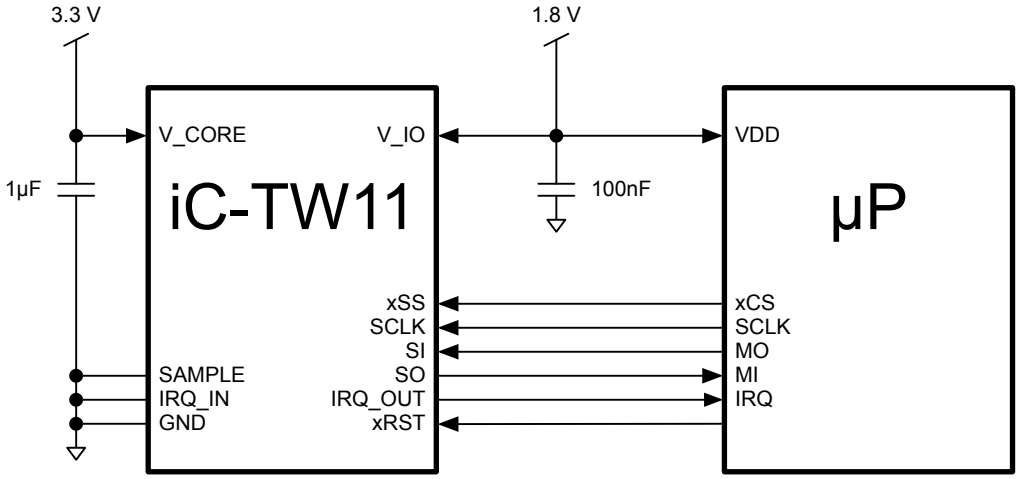


Figure 3: Basic electrical connections

The iC-TW11 has two power supply inputs. V_CORE (pin 15) is the main 3.3V power supply input and it must be well bypassed to provide a low impedance power source. This is important because the current consumption of the iC-TW11 is approximately 10 mA while active and current is drawn in short pulses. Depending on the quality of the V_CORE supply it may be necessary to use additional capacitors and/or supply filtering to achieve the required stability.

V_IO (pin 12) is a separate power supply input that sets the operating level of the I/O signals. V_IO can range from 1.8 V up to V_CORE and it should also be well bypassed. Typically, a 1.8 V supply would be used to power the host microprocessor and the iC-TW11 V_IO input as shown in Figure 3.

The iC-TW11 reset input xRST (pin 14) is typically driven from the host µP as shown. Alternatively, a sufficiently slow RC network can be connected to xRST for use as a reset source. R = 47 kΩ and C = 100 nF provide about a 5 millisecond time constant which should be adequate for most applications.

The four SPI lines should be connected to their corresponding pins on the host µP as shown.

To use the iC-TW11 in its default condition (i.e. without any configuration), it is necessary to connect IRQ_IN (pin 9) to ground as shown to allow proper interrupt generation at IRQ_OUT. If external sampling is not used, SAMPLE (pin 13) should also be tied to ground as shown to avoid spurious samples. The five reserved pins (1-4 and 6) must also be tied to ground for proper operation (not shown above).

SPI COMMUNICATION

The iC-TW11 SPI port is a 4-wire slave interface which operates in CPOL = 0 and CPHA = 0 mode only (SPI Mode 0). This means that the base (resting) value of SCLK (pin 10) is low, SI (pin 5) is sampled on the rising edge of SCLK, and SO (pin 7) is changed on the falling edge of SCLK. The active-low slave select input, xSS (pin 11), is used by the host µP to enable the SPI port to initiate communication. Data is transferred with MSB first.

SPI communication uses an overlapped packet structure where the response to a command is returned while the next command is being sent. Figure 4 shows this for a single-device application (where the host controls a single iC-TW11 slave). See BUSSING MULTIPLE ICs on page 21 and CHAINING MULTIPLE ICs on page 22 for multiple device applications.

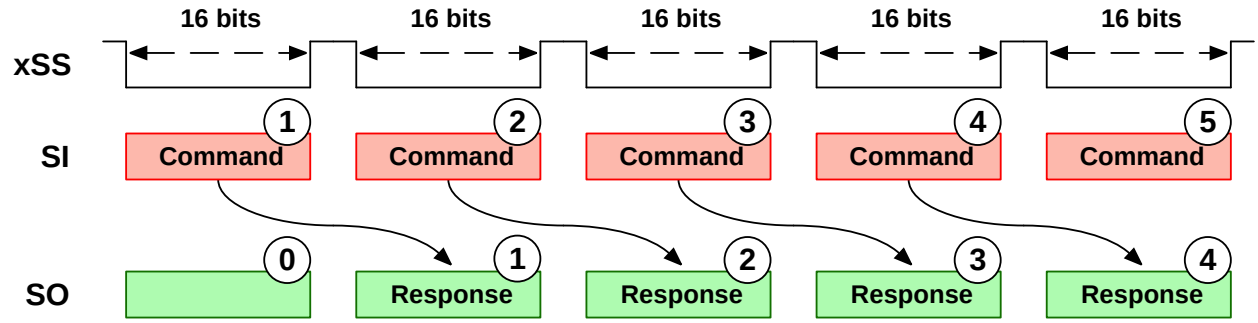


Figure 4: SPI overlapped packet structure

SPI command and response packets are always 16 bits long. The host initiates communication with the iC-TW11 by driving slave select (xSS) low and then clocking a 16-bit command (1) to the slave input, SI. The serial clock (SCLK) signal is not shown in Figure 4. The host drives xSS high at the end of the command packet and the iC-TW11 executes the command.

After waiting for the command to be executed (or for the iC-TW11 to assert IRQ_OUT), the host again drives xSS low and sends the next command packet (2) to SI while at the same time reading the 16-bit response (1) to the initial command (1) on the slave output, SO.

The iC-TW11 always returns a response packet while reading a command packet. The response packet (0) returned while writing the first command packet (1) is not defined. Likewise, the response packet returned after a register write command is not defined.

SPI COMMAND AND RESPONSE PACKET FORMAT

Command packet format

Command packets sent to the iC-TW11 by the host are formatted as shown in Table 6.

Command Packet		
Bit	Name	Description
15	sup	Suppress new sample
14	wr	Write Data to Address
13:8	address	6-bit Register Address
7:0	data	8-bit Register Data

Table 6: Command packet format

A read command is one in which the write bit, wr, (bit 14) is 0. The register at the specified address (bits 13-8) is read and its contents returned in the next response packet. Data (bits 7-0) are ignored.

A write command is one in which wr (bit 14) is 1. The data (bits 7-0) is written to the register at the specified address (bits 13-8).

The suppress bit, sup (bit 15), when set (1) suppresses the next sample. This is useful when using external sampling or when reading sine and cosine data to ensure simultaneously-sampled values. Normally, sup = 0.

Response packet format

The format of response packets depends on the specific register that is read (see Table 8 on the following page). The response packet returned following a write command is undefined.

REGISTER MAP

The iC-TW11 contains 10 user-accessible registers, all of which can be read and two of which can be written. Each of these registers is explained in detail in the following sections.

Address	Name	Description	Access
0x00	ANGLE	Sampled Angle	Read
0x01	SIN	Sine of Angle	Read
0x02	COS	Cosine of Angle	Read
0x03	HALL0	0° Hall Voltage	Read
0x04	HALL120	120° Hall Voltage	Read
0x05	HALL240	240° Hall Voltage	Read
0x06-0x1F	-	Reserved	None
0x20	DEVICE	Device Information	Read
0x21	CONFIG	Configuration Bits	R/W
0x22	STATUS	Conversion Status	Read
0x23	GAIN	Hall Array Gain	R/W
0x24-0x3F	-	Reserved	None

Table 7: Register map

OVERVIEW																
Addr	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANGLE																
0x00	busy	err	gain (4:1)				angle									
SIN																
0x01	busy	err	reserved (0)		sine											
COS																
0x02	busy	err	reserved (0)		cosine											
HALL0, HALL120, HALL240																
0x03	busy	err	reserved (0)				hall0									
0x04	busy	err	reserved (0)				hall120									
0x05	busy	err	reserved (0)				hall240									
DEVICE																
0x20	not used								rev				id			
CONFIG																
0x21	not used								0	spol	smod	0	imod	noagc	0	lpwr
STATUS																
0x22	not used								reserved (0)					uflo	oflo	busy
GAIN																
0x23	not used								reserved (0)			gain (4:0)				

Table 8: Register layout

ANGLE Register

The ANGLE register is a 16-bit read-only register that contains the most recently converted angular position of the magnet.

ANGLE Register		Addr. 0x00
Bit	Name	Description
15	busy	Busy; angle is undefined
14	err	Error during conversion
13:10	gain	4 MSBs of Hall array gain
9:0	angle	10-bit angle

Table 9: ANGLE Register

The angle is returned as a positive integer in the range of 0-1023 (0x000-0x3FF). The magnet angle in degrees is calculated as

$$Angle\,[^\circ] = Sampled\ Angle \cdot \frac{360}{1024}$$

ANGLE.gain (bits 13-10) is the 4 most significant bits of the current Hall array gain and is returned as a positive integer in the range 0-8. Hall array gain is proportional to the airgap between the magnet and the iC-TW11 (a larger airgap requires more gain) and thus gain can be used in pushbutton applications to detect if the knob is pressed or released. The full 5-bit gain value is available in the GAIN register (0x23).

The busy bit, busy (bit 15) indicates whether or not a conversion is in process. If ANGLE.busy = 0, the conversion is complete and ANGLE.angle is valid. If ANGLE.busy = 1, the conversion is in process and ANGLE.angle is undefined.

The error bit, err (bit 14) indicates whether or not an error occurred during the conversion. If ANGLE.err = 0, there were no conversion errors and ANGLE.angle is valid. If ANGLE.err = 1, there was an error during conversion and ANGLE.angle may not be valid. Conditions that set the error bit are:

1. ADC overflow. The measured Hall signal amplitudes were too high to provide an accurate angle. The AGC lowers the Hall sensor gain for the next conversion. An ADC overflow status bit is also available. See STATUS register on page 15 for more information.
2. ADC underflow. The measured Hall signal amplitudes were too low to provide an accurate Angle. The AGC raises the Hall sensor gain for the next conversion. An ADC underflow status bit is also available. See STATUS register on page 15 for more information.

If either ANGLE.busy = 1 or ANGLE.err = 1, the register read should be performed again to ensure an accurate angle value.

SIN Register

The SIN register is a 16-bit read-only register that contains the sine component used to calculate the most recently converted angular position of the magnet.

When reading the SIN register, it is recommended to suppress the next sample by setting sup = 1 in the command packet. This ensures that the sine value read is consistent with the angle calculated from the previous (most recent) sample.

SIN Register		Addr. 0x01
Bit	Name	Description
15	busy	Busy; sine is undefined
14	err	Error during conversion
13:12	-	Reserved (0)
11:0	sine	12-bit sine of angle

Table 10: SIN Register

SIN.sine is returned as a signed 2's complement value in the range ±1533 (±0x5FD). The magnitude of SIN.sine depends on the strength of the magnetic field and the gain in use when the sample was taken.

The busy bit, busy (bit 15) indicates whether or not a conversion is in process. If SIN.busy = 0, the conversion is complete and SIN.sine is valid. If SIN.busy = 1, the conversion is in process and SIN.sine is undefined.

The error bit, err (bit 14) indicates whether or not an error occurred during the conversion. If SIN.err = 0, there were no conversion errors and SIN.sine is valid. If SIN.err = 1, there was an error during conversion and SIN.sine may not be valid. See ANGLE register for conditions that set the error bit.

COS Register

The COS register is a 16-bit read-only register that contains the cosine component used to calculate the most recently converted angular position of the magnet.

When reading the COS register, it is recommended to suppress the next sample by setting sup = 1 in the command packet. This ensures that the cosine value read is consistent with the angle calculated from the previous (most recent) sample.

COS Register		Addr. 0x02
Bit	Name	Description
15	busy	Busy; cosine is undefined
14	err	Error during conversion
13:12	-	Reserved (0)
11:0	cosine	12-bit cosine of angle

Table 11: COS Register

COS.cosine is returned as a signed 2's complement value in the range ±1533 (±0x5FD). The magnitude of COS.cosine depends on the strength of the magnetic field and the gain in use when the sample was taken.

The busy bit, busy (bit 15) indicates whether or not a conversion is in process. If COS.busy = 0, the conversion is complete and COS.cosine is valid. If COS.busy = 1, the conversion is in process and COS.cosine is undefined.

The error bit, err (bit 14) indicates whether or not an error occurred during the conversion. If COS.err = 0, there were no conversion errors and COS.cosine is valid. If COS.err = 1, there was an error during conversion and COS.cosine may not be valid. See ANGLE Register for conditions that set the error bit.

HALL Registers

The three HALL registers (HALL0, HALL120, and HALL240) are 16-bit read-only registers that contain the sampled signal amplitude of the three Hall sensors used to calculate the most recently converted angular position of the magnet.

When reading the HALL registers, it is recommended to suppress the next sample by setting sup = 1 in the command packet. This ensures that the values read are consistent with the angle calculated from the previous (most recent) sample.

HALL Registers		
HALL0		Addr. 0x03
HALL120		Addr. 0x04
HALL240		Addr. 0x05
Bit	Name	Description
15	busy	Busy; Hall data undefined
14	err	Error during conversion
13:10	-	Reserved (0)
9:0	hall	10-bit Hall signal amplitude

Table 12: HALL Registers

The Hall signal amplitudes are returned as signed 2's complement values in the range of ±511 (±0x1FF). The actual magnitude of the Hall signals depends on the strength of the magnetic field and the gain in use when the sensors were sampled.

The busy bit, busy (bit 15) indicates whether or not a conversion is in process. If busy = 0, the conversion is complete and the Hall data is valid. If busy = 1, the conversion is in process and the Hall data is undefined.

The error bit, err (bit 14) indicates whether or not an error occurred during the conversion. If err = 0, there were no conversion errors and the Hall data is valid. If err = 1, there was an error during conversion and the Hall data may not be valid. See ANGLE Register for conditions that set the error bit.

DEVICE Register

The DEVICE register is an 8-bit read-only register that contains identifying information about the device.

The DEVICE Register value is returned in the lower byte of the Response packet.

DEVICE Register		Addr. 0x20
Bit	Name	Description
7:4	rev	Chip Revision Current: rev = 5 for iC-TW11_D1
3:0	id	Chip Identification (11, 0xB)

Table 13: DEVICE Register

CONFIG Register

The CONFIG register is an 8-bit read/write register that can be used to configure the iC-TW11.

When writing the CONFIG register, it is recommended to suppress the next sample by setting sup = 1 in the command packet to avoid sampling with an undefined configuration. When reading the CONFIG register, the value is returned in the lower byte of the response packet.

CONFIG Register		Addr. 0x21
Bit	Name	Description
7	-	Reserved (must be 0)
6	spol	Sample input polarity
5	smod	Sampling mode
4	-	Reserved (must be 0)
3	imod	Interrupt request (IRQ) Mode
2	noagc	AGC disable
1	-	Reserved (must be 0)
0	lpwr	Low power mode

Table 14: CONFIG Register

The default value of the CONFIG register at power-up is 0x00.

The sample input polarity bit, spol (bit 6) determines which edge of the SAMPLE input is used to sample the Hall array and do a new conversion.

CONFIG.spol	Addr. 0x20; bit 6
0	Sample on falling edge (default)
1	Sample on rising edge

Table 15: Sample input polarity

The sampling mode bit, smod (bit 5) is used to disable sampling on the rising edge of xSS at the end of an SPI command packet.

CONFIG.smod	Addr. 0x21; bit 5
0	SPI sampling enabled (default)
1	Disable SPI sampling

Table 16: Sampling mode

CONFIG.smod should be set when using the SAMPLE pin instead of SPI sampling. See USING THE SAMPLE INPUT on Page 19 for more information.

The IRQ mode bit, imod (bit 3) determines the logic used to activate IRQ_OUT.

CONFIG.imod	Addr. 0x21; bit 3
0	IRQ_OUT = IRQ_IN **AND** conversion complete (default)
1	IRQ_OUT = IRQ_IN **OR** conversion complete

Table 17: IRQ mode

See USING INTERRUPTS on page 19 for more information on using CONFIG.imod.

The AGC disable bit, noagc (bit 2) is used to disable automatic control of the Hall sensor gain. The AGC should only be disabled if an alternate gain control system is implemented in the host µP.

CONFIG.noagc	Addr. 0x21; bit 2
0	Automatic gain control active (default)
1	Disable automatic gain control

Table 18: AGC disable

If CONFIG.noagc = 1, proper Hall array gain must be set by writing the appropriate value to the GAIN Register (0x23).

The low power mode bit, lpwr (bit 0) is used to reduce the power consumption of the chip by disabling the Hall sensor filters and shortening the conversion time.

CONFIG.lpwr	Addr. 0x21; bit 0
0	Normal power operating mode (default)
1	Enable low power mode

Table 19: Low power mode

See USING LOW POWER MODE on Page 20 for more information on using CONFIG.lpwr and low power mode.

STATUS Register
The STATUS register is an 8-bit read-only register that shows the status of the most recent sample.

When reading the STATUS register, it is recommended to suppress the next sample by setting sup = 1 in the command packet. This ensures that the status read is consistent with the previous (most recent) sample. The STATUS register value is returned in the lower byte of the response packet.

STATUS Register		Addr. 0x22
Bit	Name	Description
7:3	-	Not used (0)
2	uflo	ADC underflow
1	oflo	ADC overflow
0	busy	Busy

Table 20: STATUS Register

The ADC underflow bit, uflo (bit 2) indicates that the Hall signal levels for the most recent sample were too low to provide an accurate angle conversion. Specifically, STATUS.uflo = 1 if the magnitude of all three Hall signals was less than 50% of the ADC full-scale value (256 = 0x100).

The ADC overflow bit, oflo (bit 1) indicates that the Hall signal levels for the most recent sample were too high to provide an accurate angle conversion. Specifically, STATUS.oflo = 1 if the magnitude of any Hall signal was more than 99% of the ADC full-scale value (506 = 0x1FA).

The busy bit, busy (bit 0) indicates whether or not a conversion is in process. If STATUS.busy = 0, the conversion is complete and STATUS.uflo and STATUS.oflo are valid. If STATUS.busy = 1, the conversion is in process and STATUS.uflo and STATUS.oflo are undefined.

GAIN Register
The GAIN register is an 8-bit read/write register that determines the Hall array gain.

When reading the GAIN register, it is recommended to suppress the next sample by setting sup = 1 in the command packet. This ensures that the gain value read is the actual gain that was used with the previous (most recent) sample. The GAIN register value is returned in the lower byte of the response packet.

GAIN Register		Addr. 0x23
Bit	Name	Description
7:5	-	Not used (0)
4:0	gain	Hall array gain

Table 21: GAIN Register

The Hall array gain is returned as a positive integer in the range 0-17 (0x00-0x11). GAIN.gain = 0 is the lowest gain and GAIN.gain = 17 is the highest gain. Each LSB change in GAIN.gain represents a change of approximately 1.5 dB in the Hall array gain.

Normally (i.e. in default mode; CONFIG.noagc = 0), the GAIN register is updated automatically by the AGC and it is not necessary to access it. The GAIN register should only be written if the AGC is disabled (CONFIG.noagc = 1). When writing to the GAIN register, it is recommended to suppress the next sample by setting sup = 1 in the command packet to avoid sampling with improper Hall array gain.

READING REGISTERS

A single register read requires two SPI transactions. The first transaction sends the read command packet containing the register address, and the second transaction reads the response packet containing the requested data. If the next command is sent while reading the response packet from the first command, only one additional SPI transaction is required for the next register read.

For example, the two SPI transactions to read the ANGLE register are shown below.

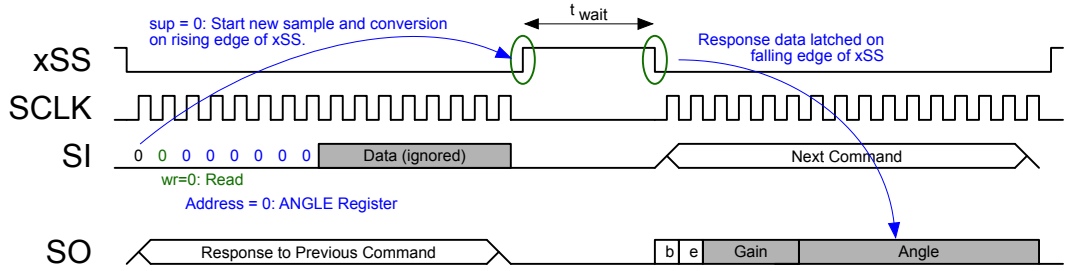


Figure 5: Reading the ANGLE register

The host initiates reading the ANGLE register by activating slave select (xSS) and sending a command packet with the suppress (sup) and write (wr) bits reset, followed by the ANGLE register address (0x00). The data byte in the command packet is ignored but must be provided to fill out the 16-bit packet.*

CONFIG.lp	**Suppress bit (s)**	**t_{wait}** typ.	**t_{wait}** max.
0 (Default)	0	225 µs	300 µs
	1		5 µs
1	0	40 µs	54 µs
	1		5 µs

Table 22: Wait Time for Reading Registers

After sending the command packet, the host deactivates xSS to start the sample and conversion process. The host must then wait for the iC-TW11 to sample the Hall array and convert the angle before reading the response packet. The actual wait time, t_{wait}, depends on the configuration and the suppress bit in the command packet, as shown in Table 22.

After waiting the appropriate amount of time, the host again activates xSS and reads the response packet while sending the next command packet.

Note that the wait times shown are valid when reading any register, not just the ANGLE register. In speed critical applications it is recommended to set the suppress

* Note that when the ignored data byte is 0x00, the complete read ANGLE register command packet is 16 zeros. Thus, in simple applications using the default configuration where it is only necessary to read the angle, SI can be permanently tied low, further simplifying the SPI interface with the host.

bit in the command packet whenever possible to take advantage of the reduced wait time.

Alternatively, the host can wait for the iC-TW11 to activate its interrupt request output (IRQ_OUT) before reading the response packet. See USING INTERRUPTS on Page 19 for more information.

The sine and cosine of the sampled angle can be read from the SIN and COS registers respectively. This is useful, for example, for calculating $\sin^2 + \cos^2$ in the host as a more accurate measure of magnetic field strength or for implementing automatic gain control in the host.

Reading the sine and cosine values takes three SPI transactions. First, the host sends a SIN register read command packet with or without the suppress bit set. After waiting the appropriate amount of time, the host reads the sine value from the response packet while simultaneously writing the COS register read command packet with the suppress bit set to ensure simultaneously-sampled values. After waiting the appropriate amount of time, the host reads the cosine value from the response packet while writing the next command.

Likewise, the raw sampled Hall effect sensor signals can be read from the HALL0, HALL120, and HALL240 registers respectively. This data can be analyzed in the host for quality and integrity to provide general system health status.

Reading the Hall register values takes four SPI transactions. First, the host sends a HALL0 register read command packet with or without the suppress bit set. After waiting the appropriate amount of time, the host reads the 0° Hall sensor value from the response packet while simultaneously writing a HALL120 register read command packet with the suppress bit set to ensure simultaneously-sampled values. After waiting the appropriate amount of time, the host reads the 120° Hall sensor value from the response packet while simultaneously writing a HALL240 register read command packet with the suppress bit set to ensure simultaneously-sampled values. After waiting the appropriate amount of time, the host reads the 240° Hall sensor value from the response packet while writing the next command.

The chip identification, configuration, status, and Hall sensor gain may be read from the DEVICE, CONFIG, STATUS, and GAIN registers respectively. Reading each of these registers requires two SPI transactions, similar to reading the ANGLE register as explained previously.

WRITING REGISTERS

The chip configuration and the Hall array gain of the iC-TW11 can be changed by writing to the CONFIG or GAIN registers respectively. A register write requires a single SPI transaction.

For example, the SPI transaction to write to the CONFIG register is shown below.

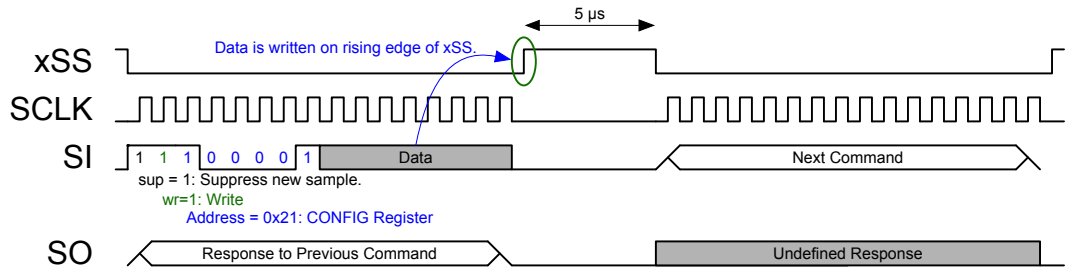


Figure 6: Writing the CONFIG register

The host initiates writing to the CONFIG register by activating slave select (xSS) and sending a command packet with the suppress (sup) and write (wr) bits set, followed by the CONFIG register address (0x21) and the required data. The host then deactivates xSS and the data is written to the CONFIG register. The host should then wait 5 µs before sending the next command. Note that the response packet returned while sending the next command is undefined and should be ignored by the host.

It is only necessary to write to the CONFIG register if the default configuration of the iC-TW11 must be changed. The default configuration is:

- SAMPLE input samples on falling edge.
- SPI sampling enabled.
- IRQ_OUT = IRQ_IN **AND** conversion complete.
- Automatic gain control (AGC) enabled.
- Normal power operating mode.

When using the default configuration, it is not necessary to write to the GAIN register since the iC-TW11's AGC is enabled. If the AGC is disabled by setting CONFIG.noagc = 1, proper Hall array gain must be set by writing the appropriate value to the GAIN register.

STARTUP (DEFAULT CONFIGURATION)

At power-up or after the external reset input, xRST, has been deactivated, the iC-TW11 is in its default state with all registers at 0x00. Specifically, the default state is:

- SAMPLE input samples on falling edge.
- SPI sampling enabled.
- IRQ_OUT = IRQ_IN **AND** conversion complete.
- Automatic gain control (AGC) enabled.
- Normal power operating mode.
- Lowest Hall array gain.

At startup with the default configuration, the AGC is enabled and the Hall array gain is at its lowest value. The first sample (initiated by a command packet with sup = 0 or a falling edge on the SAMPLE input) uses this default gain. After the conversion, the AGC determines whether the Hall signal amplitudes were in the proper range and sets the error bit (err) of the response packet and the ADC overflow (STATUS.oflo) and underflow (STATUS.uflo) bits accordingly.

Typically, the default gain used for the first sample and conversion is too low, resulting in a conversion error (err = 1) due to ADC underflow (STATUS.uflo = 1). In this case, the AGC increments the GAIN register value by 1 to increase the gain for the next sample by approximately 1.5 dB. The next sample uses this new gain and the AGC again increments (or decrements) the GAIN register value by 1 depending on the conversion status after the conversion is complete. This process is repeated for all subsequent samples.

Thus, after startup it can take up to 18 samples for the AGC to determine the proper Hall array gain. Therefore, it is recommended to implement one of the following techniques in the host at startup:

1. Take 20 samples and discard the results.
2. Sample until a response packet with no error (err = 0) is returned or until the STATUS register has a value of 0x00.
3. Write the known gain value for your application (determined by experimentation) to the GAIN register before initiating sampling.

CONVERSION ERRORS

When reading the ANGLE, SIN, COS, HALL0, HALL120, or HALL240 Registers, the status of the most recent conversion is given by the busy (busy) and error (err) bits in the response packet. If either or both of these bits are set, the angle information should be discarded and a new sample initiated.

Conditions that set the Error (err) bit are:

1. ADC overflow. The measured Hall signal amplitudes were too high to provide an accurate angle. The AGC lowers the Hall sensor gain for the next conversion. An ADC overflow status bit is also available. See STATUS register on page 15 for more information.
2. ADC underflow. The measured Hall signal amplitudes were too low to provide an accurate angle. The AGC raises the Hall sensor gain for the next conversion. An ADC underflow status bit is also available. See STATUS register on page 15 for more information.

USING INTERRUPTS

The interrupt request output can be used to notify the host µP when a sample and conversion is complete by connecting IRQ_OUT (pin 8) to a digital input on the host. In this case, after sending the command packet, the host waits for the interrupt request from the iC-TW11 before reading the response packet. This provides faster communication than just waiting for the maximum wait time, t_{wait}.

In the default configuration, IRQ_OUT = IRQ_IN **AND** conversion complete. Therefore, IRQ_IN must be active (low) in order to generate an interrupt output when the conversion is complete. This is typically accomplished by connecting IRQ_IN to ground.

The interrupt logic can be changed to **OR** by setting the interrupt mode bit in the CONFIG register (CONFIG.imod = 1). In this case, IRQ_OUT = IRQ_IN **OR** conversion complete, which is the required logic for multiple bussed devices (see BUSSING MULTIPLE ICs on page 21).

The complete interrupt operation of the iC-TW11 is summarized in the table below.

CONFIG.imod	IRQ_IN	IRQ_OUT
0 (Default)	Low	Low on conversion complete (default)
0 (Default)	High	High
1	Low	Low
1	High	Low on conversion complete

Table 23: Interrupt operation

In all cases IRQ_OUT is deactivated on the falling edge of slave select, xSS.

USING THE SAMPLE INPUT

The SAMPLE input (pin 13) allows an external device to initiate sampling and angle conversion in the iC-TW11. In the default configuration, sampling occurs on the falling edge of the SAMPLE input. To sample on the rising edge of the SAMPLE input, set the sample polarity bit (CONFIG.spol) by writing 0x40 to the CONFIG register (page 14).

When using the SAMPLE input, it is recommended to disable SPI sampling completely by setting the sample mode bit (CONFIG.smod) by writing 0x20 to the CONFIG register (page 14). SPI sampling can also be disabled by setting the suppress bit (s) in every command packet (page 11).

It is also recommended to use the interrupt request output (IRQ_OUT) to notify the host processor that a new sample is ready when using the SAMPLE input. In this case, the host waits for an interrupt request from the iC-TW11 and then sends a read ANGLE register command to fetch the new sample.

Since in the default configuration sampling occurs on the falling edge of the SAMPLE input, connecting the SAMPLE input to xSS simulates sampling on the falling edge of xSS. In this case, disable SPI sampling by setting the sample mode bit (CONFIG.smod) in the CONFIG register (page 14).

USING LOW POWER MODE

For extremely low-power applications, low power mode can be enabled by setting the low power mode bit (CONFIG.lpwr) in the CONFIG register (see page 14). Low power mode imposes certain performance restrictions, so its use should be carefully considered.

Low power mode operates by disabling the low-pass filters on the three Hall sensors (see page 9). Without having to wait for the filters to settle, sampling can occur much faster thus using less power. However, the converted angle and other sampled values are much noisier without the filters, limiting useable resolution compared to normal power mode.

In low power mode, the maximum sampling rate is increased from 4 k Samples per second to 20 k Samples per second. Likewise, typical current consumption is reduced from 2.05 µA per sample per second to 260 nA per sample per second.

CALCULATING CURRENT CONSUMPTION

Current consumption in the iC-TW11 is directly proportional to the sampling frequency, f_s. Lower sampling frequencies use less current and higher frequencies use more current.

In **normal power mode** (the default configuration), typical current, is calculated as shown below.

$$I\,[mA] = 2.05 \cdot f_s\,[kHz]$$

For example, at a sampling frequency of 1,000 samples per second, f_s = 1 kHz and I = 2.05 mA. At 10 samples per second, I = 20.5 µA. In **low power mode**, typical current, is calculated as shown below.

$$I\,[\mu A] = 260 \cdot f_s\,[kHz]$$

For example, at a sampling frequency of 1,000 samples per second, f_s = 1 kHz and I = 260 µA. At 10 samples per second, I = 2.6 µA.

DETERMINING THE MAGNETIC AIRGAP

With AGC enabled (default configuration), the relative airgap between magnet and iC-TW11 can be determined by reading the Hall array gain. This is useful for verifying that the magnet has the right distance from iC-TW11, or to implement a button push/knob turn application to determine when the button is pushed. The four most significant bits of the 5-bit gain value are available in ANGLE register for this purpose. The full 5-bit gain value can be read from the GAIN register (see page 15). Because the LSB is missing, the gain value in ANGLE Register is half the value in GAIN Register.

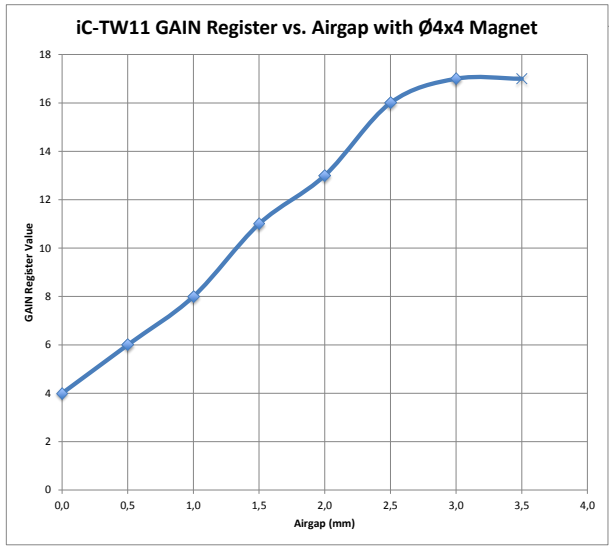


Figure 7: Typical Hall array gain vs. airgap

For example, the typical relationship between Hall array gain and magnetic airgap for the Ø4x4 mm magnet used on the iC-TW11_1C demo board is shown in figure 7.

Notice that the gain saturates at larger gaps before an ADC Underflow condition (X) is indicated at a gap of 3.5 mm.

BUSSING MULTIPLE ICs

Multiple iC-TW11 slaves can be used with a single SPI host in a traditional SPI bus connection. In this case, SCLK, SI, and SO on all devices are connected together and each device uses a separate slave select (xSS) signal, as shown in Figure 8.

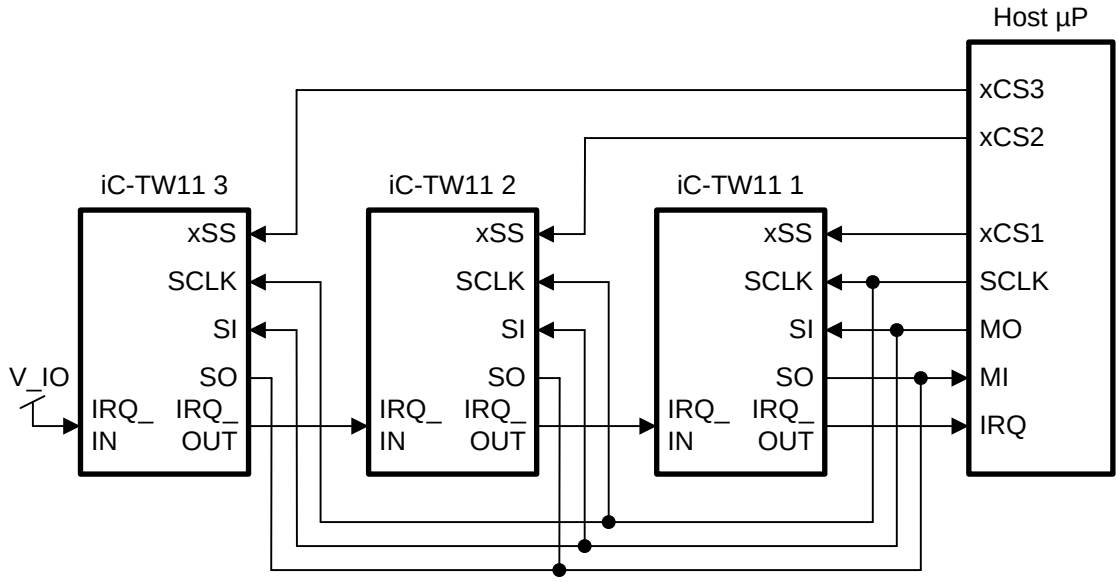


Figure 8: SPI bus connection of multiple iC-TW11s

In operation, the host initiates a sample of one of the iC-TW11s by activating the appropriate chip select (xCS) and sending the appropriate read register command. The host then either waits the appropriate amount of time (see Figure 5 Page 16) or waits for the interrupt request (IRQ) to be received to read the sampled angle. In this case, the interrupt logic in all iC-TW11s must be set to **OR** to ensure that the host receives an interrupt request when any of the TW11 asserts its IRQ_OUT. This is accomplished by setting the interrupt mode bit in the CONFIG register (CONFIG.imod = 1). See USING INTERRUPTS on Page 19 for more information.

Note that in a bussed configuration, only one iC-TW11 can be active at a time: the host must activate only one chip select at a time. Because of this, simultaneous sampling of multiple iC-TW11s in a bussed configuration is only possible using the SAMPLE input.

CHAINING MULTIPLE ICs

Multiple iC-TW11 slaves can also be chained together using a single SPI host. In this case, all devices are accessed together as a group and all data is read back together by the host in an extended response packet.

In a chained configuration, SCLK and xSS on all devices are connected together while SI and SO, and IRQ_IN and IRQ_OUT are linked from one device to the next, as shown in Figure 9.

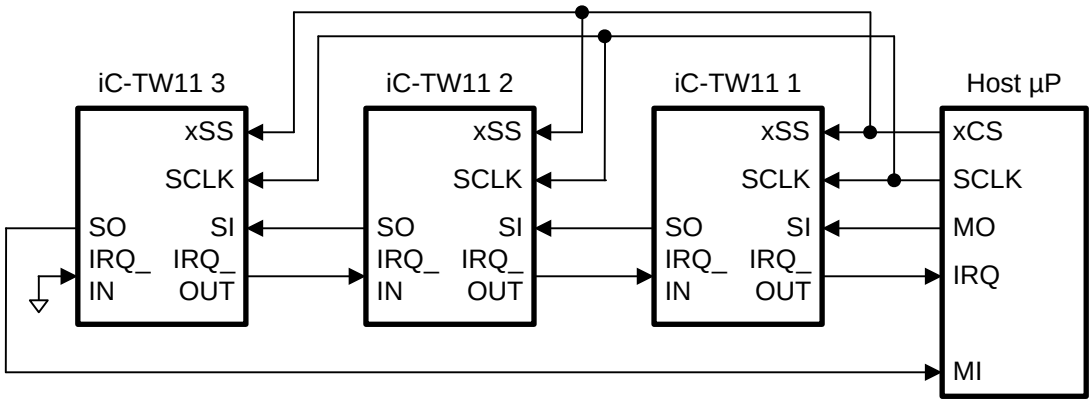


Figure 9: Chained connection of multiple iC-TW11s

In operation, the host initiates a sample of all of the iC-TW11s by activating the chip select output (xCS) and sending three consecutive read register commands by clocking 3 x 16 = 48 bits through the SI/SO chain. As long as the xSS input of the iC-TW11s is held low, data is shifted through the chained devices from SI to SO. After all commands have been loaded to the chained devices, the host deactivates xSS to execute the commands simultaneously. This extended packet communication structure is shown below.

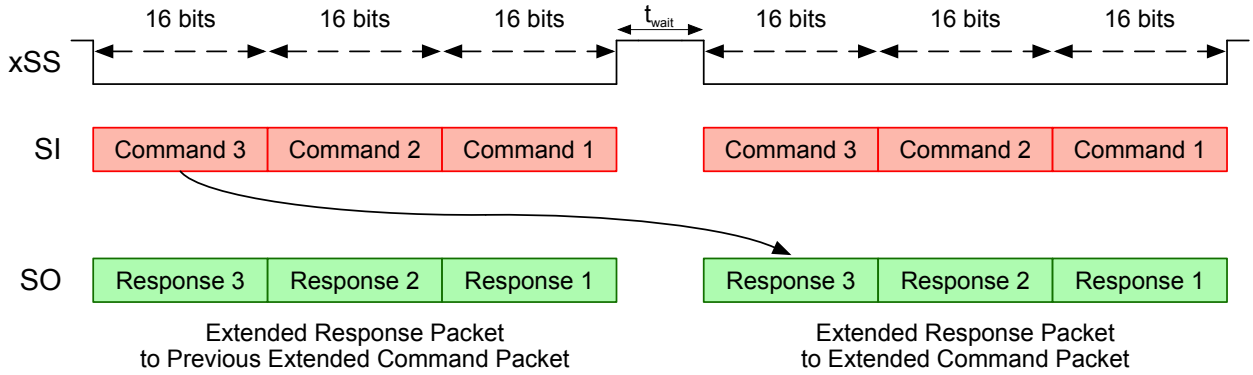


Figure 10: Extended communication packet structure with chained iC-TW11s

The host then either waits the appropriate amount of time (see Page 16) or waits for the interrupt request (IRQ) to be received to read the sampled angles as 48 consecutive bits over the SI/SO chain. In this case, the default interrupt logic of AND is used so that the host receives an interrupt request only when all the iC-TW11 slaves have completed sampling and conversion. See USING INTERRUPTS on Page 19 for more information.

DESIGN REVIEW: Function Notes

iC-TW11 D1		
No.	Function, Parameter/Code	Description and Application Notes
1	Supply Voltage V_CORE, V_IO	A leakage current of up to 100 µA can flow if xRST = low and V_IO < V_CORE.

Table 24: Notes on chip functions regarding iC-TW11 chip release D1.

REVISION HISTORY

Rel	Rel.Date	Chapter	Modification	Page
A1	14-06-11		Initial release	all

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-TW11	QFN16, 4 mm x 4 mm thickness 0.9 mm RoHS compliant		iC-TW11 QFN16-4x4
Evaluation Board	PCB, 80 mm x 60 mm		iC-TW11 EVAL TW11_1C
iC-TW11 GUI		Evaluation software for Windows PC	For download link refer to www.ichaus.com/tw11

For technical support, information about prices and terms of delivery please contact:

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