iC-HT

DUAL CW LASER DIODE DRIVER

preliminary

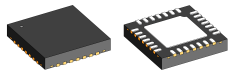
FEATURES

- Dual channel CW operation with up to 750 mA per channel
- Up to 1500 mA with both channels combined
- 2.8 V to 11 V power supply
- Operation with or without µController
- Individual enable input per channel
- Control loop accuracy better than 1%
- Internal programmable logarithmic monitor resistor
- Operating point setup with 10 bit logarithmic resolution
- ACC or APC mode individually configurable for each channel
- A/D converters for analog monitoring
- Serial programming interface (SPI or I^2C compliant)
- Configuration content verification and validation
- Programmable laser overcurrent protection
- Optimized for N-type laser diodes
- Low drop linear regulator for 3.3 V
- Low current standby mode
- Temperature monitor
- Temperature range -40 . . . 85 °C

APPLICATIONS

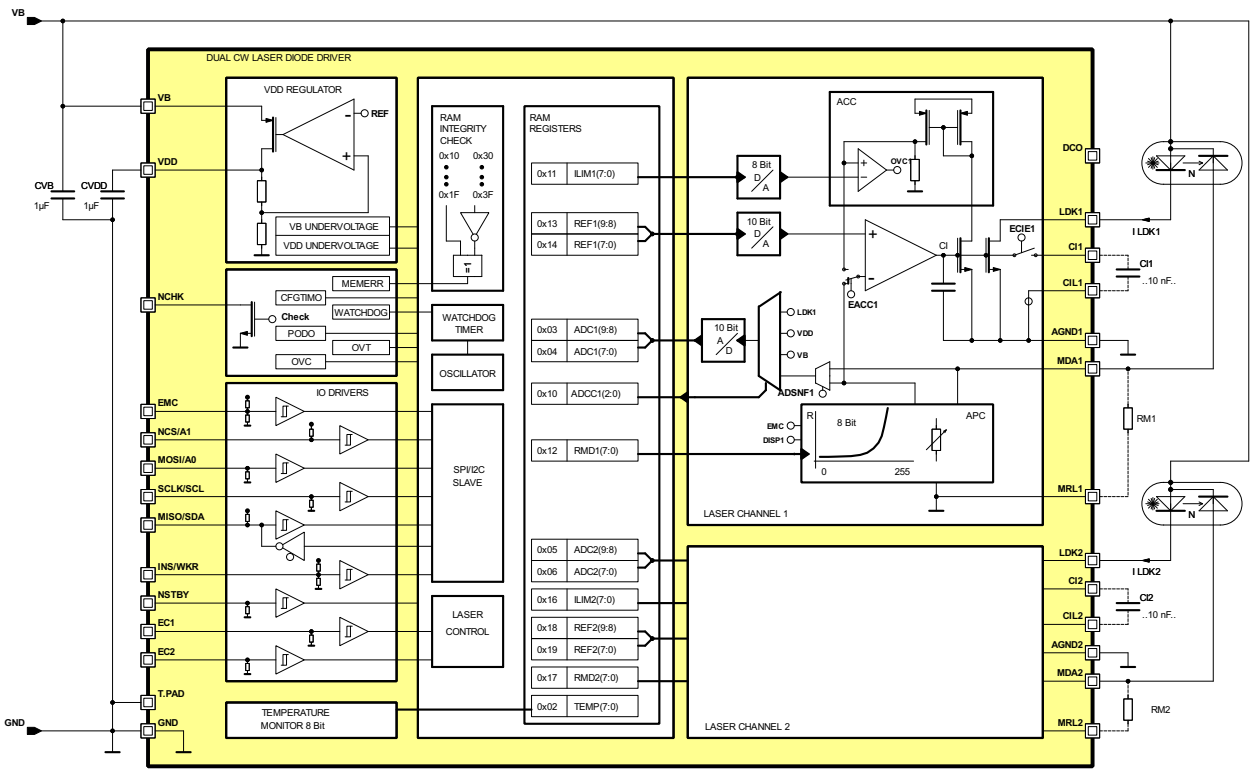
- Laser diode and LED modules
- CW N-/M-type laser diode drivers
- Embedded laser diode controllers
- Structured-light 3D illuminations
- Multiple laser diode control
- Optical amplification/pumping
- Safety related laser controllers

PACKAGES



QFN28 5 mm x 5 mm

BLOCK DIAGRAM



DESCRIPTION

Dual CW laser diode driver iC-HT can operate two individual laser diodes with up to 750 mA laser current depending on the heat dissipation. Each channel can be enabled independently. The laser diode driver can be controlled by an external microcontroller (MCU mode) or operate stand alone with pin/resistor configuration (iC-WK mode). In MCU mode, both channels can be combined for driving up to 1500 mA.

Each channel can be operated individually either in automatic current control (ACC) or automatic power control (APC). All parameters including the internal reference voltages are set via serial communication (I^2C or SPI). A 10 bit resolution D/A converter with logarithmic characteristic is used for setting the operating point. This allows an operating point resolution better than 1%.

In APC control, the monitor diode photocurrent is used to track the optically emitted power of the laser diode. The feedback for the laser diode driver is the voltage of the photocurrent at a monitor resistor. An 8 bit internal programmable logarithmic monitor resistor (PLR) or an external monitor resistor can be selected for closing the control loop. The PLR ranges from 100 Ω to 500 kΩ with a step width less than 5%.

In ACC control, the laser diode current can be set directly. Two current ranges are selectable.

iC-HT allows disabling the laser channels when an overcurrent threshold has been exceeded. The overcurrent threshold of each channel has 2 ranges and is programmable through an 8 bit linear D/A converter.

The temperature monitor measures the internal chip temperature. iC-HT disables the laser channels when overtemperature is detected.

A variety of voltages can be measured with a 10 bit A/D converter. The following voltages can be measured:

- V(LDKx)
- V(VDD)
- V(VB)
- V(MDAx)
- V(PLRx)

The DCO current output pin can control an external DC/DC converter. Controlling the DC/DC output voltage can optimize the power dissipation of the whole system e.g. to extend battery life.

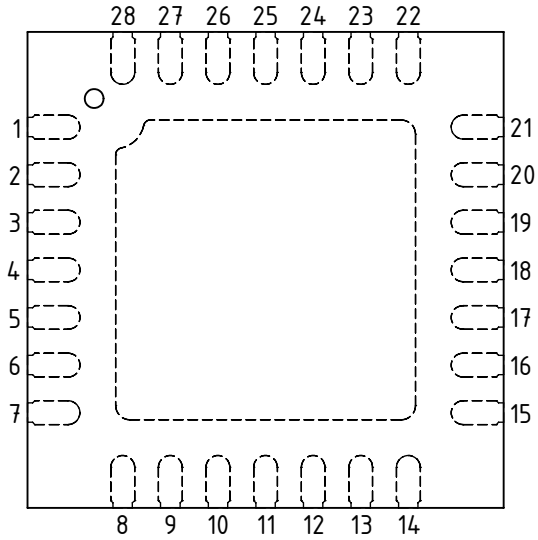
iC-HT in standby mode has a very low current consumption (< 10 µA) and does retain its configuration.

The device features for **safe operation**:

- Configuration verification
- Tri-state configuration pins
- Write protection in operating mode
- Safe default/startup state

PACKAGING INFORMATION QFN28 5 mm x 5 mm to JEDEC

PIN CONFIGURATION QFN28 5 mm x 5 mm (topview)



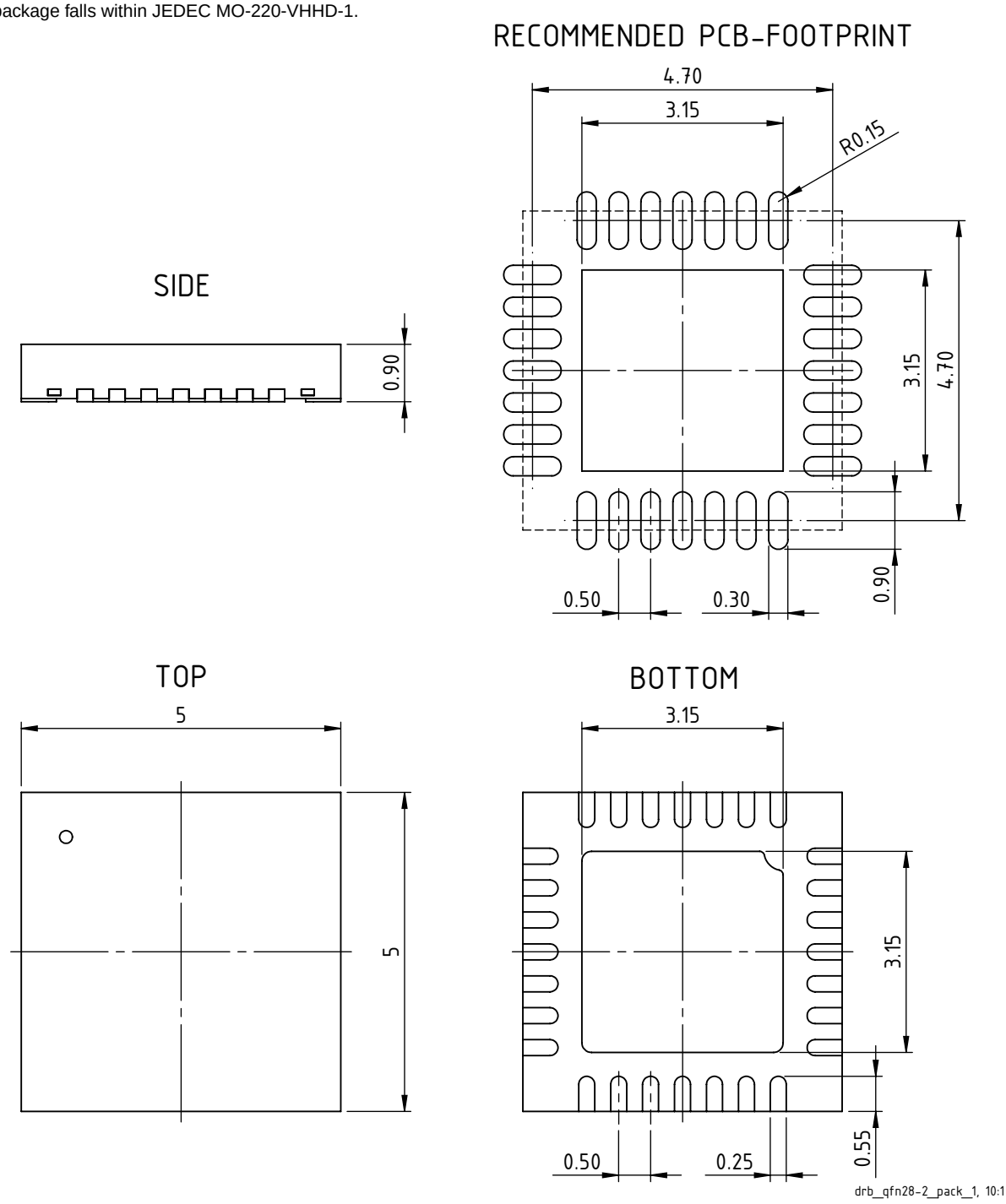
PIN FUNCTIONS

No.	Name	Function
1	LDK1	Laser Diode Cathode for channel 1
2	LDK1	Laser Diode Cathode for channel 1
3	AGND1	Analog Ground for channel 1
4	CI1	Integration Capacitor for channel 1
5	CIL1	Integration Capacitor for channel 1, low side
6	MDA1	Monitor Diode Anode for channel 1
7	MRL1	Monitor Resistor for channel 1, low side
8	EMC	Enable Microcontroller input
9	SCLK/SCL	SPI Clock / I^2C Clock
10	MISO/SDA	SPI Master In Slave OUT / I^2C Data
11	MOSI/A0	SPI Master Out Slave In / I^2C Address Bit 0
12	NCS/A1	Chip Select, active low / I^2C Address bit 1
13	EC1	Enable Channel 1 input
14	EC2	Enable Channel 2 input
15	MRL2	Monitor Resistor for channel 2, low side
16	MDA2	Monitor Diode Anode for channel 2
17	CIL2	Integration Capacitor for channel 2, low side
18	CI2	Integration Capacitor for channel 2
19	AGND2	Analog Ground for channel 2
20	LDK2	Laser Diode Cathode for channel 2
21	LDK2	Laser Diode Cathode for channel 2
22	GND	Ground
23	DCO	Digital Current Output
24	INS/WKR	I^2C or SPI selection input / Reference voltage selection in iC-WK mode
25	VDD	3.3 V output supply
26	VB	Power supply
27	NCHK	Error output, active low
28	NSTBY	Standby input, active low
TP		Thermal Pad (GND)

The *Thermal Pad* is to be connected to a *Ground Plane* (GND, AGND1. . . 2) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (iC HT label and coding is subject to change).

PACKAGE DIMENSIONS QFN28-5x5

All dimensions given in mm.
This package falls within JEDEC MO-220-VHHD-1.



ABSOLUTE MAXIMUM RATINGS

These ratings do not imply permissible operating conditions; functional operation is not guaranteed. Exceeding these ratings may damage the device.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VB	Voltage at VB		-0.3	11	V
G002	I(VB)	Current in VB		-20	50	mA
G003	VDD	Voltage at VDD		-0.3	5.5	V
G004	I(VDD)	Current in VDD		-20	1	mA
G005	V()	Voltage at CI1, CI2, EC1, EC2, MDA1, MDA2, EMC, SCLK/SCL, MISO/SDA, MOSI/A0, NCS/A1, DCO, INS/WKR, NCHK		-0.3	5.5	V
G006	I()	Current in CI1, CI2, EC1, EC2, MDA1, MDA2, EMC, SCLK/SCL, MISO/SDA, MOSI/A0, NCS/A1, DCO, INS/WKR, NCHK, NSTBY, CIL1, CIL2, MRL1, MRL2		-20	20	mA
G007	I(LDK)	Current in LDK1, LDK2	DC current	-20	900	mA
G008	V()	Voltage at LDK1, LDK2, NSTBY		-0.3	11	V
G009	V()	Voltage at AGND1, AGND2		-0.3	1	V
G010	I(AGND)	Current in AGND1, AGND2	DC current	-900	1	mA
G011	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G012	Tj	Operating Junction Temperature		-40	125	°C
G013	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VB = 2.8 . . . 11 V (referenced to GND)

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient	Mounted on PCB		25		K/W
T03	RthjTP	Thermal Resistance Chip/Thermal Pad			4		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = 2.8 . . . 11 V (referenced to GND), Tj = -40 . . . 125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device Functionality and parameters beyond the operating conditions (with reference to independent voltage supplies, for instance) are to be verified within the individual application using FMEA methods.							
001	VB	Permissible Supply Voltage	Referenced to GND	2.8		11	V
002	I(VB)	Standby Current at VB	V(NSTBY) $\leq$ 0.4 V			10	µA
003	I(VB)	Supply Current at VB	No load, EC1, EC2, NSTBY = hi			5	mA
004	V(VB)on	Turn-on threshold	Increasing VB	1.7		2.7	V
005	V(VB)off	Turn-off threshold	Decreasing VB	1.6		2.6	V
006	V(VB)Hys	Power-on hysteresis		20		250	mV
007	V(VDD)on	Turn-on threshold	Increasing VDD	1.7		2.4	V
008	V(VDD)off	Turn-off threshold	Decreasing VDD	1.6		2.3	V
009	V(VDD)Hys	Power-on hysteresis		20		250	mV
010	V(VB)INITR	RAM memory reset during Stand-By	NSTBY = lo	0.85		1.4	V
011	Rgnd()	Resistor to GND at MRL1, MRL2				20	Ω
012	Ragnd()	Resistor to AGNDx at CILx				20	Ω
013	Vc()lo	Clamp Voltage lo at VB, VDD, NCHK, EMC, NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, INS/WKR, NSTBY, EC1, EC2, DCO, LDK1, LDK2, CI1, CIL1, CI2, CIL2, AGND1, AGND2, MDA1, MDA2	I() = -10 mA	-1.6		-0.3	V
Laser Driver LDKx, CIx, MDAx							
101	Vs(LDK)lo	Saturation Voltage lo at LDK	I(LDKx) = 750 mA			0.7	V
102	V(LDKSAT)	LDKx saturation detection threshold	RLDKSx = 00 RLDKSx = 01 RLDKSx = 10 RLDKSx = 11	0.35 0.55 0.85 1.05	0.5 0.7 1 1.2	0.65 0.85 1.15 1.35	V V V V
103	Idc(LDK)	Permissible DC Current at LDKx				750	mA
104	Ileak(LDK)	LDKx leakage current	V(LDKx) = 11 V			10	µA
105	C(CI)	Possible capacitor at CI1, CI2	ECIE = 0, EMC = hi	0			µF
106	I(CI)	Charge Current at CI1, CI2	V(CI) = 0 V, EC1, EC2 = hi, ECIEx = 1 COMP = 111	-220		-30	µA
107	I(LDK)max	Laser overcurrent shutdown threshold	V(LDKx) = 0.7 V . . . VB - 1.5 V ILIMx(7:0) = 0x00, RACCx = 0 ILIMx(7:0) = 0xFF, RACCx = 0 ILIMx(7:0) = 0x00, RACCx = 1 ILIMx(7:0) = 0xFF, RACCx = 1	 0 750 0 80		 25 1400 3.2 175	 mA mA mA mA
108	Δ I(LDK)	Shutdown threshold resolution	RACCx = 0 RACCx = 1	2.8 0.3	4 0.5	5.2 0.8	mA mA
109	tovc	Time to overcurrent shutdown	Laser current decreased 10%	1		5	µs
110	V(MDA)	Voltage at MDA1, MDA2	Closed control loop EC1, EC2 = hi EMC = lo, INS/WKR = lo EMC = lo, INS/WKR = hi	 225 455	 250 500	 275 545	 mV mV
111	Ten	Time to laser enabled	NSTBY lo $\rightarrow$ hi, no load at VDD, V(VDD) 0 to 90 %, CVDD = 1 µF, EMC = lo			1.3	ms
112	Tci	Time to light	NSTBY = hi, ECIE = 0, COMP = 010, light off to 80 % target value			300	µs
113	Tcio	Time to target light	Light from 80 % to 99 % target value			4700	µs

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = 2.8 . . . 11 V (referenced to GND), Tj = -40 . . . 125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
114	Idc(LDK)	LDKx ACC mode current	EC1, EC2, EMC = hi, EACCx = 1, V(LDKx) = 0.7 V . . . VB - 1.5 V REFx(9:0) = 0x000, RACCx = 0 REFx(9:0) = 0x3FF, RACCx = 0 REFx(9:0) = 0x000, RACCx = 1 REFx(9:0) = 0x3FF, RACCx = 1	 50 650 5 70	 82 750 10 113	 120 1400 15 160	 mA mA mA mA
115	Tk	Temperature coefficient ACC mode		-1500	-500	0	ppm/K
Programmable Resistor							
201	Rmda	Resistor at MDAx pin	RMDx(7:0) = 0xF0 . . . 0xFF, DISPx = 0 RMDx(7:0) = 0x00 . . . 0x0F, DISPx = 0	350 0.154	500 0.220	650 0.286	kΩ kΩ
202	Tk	Temperature coefficient		-1500	-500	0	ppm/K
203	Δ R	Resistor increment	$\Delta R = \frac{R(n+1)-R(n)}{R(n)}$	2	3.3	5	%
204	Ileak(MDA)	MDAx leakage current	DISPx = 1	-1		1	µA
D/A Converter							
301	R(DAC)	D/A Converter Resolution				10	bit
302	Δ V	Percentual voltage increments	$\Delta V = \frac{V(n+1)-V(n)}{V(n)}$	0.1	0.235	0.5	%
303	V(DAC)	D/A Converter	REFx(9:0) = 0x000 lowest value REFx(9:0) = 0x3FF highest value	0.09 1.00	0.10 1.10	0.12 1.25	V V
Check Output NCHK							
401	Vs()lo	Saturation Voltage lo at NCHK	I(NCHK) = 1.0 mA			0.4	V
402	Isc()lo	Short Circuit Current lo at NCHK	V(NCHK) = 0.4 . . . 3.3 V	9		33	mA
403	Ilk()	Leakage Current at NCHK	NCHK = 1; V(NCHK) = 0 . . . 5.5 V	 -1		 1	 µA
Series Regulator Output VDD							
501	V(VDD)	Regulated output voltage	VB = 3.7 . . . 8 V, I(VDD) = -10 . . . 0 mA NSTBY = hi	3		3.5	V
502	V(VB,VDD)	Voltage Drop between VB and VDD	VDD unregulated, I(VDD) = -10 . . . 0 mA NSTBY = hi		100	400	mV
503	C(VOUT)	Capacitor at VDD	Ri(C) < 1 Ω	1		3.3	µF
504	Tvdd	Settling time VDD	NSTBY lo → hi, no load at VDD, V(VDD) 0 to 90 % CVDD = 1 µF			1	ms
Digital inputs							
601	Vt()hi	Input Threshold Voltage hi at EMC, NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, INS/WKR, NSTBY, EC1, EC2				2	V
602	Vt()lo	Input Threshold Voltage lo at EMC, NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, INS/WKR, NSTBY, EC1, EC2	VB > 3 V VB = 2.8 V	0.7 0.6			V V
603	Vt()hys	Hysteresis at EMC, NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, INS/WKR, NSTBY, EC1, EC2	Vt()hys = Vt()hi - Vt()lo	100			mV
604	Ipd()	Pull-Down Current at MOSI/A0, EC1, EC2	V() = 0.4 V . . . VDD	1		50	µA
605	Ipd()	Pull-Down Current at NSTBY	V() = 0.4 V . . . VB	1		50	µA
606	Rpu()	Pull-Up Resistor at SCLK/SCL, NCS/A1		80	150	260	kΩ
607	Rpu()	Pull-Up Resistor at MISO/SDA	EMC = hi, INS/WKR = lo EMC = hi, INS/WKR = hi	8 53	20 100	50 174	kΩ kΩ
608	Er()	Safe enable threshold voltage at EMC, INS/WKR	Rising Falling	52 30	54 32	56 34	% VDD % VDD

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = 2.8 . . . 11 V (referenced to GND), Tj = -40 . . . 125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
609	Voc()	Open Circuit Voltage at EMC, INS/WKR		39	41	43	% VDD
610	Ri()	Internal Resistance at EMC, INS/WKR		170	250	330	kΩ
611	Isc()lo	Short Circuit current lo at MISO/SDA	INS/WKR = lo, V(MISO/SDA) = 5.5 V	-40		-4	mA
612	Vs()lo	Saturation Voltage lo at MISO/SDA	INS/WKR = lo, I(MISO/SDA) = 2 mA			0.4	V
A/D Converter							
701	Ton	Converter initialization time	ADCCx(2) changes from 0 to 1 LDKx, VDD or VB measurements			500	µs
702	Tconv	Conversion time				140	µs
703	R(ADC)	A/D Converter Resolution				10	bit
704	RAC	Relative Accuracy		-1		+1	LSB
705	VZS()	Zero Scale Voltage	ADCx(9:0) = 000h		0		V
706	VFS()	Full Scale Voltage	ADCx(9:0) = 3FFh	1.0	1.1	1.2	V
707	MDAM	MDAx Measurement	MDAx = 0.5 V, ADCCx(2:0) = 100, ADSNFx = 0	372	465	558	LSB
708	VDDM	VDD Measurement	VDD = 3.3 V, ADCCx(2:0) = 110	312	390	468	LSB
709	VBM	VB Measurement	VB = 8 V, ADCCx(2:0) = 101	744	930	1023	LSB
710	LDKM	LDKx Measurement	LDKx = 8 V, ADCCx(2:0) = 111	744	930	1023	LSB
Overtemperature							
B01	Toff	Overtemperature Shutdown	Rising temperature	130		170	°C
B02	Ton	Overtemperature Release	Falling temperature	120		165	°C
B03	Thys	Hysteresis	Toff – Ton	3			°C
Temperature Monitor							
C01	Trange	Temperature Measurement Range		-40		125	°C
C02	Tresol	Temperature Measurement Resolution			1		°C
C03	Reading	Temperature Value Ranges	Tj = 125 °C Tj = -40 °C	160 0		190 15	digits digits
DCO Output							
D01	Isc()hi	DCO Output Current	V(VDD) = 3...3.5 V, V(DCO) < 1.4 V, RDCO = 0x3F	-175	-130	-85	µA
D02	Ileak	Leakage Current at DCO	RDCO = 0x00 or NSTBY = lo, V(DCO) = 0 . . . 5.5 V	-1		1	µA
D03	I(DCO)LSB	I(DCO) Resolution	V(DCO) < 1.4 V	1.3	2	2.7	µA
Oscillator							
E01	Fosc	Oscillator Frequency	NSTBY = hi	100	200	400	kHz
E02	T(cfgtimo)	Configuration Mode Timeout	MODE(1:0) = 10	40	82	164	ms
E03	tWDT	Watchdog Timeout	NSTBY = hi	20		120	µs

OPERATING REQUIREMENTS: SPI and I²C Interface

Operating Conditions: VB = 2.8 . . . 11 V , Tj = -40 . . . 125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI / I²C Interface Timing						
I001	tsCCL	Setup Time: NCS/A1 hi → lo before SCLK lo → hi	INS/WKR = lo	20		ns
I002	tsDCL	Setup Time: MOSI/A0 stable before SCLK/SCL lo → hi	INS/WKR = lo	20		ns
I003	thDCL	Hold Time: MOSI/A0 stable after SCLK/SCL lo → hi	INS/WKR = lo	20		ns
I004	tCLh	Signal Duration SCLK/SCL hi	INS/WKR = lo	50		ns
I005	tCLl	Signal Duration SCLK/SCL lo	INS/WKR = lo	50		ns
I006	thCLC	Hold Time: NCS/A1 lo after SCLK/SCL hi → lo	INS/WKR = lo	20		ns
I007	tCSh	Signal Duration NCS/A1 hi	INS/WKR = lo	50		ns
I008	tpCLD	Propagation Delay: MISO/SDA stable after SCLK/SCL hi → lo	INS/WKR = lo, V(VDD) > 3 V, Cload = 10 pF, no external pull-up	0	30	ns
I009	tHIZ	MISO to HIZ delay	INS/WKR = lo	0	25	ns
I010	f(SCLK)	SPI clock frequency			10	MHz
I011	f(SCL)	I²C clock frequency			400	kHz

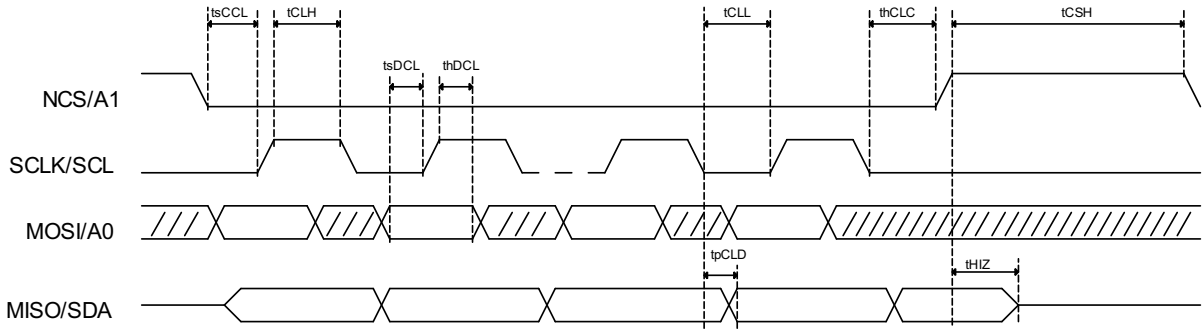


Figure 1: SPI interface timing

OPERATING AND STANDBY MODES

iC-HT operating modes are selected by the pins EMC and INS. These pins are intended to be static and should not be changed during operation to avoid misconfiguration or unintended operation. It is recommended to tie the pins EMC and INS to VDD or GND. Floating pins EMC and INS/WKR are detected as faulty configuration and signaled at NCHK.

iC-WK mode
In iC-WK mode the iC-HT operates as an Automatic Power Control (APC) laser controller, similar to iC-Haus iC-WK/iC-WKL , iC-WKM and iC-WKN. iC-WK mode is set by pin configuration and the external monitor resistor. Pin EMC is set to lo and pin INS/WKR selects the reference voltage:

- INS/WKR = hi for 0.5 V reference voltage, similar to iC-WK, iC-WKL, iC-WKN.
- INS/WKR = lo for 0.25 V reference voltage, similar to iC-WM.

Floating pins EMC and INS/WKR are detected as faulty configuration and signaled at NCHK.

MCU mode
In microcontroller unit (MCU) mode, iC-HT features two control modes: automatic power control (APC) and automatic current control (ACC). Pin EMC is set to hi and pin INS/WKR selects the serial communication interface protocol. Selection of the communication protocol is achieved through pin INS/WKR:

- INS/WKR = hi for I2C.
- INS/WKR = lo for SPI.

Floating pins EMC and INS/WKR are detected as faulty configuration and signaled at pin NCHK. Any input interface could be enabled if EMC or INS pins are open. Comunication with the chip might be possible but laser cannot be switched on. This situation is only signaled at pin NCHK, which would remain low as long as any of the EMC or INS pins are unconnected. MCU must monitor the status of the pin NCHK to get all the status information of the chip.

Standby Mode
iC-HT in standby mode has a very low current consumption (< 10 µA) and does retain its configuration. Standby mode will not reset the internal RAM.

In order to exit standby mode, pin NSTBY must be set to hi (e.g. VB). VDD is switched off in standby mode and can not be used to exit standby mode.

VB, NSTBY and LDKx withstand voltages up to 11 V, whereas the remaining input pins operate up to 5.5 V and do have high impedance at standby mode.

Information on timing after waking up from standby mode can be found on page 36.

LASER DIODE/LED TYPES AND OPERATION MODES

For APC operation a monitor diode is required. This operation is possible in microcontroller unit (MCU) mode and in the iC-WK mode.

iC-HT can operate in APC two types of laser diodes/LEDs with monitor diodes:

- N-Type laser diodes
- M-Type laser diodes

In automatic current control (ACC) operation there is no monitor diode and any diode can be operated in microcontroller unit (MCU) mode.

All operations are possible with laser diodes (LDs) or light emitting diodes (LEDs). In the following text we do not differ between laser diodes (LDs) and light emitting diodes (LEDs).

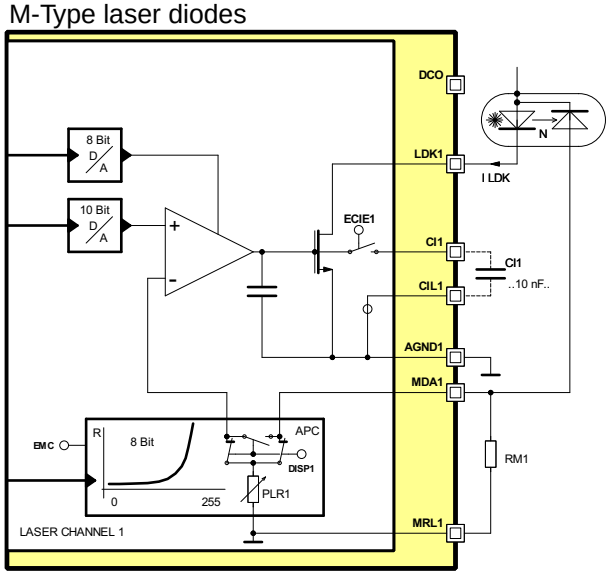


Figure 2: iC-HT with N-type laser diode

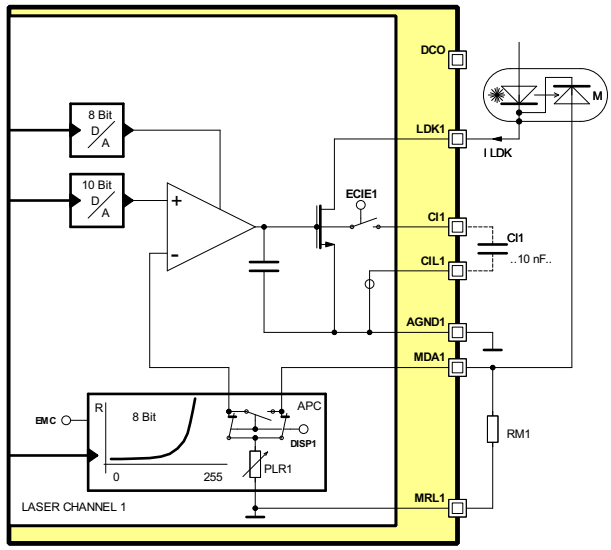


Figure 3: iC-HT with M-type laser diode

iC-WK MODE

Setting pin EMC = lo configures iC-HT for iC-WK mode. EMC pin must be set to GND.

In iC-WK mode both channels operate in APC mode. The internal programmable logarithmic monitor resistors are disabled, therefore connection of external resistors at pins MDAx is required.

The APC reference can be set to two different values by means of pin INS/WKR, as it is explained in table 5, and the overcurrent threshold is set to its maximum value of 750 mA (cf. *Electrical Characteristics No. 107*). In case of overcurrent, the respective channel is disabled. For re-enabling the channel, the corresponding ECx pin must be set lo and then back hi.

Reference Voltage in iC-WK mode		
INS/WKR	**Reference Voltage**	**similar to**
Lo	0.25 V	iC-WKM
Hi	0.5 V	iC-WK, iC-WKL, iC-WKN

Table 5: Reference selection (cf. *Electrical Characteristics No. 110*)

External CI capacitors must be added in this operation mode at pins CIx and CILx. Figure 4 shows an example in iC-WK mode using an N-type laser diode, where 0.5 V reference is selected. Figure 5 presents the same configuration with an M-type laser diode.

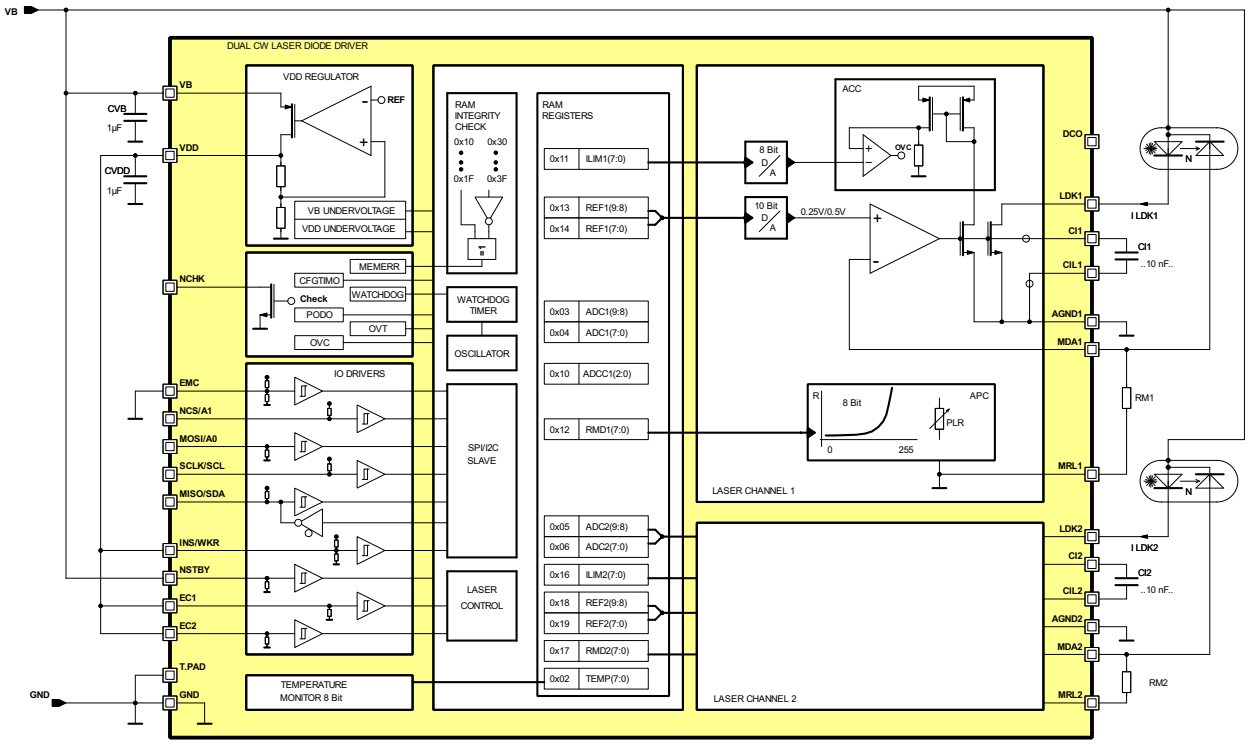


Figure 4: iC-HT in iC-WK mode with N-type laser diode

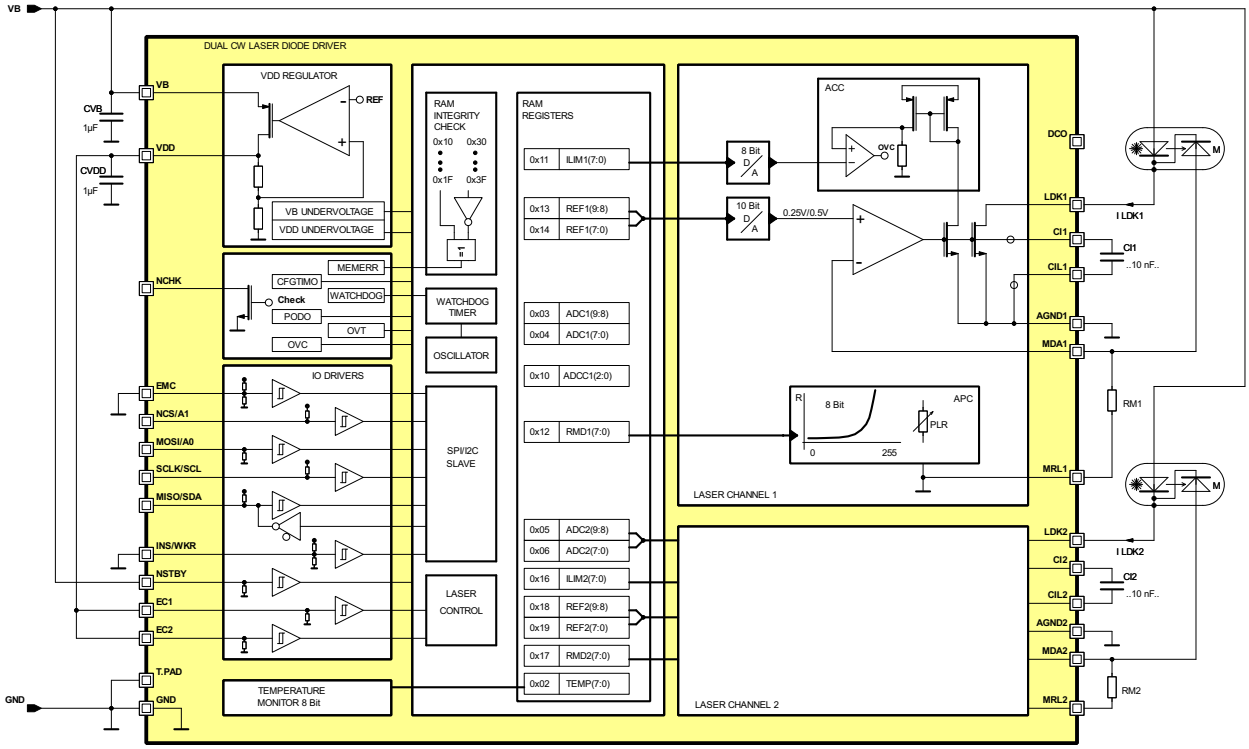


Figure 5: iC-HT in iC-WK mode with M-type laser diode

In the configuration from figures 4 and 5 pin NSTBY is connected to VB. This is required to force iC-HT leaving standby mode and starting normal operation, as the pin includes an internal pull-down resistor.

Laser channel enabling

Setting pins EC1, EC2 to hi enables the corresponding channels. In order to ensure safe operation of iC-HT, several events automatically disable both output channels:

- Pins INS/WKR or EMC left unconnected (INSOPEN, EMCOPEN), iC-HT enters error mode and the laser channels cannot be enabled.
- Supply power-down either at VB (PDOVB) or VDD (PDOVDD), the laser channels are unconditionally disabled during the power down event.
- Overcurrent (OVC) or overtemperature (OVT), laser channels are switched off. Cycling pins EC1, EC2 or a power-up is required to switch on the laser again.

MICROCONTROLLER MODE

Setting pin EMC to hi configures iC-HT for microcontroller mode (MCU mode). EMC pin must be set using a pull-up resistor or directly short-circuited to VDD pin. Several parameters can be configured through a microcontroller via I^2C or SPI communication. More information about the serial communication interface can be found on page 23.

The configuration of the internal parameters of iC-HT must be done in configuration mode. In this mode, the configuration memory can be written and read back without changing the previous configuration state of iC-HT. Once the configuration is considered as valid, iC-HT can be switched to operation mode. These two modes are configured by the MODE register. If the time in configuration mode exceeds the Configuration Mode Timeout (cf. *Electrical Characteristics No. E02*), both channels will be switched off. More information on page 34.

Each individual channel can be enabled by setting pin ECx to hi. Setting register bits DISCx to 1 disables the corresponding channel. If either pin ECx is lo or register bits DISCx is 1, the corresponding channel is disabled.

DISC1	Addr. 0x10; bit 3	R/W 1
0	Channel 1 can be enabled by pin EC1	
1	Channel 1 cannot be enabled by pin EC1	

Table 6: Disable channel 1

DISC2	Addr. 0x15; bit 3	R/W 1
0	Channel 2 can be enabled by pin EC2	
1	Channel 2 cannot be enabled by pin EC2	

Table 7: Disable channel 2

Different voltages can be measured using a 10 bit A/D converter with two resolutions. The following internal voltages can be measured:

- V(LDKx) up to 8 V with 8.6 mV resolution
- V(VDD) up to 8 V with 8.6 mV resolution
- V(VB) up to 8 V with 8.6 mV resolution
- V(MDAx) up to 1 V with 1.075 mV resolution
- V(PLRx) up to 1 V with 1.075 mV resolution

The register bits ADCCx select the signal measured with the 10 bit A/D converter.

ADCC1(2:0)	Addr. 0x10; bit 7:5	R/W 000
0xx	Disabled	
100	V(MDA1), ADSNF1 = 0	
100	V(PLR1), ADSNF1 = 1	
101	V(VB)	
110	V(VDD)	
111	V(LDK1)	

Table 8: ADC channel 1 source selection

ADCC2(2:0)	Addr. 0x15; bit 7:5	R/W 000
0xx	Disabled	
100	V(MDA2), ADSNF2 = 0	
100	V(PLR2), ADSNF2 = 1	
101	V(VB)	
110	V(VDD)	
111	V(LDK2)	

Table 9: ADC channel 2 source selection

With ADCCx(2:0) = 100, the signal to the A/D converter is selected by register bit ADSNFx. With ADSNFx = 1 the measuring point to the A/D converter is the internal sense node of the internal programmable logarithmic monitor resistor (PLR). With ADSNFx = 0 the sensing point is connected directly to MDAx pin.

ADSNF1	Addr. 0x1A; bit 2	R/W 0
0	ADC measurement pin MDA1 (force)	
1	ADC measurement PLR1 (sense)	

Table 10: ADC channel 1 sense/force selection

ADSNF2	Addr. 0x1A; bit 6	R/W 0
0	ADC measurement pin MDA2 (force)	
1	ADC measurement PLR2 (sense)	

Table 11: ADC channel 2 sense/force selection

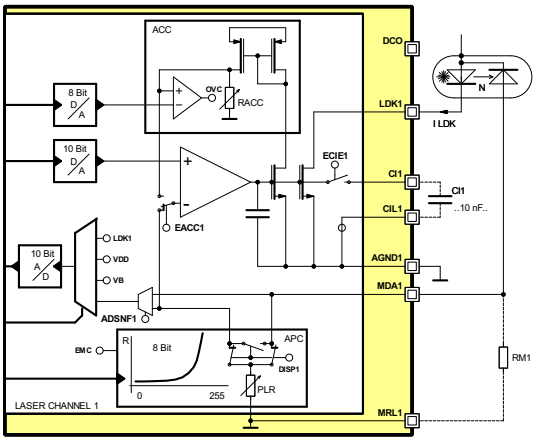


Figure 6: Channel 1 schematic

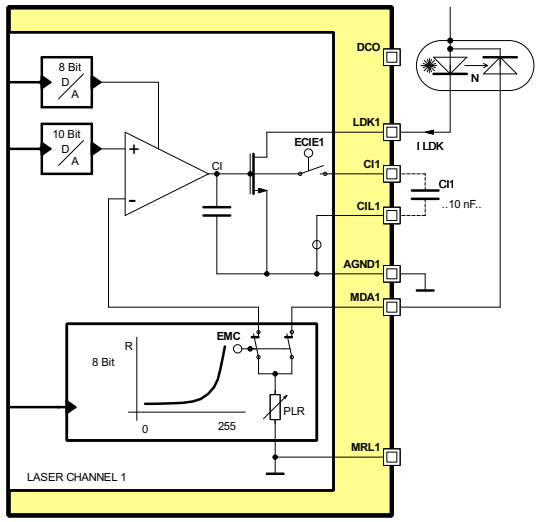


Figure 7: APC mode simplified

Two different control modes can be configured independent for each channel: automatic power control (APC) and automatic current control (ACC). In both modes a 10 bit logarithmic D/A converter sets the reference voltage and an 8 bit programmable D/A converter configures the overcurrent threshold.

APC (Automatic Power Control) mode
In APC mode the laser power is controlled. The monitor diode current is used as feedback in the laser power control loop. APC mode is selected by setting EACCx register bit to 0.

EACC1	Addr. 0x10; bit 0	R/W 0
0	APC mode enabled for channel 1	
1	ACC mode enabled for channel 1	

Table 12: APC/ACC in channel 1

EACC2	Addr. 0x15; bit 0	R/W 0
0	APC mode enabled for channel 2	
1	ACC mode enabled for channel 2	

Table 13: APC/ACC in channel 2

An example of APC with default configuration is shown in figure 7.

An internal 8 bit programmable logarithmic monitor resistor (PLR) can be used in APC mode. In APC mode it is also possible to use an external monitor resistor connected to pin MDAx. If register bit DISPx is 0, the PLR is present. If DISPx is 1, the PLR is disabled and an external monitor resistor must be used.

DISP1	Addr. 0x10; bit 2	R/W 0
0	PLR enabled for channel 1	
1	PLR disabled for channel 1	

Table 14: Disable PLR channel 1

DISP2	Addr. 0x15; bit 2	R/W 0
0	PLR enabled for channel 2	
1	PLR disabled for channel 2	

Table 15: Disable PLR channel 2

Both programmable logarithmic monitor resistors (PLR) feature a wide logarithmic resistor range from 100 Ω to 500 kΩ, in steps of typically 3.3%. This covers a wide range of monitor currents. More information about the PLR can be found on page 25.

For fine-tuning the optical power, the reference voltage can be set with a 10 bit logarithmic D/A converter, which is configurable through the register REFx. This converter has a voltage range that goes typically from 0.1 V to 1.1 V, allowing an operation resolution of typically 0.235%. More information on the logarithmic D/A converter can be found on page 26.

For calculating the minimum value of Imon, Vref(0x00, max value) (cf. *Electrical Characteristics No. 303*) and Rmda(RMDx = 0xFF, min value) (cf. *Electrical Characteristics No. 201*) are used.

$Imon(min) = \frac{Vref(0x000,max)}{Rmda(RMDx=0xFF,min)} = \frac{0.11}{350000} = 0.31\,uA$

It is not recommended to configure iC-HT to have such small Imon values, otherwise the leakage current at MDAx may have an influence (cf. *Electrical Characteristics No. 204*), especially at high temperatures. To avoid this, Imon should be much greater than the leakage current.

For calculating the maximum value of Imon, Vref(0x3FF, min value) (cf. *Electrical Characteristics No. 303*) and Rmda(RMDx = 0x00, max vaule) (cf. *Electrical Characteristics No. 201*) are used. The following formula can to be used for calculating Rmda(RMDx = 0x00, max value):

$Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$, n from 0 to 255

$Rmda(RMDx = 0x00, max) = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{16}$

$286 = Rmd_0(1 + \frac{3.3}{100})^{16}$

$Rmd_0 = 170\Omega$

Therefore:

$Imon(max) = \frac{Vref(0x3FF,min)}{Rmd_0} = \frac{1.00}{170} = 5.88\,mA$

Any other Imon value can be calculated using Rmd formula above. Due to its logarithmic characteristic, the steps between two consecutive values is kept within 3.3 % typical value.

The programmable overcurrent shutdown can be set to protect the laser by disabling the channel. The overcurrent threshold is configurable in two different ranges. The range is selected through register bit RACCx. If RACCx = 1, the overcurrent threshold is in the low range, up to 90 mA. If RACCx = 0, the overcurrent threshold is in the high range, up to 750 mA (cf. *Electrical Characteristics No. 107*).

RACC1	Addr. 0x1A; bit 0	R/W 0
0	Current range high for channel 1	
1	Current range low for channel 1	

Table 16: RACC1 current range configuration channel 1

RACC2	Addr. 0x1A; bit 4	R/W 0
0	Current range high for channel 2	
1	Current range low for channel 2	

Table 17: RACC2 current range configuration channel 2

In each range, the particular overcurrent threshold value can be set in register ILIMx. The regulator does not differ the two current ranges in APC.

ILIM1	Addr. 0x11; bit 7:0	R/W 0xFF
0x0A	Channel 1 overcurrent threshold set to minimum current	
...	Channel 1 overcurrent threshold set to $Ilim = (\Delta I(LDK) \cdot n)$, n from 10 to 255	
0xFF	Channel 1 overcurrent threshold set to maximum current	

Table 18: Overcurrent threshold configuration channel 1

ILIM2	Addr. 0x16; bit 7:0	R/W 0xFF
0x0A	Channel 2 overcurrent threshold set to minimum current	
...	Channel 2 overcurrent threshold set to $Ilim = (\Delta I(LDK) \cdot n)$, n from 10 to 255	
0xFF	Channel 2 overcurrent threshold set to maximum current	

Table 19: Overcurrent threshold configuration channel 2

An overcurrent event can be simulated using SOVCx. If SOVCx = 1, the corresponding overcurrent error bit OVCx will be set to 1, the error will be signaled at NCHK and the corresponding laser channel will be disabled. The overcurrent error will remain forced until SOVCx = 0.

SOVC1	Addr. 0x1D; bit 5	R/W 0
0	No Overcurrent event at channel 1 is simulated.	
1	Overcurrent event at channel 1 simulated.	

Table 20: Simulate overcurrent channel 1

SOVC2	Addr. 0x1D; bit 6	R/W 0
0	No overcurrent event at channel 2 is simulated.	
1	Overcurrent event at channel 2 simulated.	

Table 21: Simulate overcurrent channel 2

ACC (Automatic Current Control) mode
In this mode, the laser diode current is controlled and no monitor diode is required. ACC mode is selected setting EACCx register bit to 1.

EACC1	Addr. 0x10; bit 0	R/W 0
0	APC mode enabled for channel 1	
1	ACC mode enabled for channel 1	

Table 22: APC/ACC in channel 1

EACC2	Addr. 0x15; bit 0	R/W 0
0	APC mode enabled for channel 2	
1	ACC mode enabled for channel 2	

Table 23: APC/ACC in channel 2

In ACC mode the internal programmable logarithmic monitor resistor (PLR) is not used. Instead the internal RACCx resistor is used to set the current. For fine-tuning the regulated current, the reference voltage can be set with a 10 bit logarithmic D/A converter, which is configurable through the register REFx. This converter has a voltage range that goes typically from 0.1 V to 1.1 V, allowing an operation resolution of typically 0.235%. More information on the logarithmic D/A converter can be found on page 26. Figure 8 shows an example of this configuration.

Two different current ranges can be set through register bit RACCx, with RACCx = 1 for up to 75 mA and with RACCx = 0 for up to 650 mA. The programmable overcurrent shutdown protects against over regulations during the laser power-on. Table 44 shows some typical current settings. For detailed limits, please refer to *Electrical Characteristics No. 114*

ACC typical current settings		
REFx	**RACCx=0**	**RACCx=1**
0x000	77.0 mA	9.06 mA
0x001	77.2 mA	9.08 mA
0x010	77.4 mA	9.10 mA
...	...	...
0x200	256.2 mA	30.14 mA
0x201	256.8 mA	30.21 mA
0x202	257.4 mA	30.28 mA
...	...	...
0x3FD	846.0 mA	99.53 mA
0x3FE	848.0 mA	99.77 mA
0x3FF	850.0 mA	100 mA

Table 24: ACC typical current settings

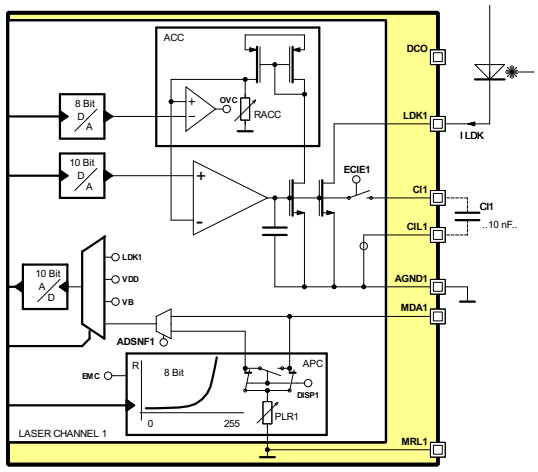


Figure 8: ACC mode simplified

RACC1	Addr. 0x1A; bit 0	R/W 0
0	Current range high for channel 1	
1	Current range low for channel 1	

Table 25: RACC1 configuration

RACC2	Addr. 0x1A; bit 4	R/W 0
0	Current range high for channel 2	
1	Current range low for channel 2	

Table 26: RACC2 configuration

In each range, the particular overcurrent threshold value can be set in register ILIMx. The regulator does differ the two current ranges in ACC.

ILIM1	Addr. 0x11; bit 7:0	R/W 0xFF
0x0A	Channel 1 overcurrent threshold set to minimum current	
...	Channel 1 overcurrent threshold set to $Ilim = (\Delta I(LDK) \cdot n)$, n from 10 to 255	
0xFF	Channel 1 overcurrent threshold set to maximum current	

Table 27: Overcurrent threshold configuration channel 1

ILIM2	Addr. 0x16; bit 7:0	R/W 0xFF
0x0A	Channel 2 overcurrent threshold set to minimum current	
...	Channel 2 overcurrent threshold set to $Ilim = (\Delta I(LDK) \cdot n)$, n from 10 to 255	
0xFF	Channel 2 overcurrent threshold set to maximum current	

Table 28: Overcurrent threshold configuration channel 2

An overcurrent event can be simulated using bit SOVCx. If SOVCx = 1, the corresponding overcurrent

error bit OVCx will be set to 1, the error will be signaled through NCHK and the corresponding laser channel will be disabled. The overcurrent error will remain forced until SOVCx = 0.

SOVC1	Addr. 0x1D; bit 5	R/W 0
0	No overcurrent event at channel 1 is simulated.	
1	Overcurrent event at channel 1 simulated.	

Table 29: Simulate overcurrent channel 1

SOVC2	Addr. 0x1D; bit 6	R/W 0
0	No overcurrent event at channel 2 is simulated.	
1	Overcurrent event at channel 2 simulated.	

Table 30: Simulate overcurrent channel 2

An external capacitor can be added in ACC mode in order to avoid oscillations as it is shown in figure 8. The external CIx must be enabled setting the ECIEx bit (Tables 93 and 106).

In ACC mode, the MDAx pin can be monitored through a 10 bit A/D converter. This can be used for measuring the laser light power, if a photodiode is connected to pin MDAx, as it is shown in figure 9. This allows adjusting the voltage reference in order to set the laser current and obtain the desired laser light power.

The internal programmable logarithmic monitor Resistor (PLR), if enabled (DISPx = 0), gives feedback for the current control through the 10 bit A/D converter. Register bit ADSNFx must be set to 1 in order to measure the internal sense node. An external monitor resistor can be used to measure the optical power, achieved by setting DISPx to 1. Therefore register bit ADSNFx must be set to 0 in order to measure directly at pin MDAx.

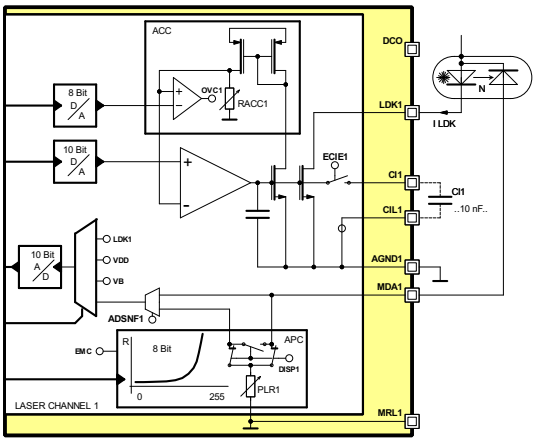


Figure 9: ACC with monitor photodiode

ACC mode permits to combine both channels in one iC-HT (see chapter COMBINING BOTH CHANNELS) and several iC-HT in parallel. When both channels are combined the programmable overcurrent shutdown is by channel. Another option is to connect the LDK together when both channels are configured in ACC mode and the channel 1 with high current range configuration and the channel 2 with low current range configuration. With this pre-sets there is a granularity about 0.2% using the channel 1 steps regulation and about 0.03% using the channel 2 in the regulation.

The Regulator

In MCU mode the control can be carried out without the need of external capacitor. This allows a fast response of the regulator. The speed of the regulator's response and stability can be configured using three bits (COMPx), providing a compensation factor.

COMP1	Addr. 0x13; bit 6:4	R/W 011
000	Minimum compensation for the channel 1 regulator, slower response of regulator	
...		
111	Maximum compensation for the channel 1 regulator, faster response of regulator	

Table 31: Regulator delay compensation channel 1

COMP2	Addr. 0x18; bit 6:4	R/W 011
000	Minimum compensation for the channel 2 regulator, slower response of regulator	
...		
111	Maximum compensation for the channel 2 regulator, faster response of regulator	

Table 32: Regulator delay compensation channel 2

Alternatively it is possible to use external capacitors connected to pins CIx and CILx. In this case, register bit ECIEx should be set to 1 and COMPx to its highest value, "111".

ECIE1	Addr. 0x10; bit 1	R/W 0
0	External CI capacitor for channel 1 disconnected	
1	External CI capacitor for channel 1 connected	

Table 33: Enable external capacitor channel 1

ECIE2	Addr. 0x15; bit 1	R/W 0
0	External CI capacitor for channel 2 disconnected	
1	External CI capacitor for channel 2 connected	

Table 34: Enable external capacitor channel 2

The regulator is offset compensated in order to prevent optical power drifts. Offset compensation can be disabled by setting register bit EOCx to 0.

EOC1	Addr. 0x10; bit 4	R/W 1
0	Channel 1 regulator offset compensation disabled	
1	Channel 1 regulator offset compensation enabled	

Table 35: Enable offset compensation channel 1

EOC2	Addr. 0x15; bit 4	R/W 1
0	Channel 2 regulator offset compensation disabled	
1	Channel 2 regulator offset compensation enabled	

Table 36: Enable offset compensation channel 2

An internal oscillator is used for the offset compensation. A watchdog timer (WDT) is included in order to monitor proper function of the oscillator. If an error is detected by the WDT, the laser channels are disabled, OSCERR error bit is set in STATUS0 register and the error event is signaled at pin NCHK. This error signaling can be suppressed using the mask register bit MOSCERR (set to 1).

MOSCERR	Addr. 0x1D; bit 0	R/W 0
0	Oscillator error (watchdog) will be signaled at NCHK	
1	Oscillator error (watchdog) will not be signaled at NCHK	

Table 37: Oscillator error mask

iC-HT monitors the saturation voltage of the regulator´s output transistor at pin LDKx. The LDK saturation threshold can be configured through register bits RLDKSx.

RLDKS1	Addr. 0x13; bit 3:2	R/W 00
00	V(LDK1) < 0.5 V sets the LDKSAT1 alarm bit	
01	V(LDK1) < 0.8 V sets the LDKSAT1 alarm bit	
10	V(LDK1) < 1.0 V sets the LDKSAT1 alarm bit	
11	V(LDK1) < 1.2 V sets the LDKSAT1 alarm bit	

Table 38: LDK saturation threshold selection channel 1

RLDKS2	Addr. 0x18; bit 3:2	R/W 00
00	V(LDK2) < 0.5 V sets the LDKSAT2 alarm bit	
01	V(LDK2) < 0.8 V sets the LDKSAT2 alarm bit	
10	V(LDK2) < 1.0 V sets the LDKSAT2 alarm bit	
11	V(LDK2) < 1.2 V sets the LDKSAT2 alarm bit	

Table 39: LDK saturation threshold selection channel 2

If the LDKx voltage falls below the LDK saturation threshold the LDKSATx error bit in STATUS1 register will be set and it will be signaled through output pin NCHK. Setting the mask register bit MLDKSATx to 1 suppresses the signaling at NCHK.

MLDKSAT1	Addr. 0x1D; bit 2	R/W 1
0	LDKSAT1 event will be signaled at NCHK	
1	LDKSAT1 event will not be signaled at NCHK	

Table 40: LDK saturation mask channel 1

MLDKSAT2	Addr. 0x1D; bit 3	R/W 1
0	LDKSAT2 event will be signaled at NCHK	
1	LDKSAT2 event will not be signaled at NCHK	

Table 41: LDK saturation mask channel 2

Laser channel enabling and error handling

With pin INS/WKR or EMC unconnected, a corresponding error signal will be generated (INSOPEN, EMCOPEN) and will disable the laser channels. Any input interface could be enabled if EMC or INS pins are open. Comunication with the chip might be possible but laser cannot be switched on. This situation is only signaled at the MCU interruption pin NCHK, which would remain low as long as any of the EMC or INS pins are unconnected. MCU must monitor the status of the NCHK pin to get all the status information of the chip

Setting DISC1 and DISC2 to 1(default) disables the corresponding channel.

The errors in STATUS0 and STATUS1 registers disable the laser channels. Every change in the STATUS registers is signaled at pin NCHK, unless the error event is masked by the corresponding error mask bit.

Register	Address	Bits	Default	Description
INITRAM	0x00	0	R/O	RAM initialized.
PDOVDD	0x00	1	R/O	Power down event at VDD
MEMERR	0x00	2	R/O	RAM memory validation error
OVT	0x00	3	R/O	Overtemperature event
OVC2	0x00	4	R/O	Overcurrent at channel 2
OVC1	0x00	5	R/O	Overcurrent at channel 1
OSCERR	0x00	6	R/O	Oscillator error (watchdog set)
CFGTIMO	0x00	7	R/O	Configuration mode timeout event
MAPC1	0x01	0	R/O	Channel 1 current state (on or off)
MONC1	0x01	1	R/O	Monitor channel 1 enabled at least once (latched)
LDKSAT1	0x01	2	R/O	Channel 1 LDK saturation event
MAPC2	0x01	4	R/O	Channel 2 current state (on or off)
MONC2	0x01	5	R/O	Monitor channel 2 enabled at least once (latched)
LDKSAT2	0x01	6	R/O	Channel 2 LDK saturation event

Table 42: Status registers overview

In order to enable the channels, the error events must be acknowledged. Acknowledging an error is accomplished by reading the STATUS register. After a power-on PDVDD and INITRAM errors will be set, therefore it is required to read STATUS0 and STATUS1 registers after each power-on.

Exiting standby mode will not reset the RAM but will set the PDOVDD status bit. Therefore STATUS0 must be read once after each standby to re-enable the laser channels.

In case of an overcurrent (OVC) or an overtemperature (OVT) event, laser channels are disabled.

A memory error event and a configuration timeout error event will also disable the laser channels. More information about the memory error on page 34. The conditions to enable each laser channel are shown in figure 10.

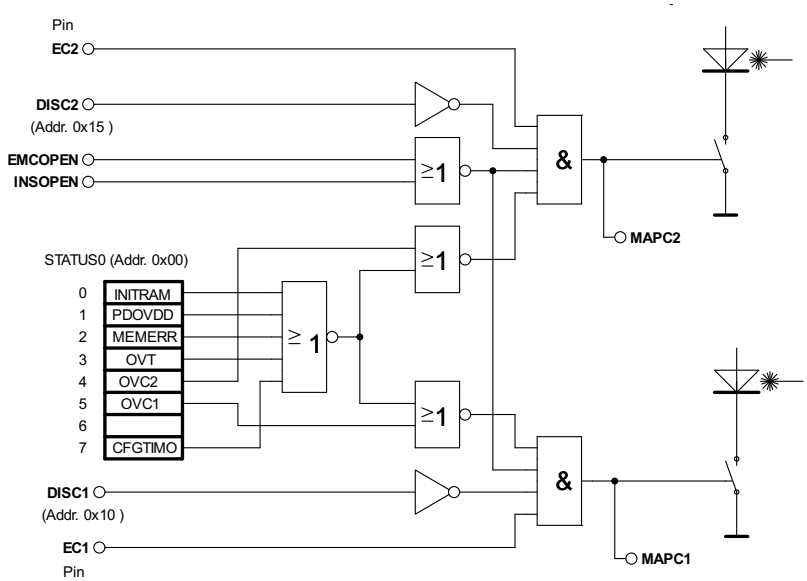


Figure 10: Laser control logic in MCU mode

COMBINING BOTH CHANNELS

iC-HT can drive one laser diode up to 1500 mA with both channels combined.

Therefore register bit MERGE must be set to 1. Disable channel register bits DISC1 and DISC2 must both be set to 0 and both enable channel pins EC1 and EC2 must be set hi.

MERGE	Addr. 0x1B; bit 6	R/W 0
0	Channel 1 and 2 operate independently	
1	Power transistor from channel 2 in parallel with channel 1, controlled by channel 1	

Table 43: Channel merging

When both channels are combined the control is done by channel 1. APC and ACC can both be used with both channels combined. In ACC mode, the reference needs be set to 50% of the desired current value. This is not required for APC.

ACC typical current settings with MERGE = 1		
REF1	**RACCx=0 RMERGE=1**	**RACCx=1 MERGE=1**
0x000	144.0 mA	18.12 mA
0x001	144.4 mA	18.16 mA
0x010	144.8 mA	18.20 mA
…	…	…
0x200	512.4 mA	60.28 mA
0x201	513.6 mA	60.42 mA
0x202	514.8 mA	60.56 mA
…	…	…
0x3FD	1692.0 mA	199.54 mA
0x3FE	1696.0 mA	199.54 mA
0x3FF	1700.0 mA	200 mA

Table 44: ACC typical current settings with MERGE = 1

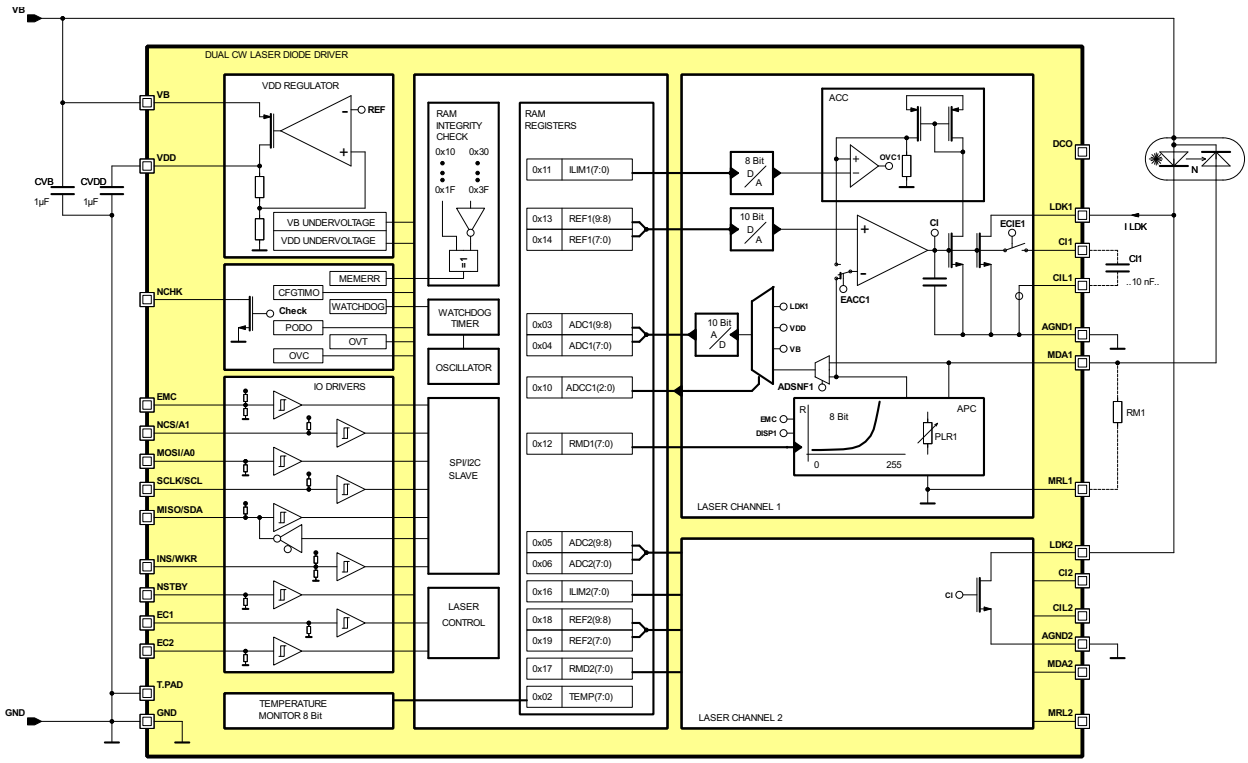


Figure 11: Combining both channels

In combined mode, the internal CI nodes of both channels are connected together. If required, an external capacitor on channel 1 can be used for improved stability. It is possible to have an additional external capacitor on channel 2 if ECIE2 bit is set to 1. Having an external capacitor on channel 2 and none on channel 1 is invalid.

On combined operation both overcurrent thresholds are active. The overcurrent threshold channel 1 needs to be set to to 50% and the overcurrent threshold chan-

nel 2 should be disabled by setting it to its maximum value (0xFF). An overcurrent will only be detected on channel 1.

ILIM1	Addr. 0x11; bit 7:0	R/W 0xFF
0x0A	Channel 1 overcurrent threshold: 80 mA, MERGE=1	
...	Channel 1 overcurrent threshold set to $Ilim = (2 * \Delta I(LDK) \cdot n)$, n from 10 to 255, MERGE=1	
0xFF	Channel 1 overcurrent threshold: 2040 mA, MERGE=1	

Table 45: Overcurrent threshold configuration channel 1 with MERGE = 1

It is possible to use a second photodiode connected to channel 2 (e.g. as a safety supervisor). The ADC on channel 2 can be used to monitor the voltage at pin MDA2, as it is shown in figure 12.

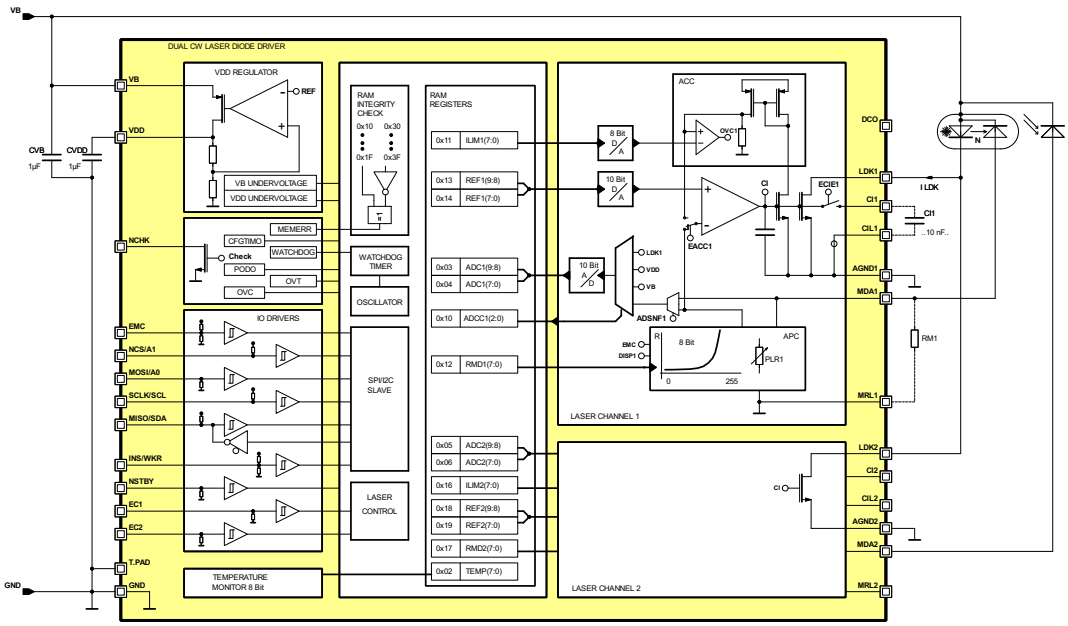


Figure 12: Additional photodiode in combined configuration

SERIAL COMMUNICATION INTERFACES

SPI slave interface

The SPI slave interface is enabled by setting pin INS/WKR to lo and uses pins NCS/A1, SCLK/SCL, MISO/SDA and MOSI/A0. Pin NCS/A1 is the chip select pin and must be set lo by the SPI master in order to start communication. Pins MISO/SDA and MOSI/A0 are the data communication lines and pin SCLK/SCL is the clock line generated by the SPI master (e.g. microcontroller). The SPI protocol frames are shown in figure 13.

A communication frame consists of one address byte and at least one data byte. Bits 7:6 of the address byte is the opcode used for selecting a read operation (set to "10") or a write (set to "01") operation. The remaining 6 bits are used for register addressing.

It is possible to transmit several bytes consecutively, if the NCS signal is not reset and SCLK/SCL keeps clocking, as it is shown in figure 13. The address is internally incremented after each transmitted byte. Once the address reaches the last register (0x3F), it is reset back to 0x00.

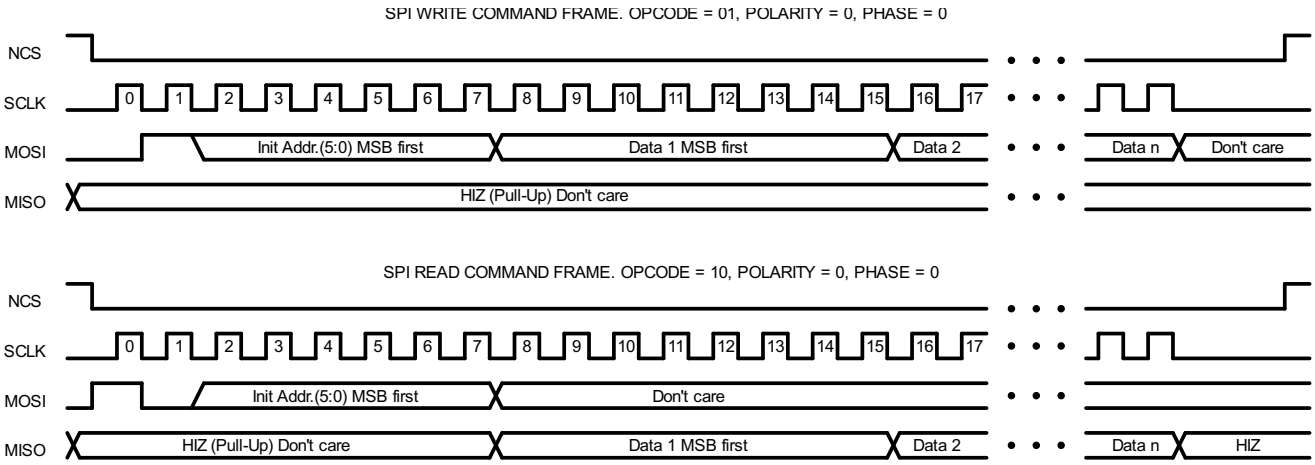


Figure 13: SPI read and write commands

I²C slave interface

The I²C slave interface is enabled by setting pin INS/WKR to hi and uses pins NCS/A1, SCLK/SCL, MISO/SDA and MOSI/A0. The protocol frames are shown in figure 14.

A communication frame consists of one slave address byte, one register address byte and at least one data byte. Bits 7:1 of the slave address byte form the slave identification code (ID) and bit 0 is used for specification of the data direction (0 for write, 1 for read). The slave ID consists of 7 bits. The five most significant bits are fixed by default to value 0b11000. Pins MOSI/A0 and NCS/A1 are used to set the remaining slave ID bits (see table 46 and 47).

Action	b7	b6	b5	b4	b3	b2	b1	b0
Write to slave	1	1	0	0	0	A1	A0	0
Read from slave	1	1	0	0	0	A1	A0	1

Table 46: I²C write/read byte

Action	A1	A0	Slave ID	Address byte
Write to slave 0	lo	lo	0x60	0xC0
Read from slave 0	lo	lo	0x60	0xC1
Write to slave 1	lo	hi	0x61	0xC2
Read from slave 1	lo	hi	0x61	0xC3
Write to slave 2	hi	lo	0x62	0xC4
Read from slave 2	hi	lo	0x62	0xC5
Write to slave 3	hi	hi	0x63	0xC6
Read from slave 3	hi	hi	0x63	0xC7

Table 47: I²C write/read address

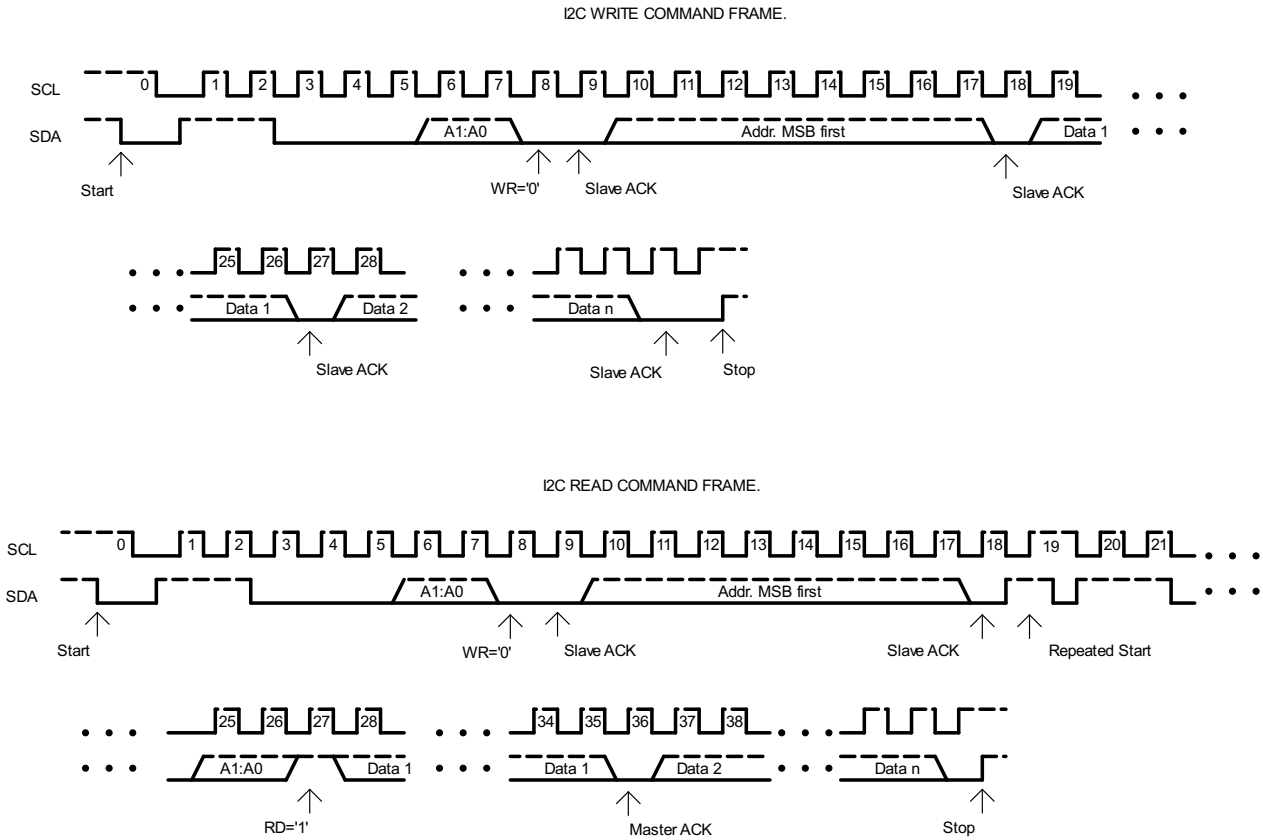


Figure 14: I^{2}C read and write commands

8 BIT INTERNAL PROGRAMMABLE LOGARITHMIC MONITOR RESISTORS

In MCU mode internal 8 bit programmable logarithmic monitor resistors (PLRx) are provided for APC.

The resistor value can be selected from 256 values, ranging from 100 Ω to 500 kΩ, following logarithmic increments with a typical step width of 3.3%. The resistors are configured with registers RMDx(7:0).

RMD1	Addr. 0x12; bit 7:0	R/W 0xFF
0x00	PLR1 set to the minimum resistance	
...	PLR1 set to $Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$, n from 0 to 255	
0xFF	PLR1 resistor set to the maximum resistance	

Table 48: MDA resistor channel 1

RMD2	Addr. 0x17; bit 7:0	R/W 0xFF
0x00	PLR2 resistor set to the minimum resistance	
...	PLR2 set to $Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$, n from 0 to 255	
0xFF	PLR2 resistor set to the maximum resistance	

Table 49: MDA resistor channel 2

The following formula calculates the register RMDx in order to set the desired resistor value:

$$Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}, \text{ n from 0 to 255}$$

Where Rmd_0 is the minimum resistor value (typically 100 Ω), $\Delta Rmd(\%)$ is the step between two consecutive resistor values (typically 3.3%) and n is the value of RMDx register in decimal.

In APC mode the regulation node is the internal connection to PLR, it is not MDAx pin. Voltage present at pin MDAx may differ from the internal regulation node. This regulation node can be sensed through the 10 bit A/D converter and read at register ADCx. Register bit ADSNFx must be set to 1 for this purpose. If ADSNFx is set to 0, MDAx pin will be the input of the A/D converter.

At pin MDAx only the 4 MSB of the RMDx configuration from PLRx are measurable. The 8 bits of the PLRx configuration RMDx can be measured with the A/D converter setting ADSNFx to 1.

The PLRx can be disabled using register bit DISPx. With DISPx = 0 the PLRx is enabled and DISPx = 1 disables the PLRx.

DISP1	Addr. 0x10; bit 2	R/W 0
0	PLR enabled for channel 1	
1	PLR disabled for channel 1	

Table 50: Disable PLR channel 1

DISP2	Addr. 0x15; bit 2	R/W 0
0	PLR enabled for channel 2	
1	PLR disabled for channel 2	

Table 51: Disable PLR channel 2

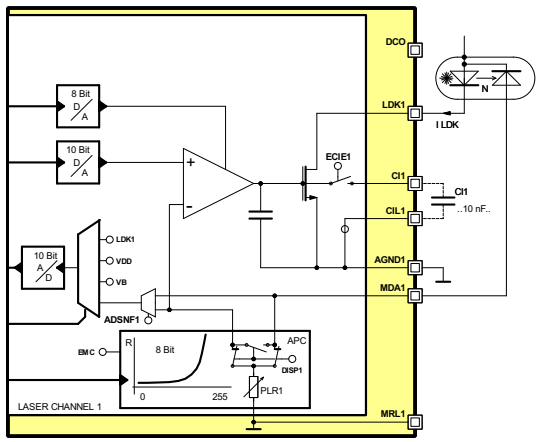


Figure 15: PLR in APC

In ACC mode the PLR is not used in the control circuit. Instead, the internal RACCx resistor is used in the control loop.

Even though the PLR is not in the control circuit, it can be enabled (DISPx = 0) in order to give feedback through the 10 bit A/D converter for the controlling light power if a monitor diode is connected.

Register bit ADSNF is set to 1 to measure the internal sense node. Alternatively, an external monitor resistor can be used to measure the optical power, by setting DISPx to 1. Then register bit ADSNF must be set to 0 in order to measure directly at pin MDAx.

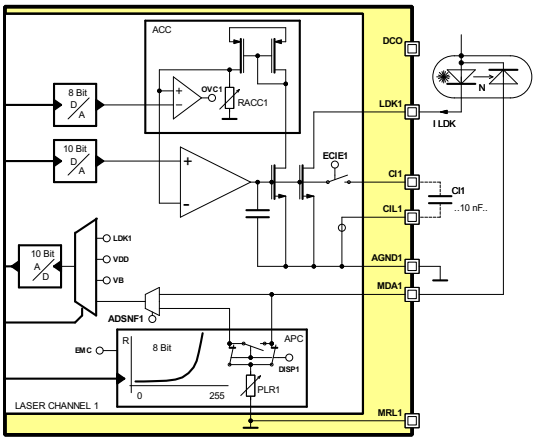


Figure 16: ACC with monitor photodiode

10 BIT LOGARITHMIC D/A CONVERTER

The 10 bit logarithmic D/A converter is used for setting the regulator´s voltage reference. The D/A converter is active in all operating modes. In iC-WK mode only two values are available: 0.25 V (setting INS/WKR pin lo) and 0.5 V (setting INS/WKR pin hi). In MCU mode both APC and ACC use the D/A converter. With a range from 0.1 V to 1.1 V and the typical step width is 0.235%.

The D/A converter is configured through register REFx(9:0). With REFx(9:0) = 0x000, D/A output value is set to 0.1 V, and for REFx(9:0) = 0x3FF, D/A output is configured to 1.1 V.

REF1	Addr. 0x13/14; bit 9:0	R/W 0x000
0x000	Channel 1 regulator reference voltage set to minimum voltage	
. . .	Channel 1 regulator reference voltage set to $Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}$, n from 0 to 1023	
0x3FF	Channel 1 regulator reference voltage set to maximum voltage	

Table 52: Channel 1 regulator voltage reference

REF2	Addr. 0x18/19; bit 9:0	R/W 0x000
0x000	Channel 2 regulator reference voltage set to minimum voltage	
. . .	Channel 2 regulator reference voltage set to $Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}$, n from 0 to 1023	
0x3FF	Channel 2 regulator reference voltage set to maximum voltage	

Table 53: Channel 2 regulator voltage reference

To calculate the D/A converter value for each REFx value, use the following formula:

$$Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}, \text{ n from 0 to 1023}$$

Where $Vref_0$ is the minimum value (typically 0.1 V), $\Delta Vref$(%) is the step value (typically 0.235 %) and n is the value of REFx register in decimal.

10 BIT LINEAR A/D CONVERTER

A 10 bit linear A/D converter is available for each channel when working in MCU mode. A variety of voltages can be measured by the converter with two resolutions:

- V(LDKx) up to 8 V with 8.6 mV resolution
- V(VDD) up to 8 V with 8.6 mV resolution
- V(VB) up to 8 V with 8.6 mV resolution
- V(MDAx) up to 1 V with 1.075 mV resolution
- V(PLRx) up to 1 V with 1.075 mV resolution

Note that when the value to be converted is higher than 8 V the A/D converter is saturated at its highest conversion value.

The register bits ADCCx select the signal measured with the 10 bit A/D converter.

ADCC1(2:0)	Addr. 0x10; bit 7:5	R/W 000
0xx	Channel 1 ADC disabled	
100	Channel 1 ADC sourced by V(MDA1), ADSNF1 = 0	
100	Channel 1 ADC sourced by V(PLR1), ADSNF1 = 1	
101	Channel 1 ADC sourced by V(VB)	
110	Channel 1 ADC sourced by V(VDD)	
111	Channel 1 ADC sourced by V(LDK1)	

Table 54: ADC channel 1 source selection

ADCC2(2:0)	Addr. 0x15; bit 7:5	R/W 000
0xx	Channel 2 ADC disabled	
100	Channel 2 ADC sourced by V(MDA2), ADSNF2 = 0	
100	Channel 2 ADC sourced by V(PLR2), ADSNF2 = 1	
101	Channel 2 ADC sourced by V(VB)	
110	Channel 2 ADC sourced by V(VDD)	
111	Channel 2 ADC sourced by V(LDK2)	

Table 55: ADC channel 2 source selection

With ADCCx(2:0) = 100, the signal to the A/D converter is selected by register bit ADSNFx (A/D converter sense not force). With ADSNFx = 1 the measuring point to the A/D converter is the internal sense node of the internal programmable logarithmic monitor resistor (PLR). With ADSNFx = 0 the sensing point is connected directly to MDAx pin.

ADSNF1	Addr. 0x1A; bit 2	R/W 0
0	ADC measurement MDA1 pin (force)	
1	ADC measurement PLR1 (sense)	

Table 56: ADC channel 1 sense/force selection

ADSNF2	Addr. 0x1A; bit 6	R/W 0
0	ADC measurement MDA2 pin (force)	
1	ADC measurement PLR2 (sense)	

Table 57: ADC channel 2 sense/force selection

When enabled, the A/D converter is continuously acquiring the signal selected by ADCCx register. The conversion time, is 140 µs. Changing the source requires 500 µs settling time.

In order to do a measurement, register ADCx must be read. The converter does not provide an end of conversion (EOC) bit. Instead, ADCx register contains always the value of the last conversion.

As the A/D converter is 10 bit long, the results are split into two byte wide separated registers; ADCxh contains channel x ADC MSBs values while ADCxl stores the LSBs. A consecutive read action of both registers (lower and upper part) should be carried out in order to prevent an undesired change in the measured value between two read actions.

ADC1	Addr. 0x03/04; bit 9:0	R
0x000	ADC minimum value	
0x3FF	ADC maximum value	

Table 58: ADC channel 1

ADC2	Addr. 0x05/06; bit 9:0	R
0x000	ADC minimum value	
0x3FF	ADC maximum value	

Table 59: ADC channel 2

The voltage corresponding to the measured digital value can be directly obtained through the following formula:

$$V(LDKx, VB, VDD) = 8 * \frac{VFS}{1023} * ADCx$$

$$V(MDAx, PLRx) = \frac{VFS}{1023} * ADCx$$

VFS is the fullscale voltage of the A/D converter (cf. *Electrical Characteristics No. 706*) typical 1.1 V. For a more precise measurement, the A/D converter can be calibrated by measuring a known VB voltage and calculate the VFS.

If ADSNFx = 0 the sensing point is connected directly to MDAx pin. Depending on the regulation voltage, it is possible that V(MDAx) is higher than 1.1 V. When MDAx pin is the source of the A/D converter, saturation of the converter will occur. When monitoring pin MDAx with the A/D converter, V(MDAx) must be lower than 1.1 V.

DC/DC CONVERTER OPTIMIZATION

iC-HT provides a 6 bit configurable current at pin DCO that can be used to trim the output voltage of a DC/DC converter.
Possible application benefits with using DCO:

- DC/DC step down operation: regulation at voltages lower than power supply
- DC/DC step up operation: regulation at voltages higher than power supply
- Efficiency enhancement

RDCO	Addr. 0x1B; bit 5:0	R/W 0x02
0x00	No current	
...		
0x3F	130 µA typ (cf. *Electrical Characteristics No. D01*)	

Table 60: Digital current output register

The proposed applications can be demonstrated with a standard DC/DC converter e.g. TPS63060DSC from Texas Instruments. This converter allows an input voltage ranging from 2.5 V to 12 V and offers an output voltages from 2.5 V to 8 V. It is capable of delivering up to 2 A current, depending on the output voltage. Figure 17 shows a possible configuration.

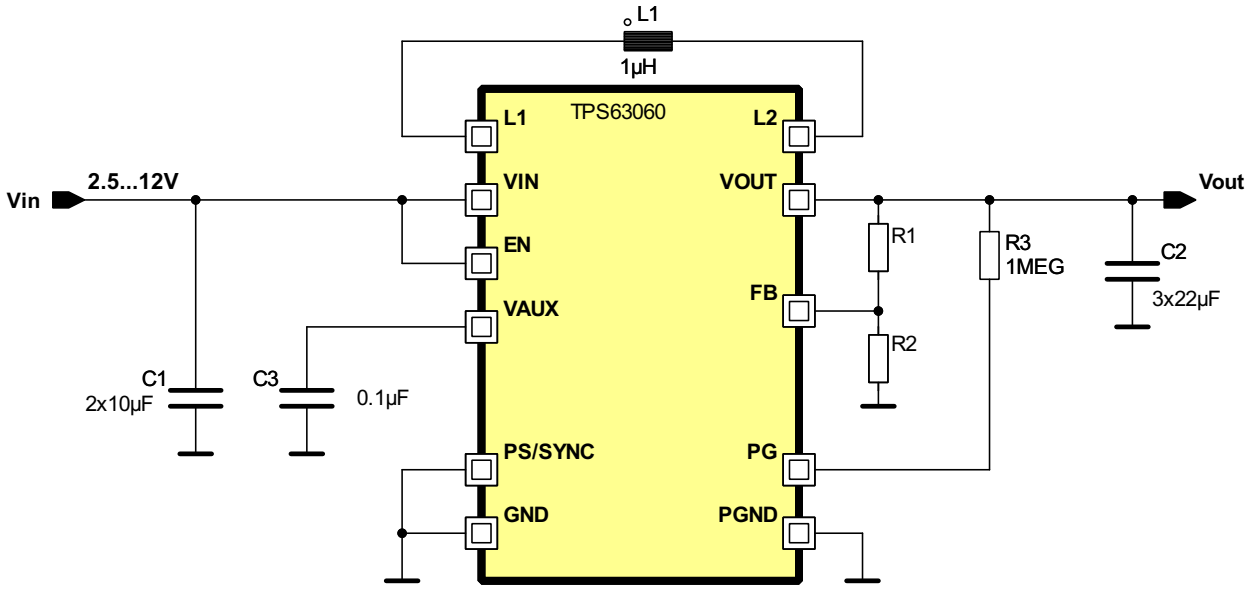


Figure 17: TPS63063 DC/DC converter from TI

DC/DC step down operation:
regulation at voltages lower than power supply
The resistors R1 and R2 in the feedback path allow setting the desired output value Vout. The DC/DC converter drives Vout pin in order to yield 0.5 V at feedback pin FB. The DCO output signal from iC-HT is connected to FB pin. The Vout is controlled with the internal register RDCO from iC-HT.

The DCO current into FB node controls the voltages of the divider R1 and R2 and Vout changes in order to maintain 0.5 V at FB pin. Selecting R1 and R2 needs to consider:

- Resistors values:
  $R1 = R2(\frac{Vout}{Vfb} - 1)$
- Current of the voltage divider should be high enough, in comparism to the current from the pin DCO, to offer acceptable resolution. The programmable current resolution from register RDCO is 2 µA.
- DCO current into the voltage divider will lower Vout voltage, Vout is 8 V when no current is present at DCO.

Choosing R1 to 100 kΩ, the value of R2 can be calculated:

$$R2 = \frac{R1}{\frac{Vout}{Vfb} - 1} = \frac{100k}{\frac{8}{0.5} - 1} = 6.7k\Omega$$

With this configuration the current through the voltage divider is 75 µA at 8 V . The resolution of each RDCO step is then 200 mV.

The value in RDCO register needed in order to have the desired output voltage can be calculated using the following formula:

$$RDCO = \frac{Idco}{2uA} = \frac{IR2-IR1}{2uA} = \frac{\frac{0.5}{6.7k} - \frac{Vout-0.5}{100k}}{2uA}$$

The resulting value will vary slightly depending on the tolerances of the selected resistors and DCO current.

The voltage is reduced from 8 V (RDCO = 0) to 2.5 V, when RDCO = 27.

DC/DC step up operation: regulation at voltages higher than power supply

A practical application of the present case is the control of blue lasers. This type of laser present a forward voltage around 5 V, which demands an LDA voltage of about 6 V. If the system is supplied with a 3 V LiPo battery, it is necessary to use a the DC/DC in order to step up and drive the laser diode and driver with a sufficient voltage. Figure 18 shows this application:

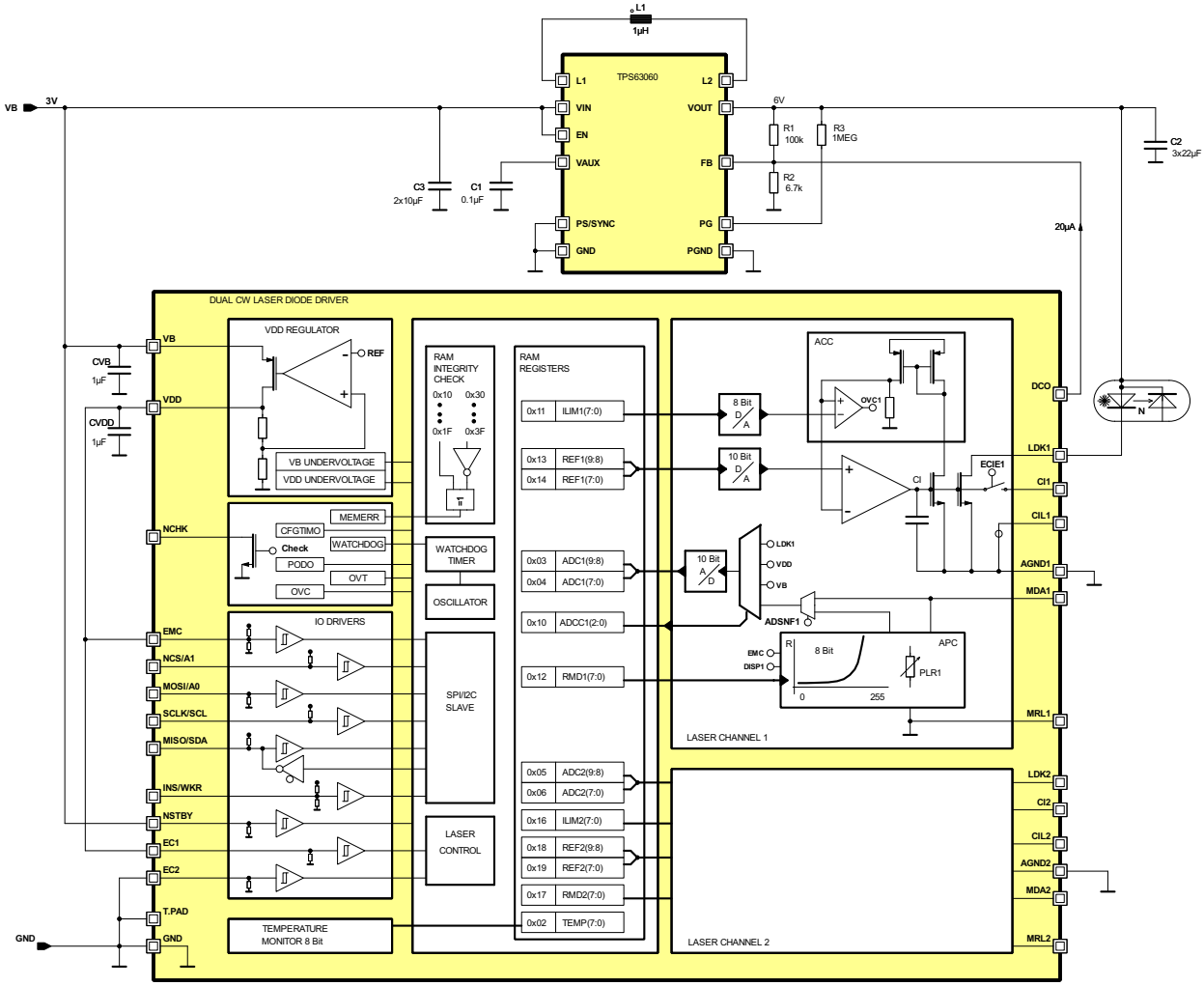


Figure 18: Regulation at voltage greater than power supply

Setting register RDCO to 10 it delivers 20 µA and 6 V are obtained at Vout.

Extension of system working voltage range

iC-HT must be supplied by a voltage within the threshold values of 2.8 V and 8 V. It is possible to control the DC/DC output in a voltage range of 2.5 V - 12 V if the DC/DC converter, controlled by DCO output signal, is included in the system, as it is shown in figure 19:

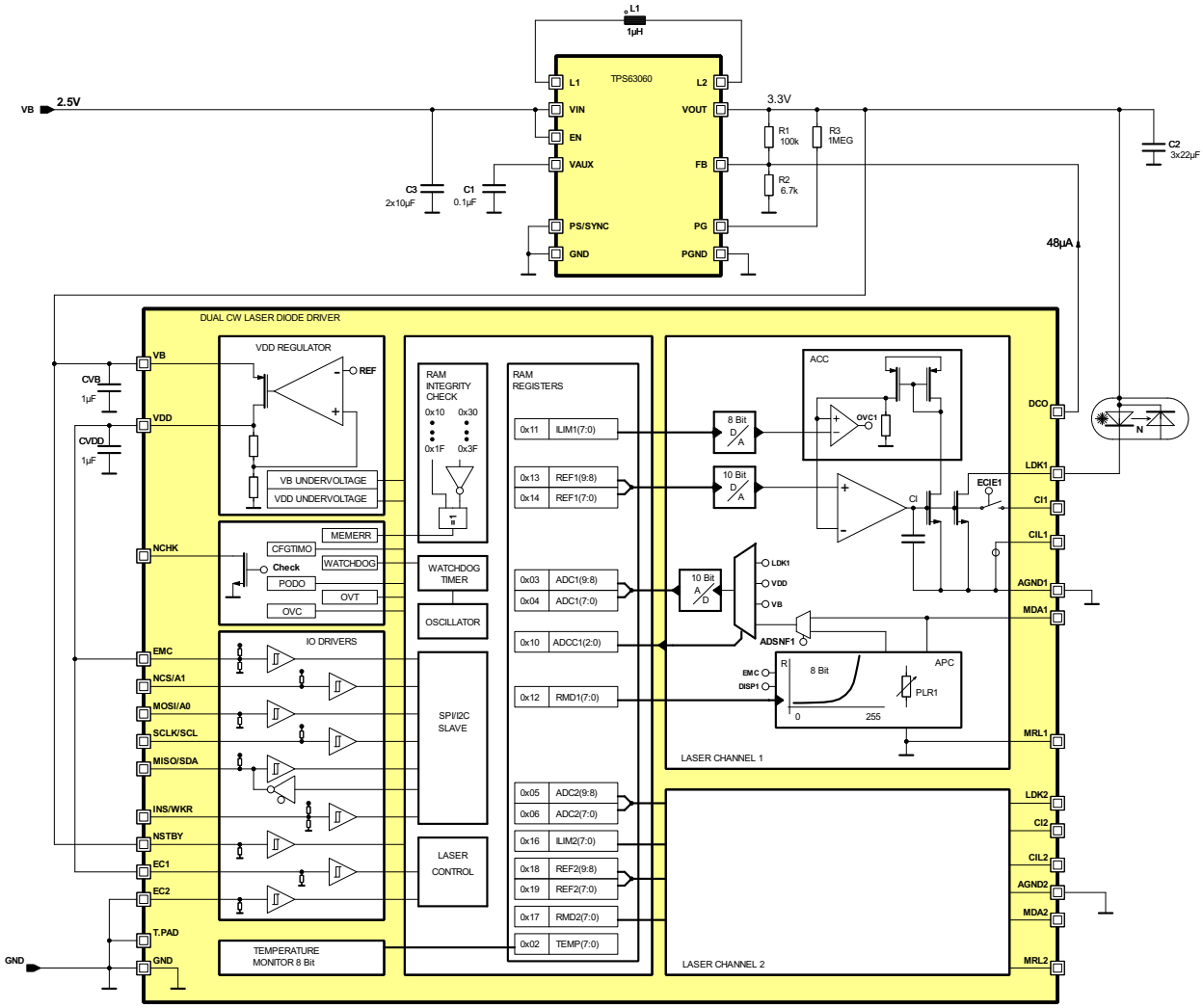


Figure 19: Extension of working voltage range

In the figure 19 both the laser and the iC-HT are supplied by output voltage Vout from DC/DC converter. The register RDCO is set to 23, which forces 48 µA to be output to the voltage divider. A system voltage of 3.3 V is obtained at Vout.

Efficiency enhancement

If iC-HT and the laser diode are supplied with the same power supply, the efficiency of the driver can be poor, depending on the supplied voltage, the saturation voltage and the laser diodes forward voltage. Power dissipation of the driver can be reduced if LDAx is fed through the DC/DC converter configured to deliver a lower voltage than the power supply as shown in figure 20.

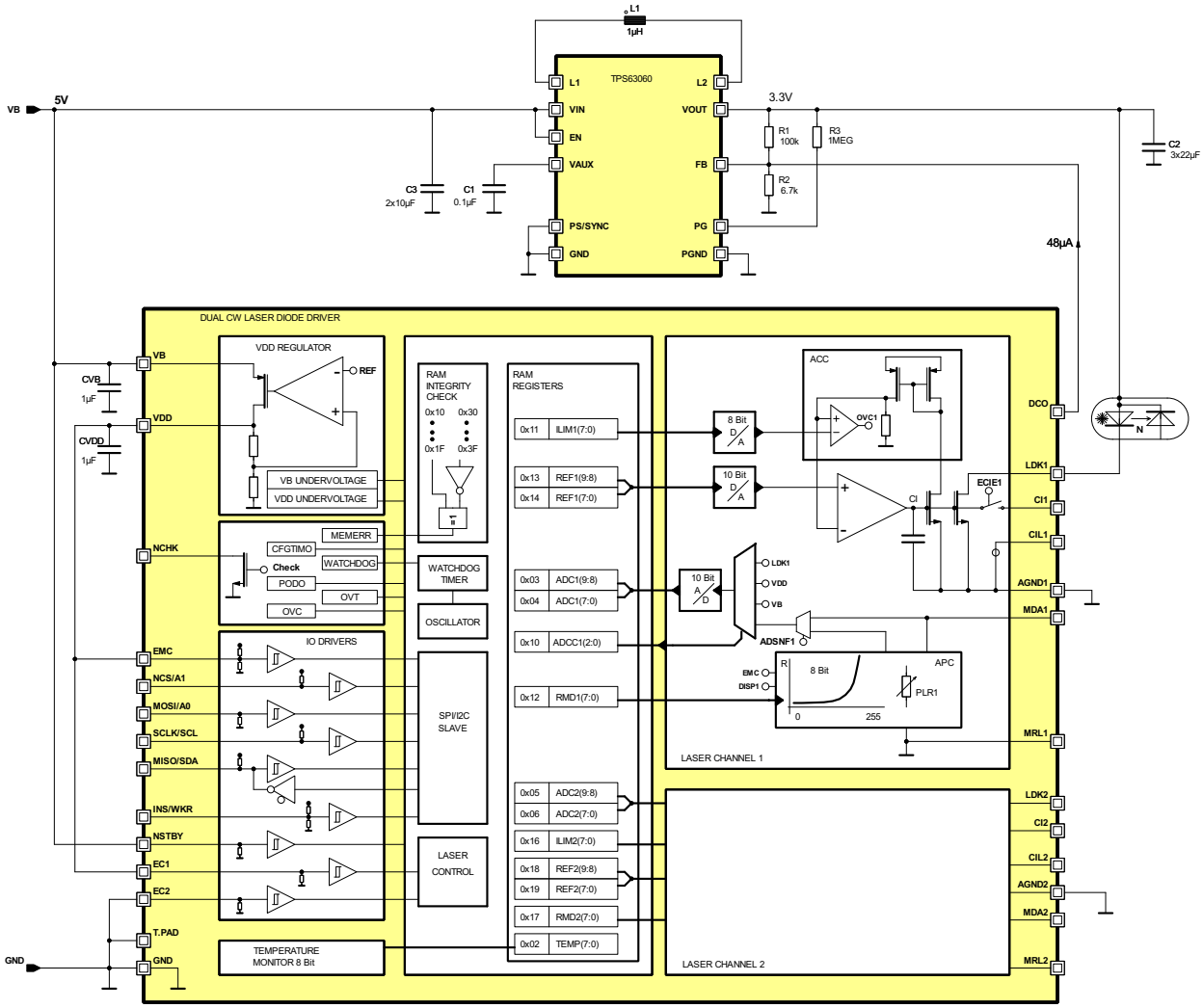


Figure 20: System efficiency enhancement

The register RDCO is set to 23 to provide a laser diode supply voltage of 3.3 V at Vout.

WATCHDOG TIMER

The internal 200 kHz oscillator is monitored with the Watchdog Timer (WDT).

If the oscillator remains longer than the maximum time of tWDT (cf. *Electrical Characteristics No. E03*) without activity an oscillator error is triggered. An oscillator error sets OSCERR error bit to 1. The automatic offset compensation of the laser control requires the oscillator.

The state of OSCERR is signaled at pin NCHK. The signaling of OSCERR state can be masked with bit MOSCERR. Setting MOSCERR to 1 masks the oscillator error and OSCERR will not be signaled at NCHK.

It is possible to simulate an error of the oscillator using SOSCERR bit. If SOSCERR = 1, the oscillator error is forced. When OSCERR is set to 1 the error will be signaled through NCHK, depending on the state of MOSCERR.

OSCERR	Addr. 0x00; bit 6	R
0	Oscillator operates OK	
1	Watchdog timeout set, oscillator fail. Cleared on read	

Table 61: Oscillator error

MOSCERR	Addr. 0x1D; bit 0	R/W 0
0	Oscillator error (watchdog) will be signaled at NCHK	
1	Oscillator error (watchdog) will not be signaled at NCHK	

Table 62: Oscillator error mask

SOSCERR	Addr. 0x1D; bit 7	R/W 0
0	No oscillator error simulated.	
1	Oscillator error simulated (watchdog timeout).	

Table 63: Simulate oscillator error

TEMPERATURE MONITOR AND PROTECTION

iC-HT includes an 8 bit temperature monitor that allows to measure the internal chip temperature going from -40 °C to 125 °C. The resolution is 1 °C/LSB. The internal temperature can be obtained by reading TEMP register. The TEMP register is a read-only register.

TEMP	Addr. 0x02; bit 7:0	R
0x00	Minimum temperature	
...		
0xFF	Maximum temperature	

Table 64: Chip temperature

Absolute read values may differ from one chip to another. An individual initial calibration of the temperature monitor is recommended. The TEMP register must be read at a known temperature. Using the resolution value of 1 °C/LSB, the internal temperature can be calculated.

The temperature monitor can be used to compensate temperature effects on the laser diode. The microcontroller can use a laser diode characteristic formula or a look-up table combined with the temperature value measured through TEMP register. The reference voltage can be configured accordingly in order to compensate temperature effects.

iC-HT is protected against overtemperature. In iC-WK mode, if the internal temperature value exceeds the overtemperature threshold an OVT error event will be triggered and signaled through pin NCHK. Both laser channels will be disabled. Pin NCHK will keep signaling the error although the internal temperature goes down to a safe value below the overtemperature threshold value. If the temperature has exceeded the overtemperature threshold value, pins EC1 and EC2 have to be pulled lo in order to stop signaling the error. Setting pin ECx back hi will re-enable the corresponding channel.

In microcontroller mode, if the internal temperature exceeds a safety value an overtemperature error bit (OVT) will be set to 1. If OVT = 1, both channels will be disabled and the error event will be signaled through NCHK pin. If the internal temperature goes down to a safe value below the overtemperature threshold value, OVT will remain at value 1. Reading the OVT bit stop signaling error through pin NCHK. Reading OVT bit will set it back to 0. Setting ECx pin lo and then back hi will allow re-enabling the corresponding channel.

The overtemperature threshold value can not be configured.

OVT	Addr. 0x00; bit 3	R
0	No overtemperature event has occurred since last read	
1	Overtemperature event has occurred. Cleared on read	

Table 65: Overtemperature detection

In microcontroller mode it is possible to simulate an overtemperature event using SOVT bit. Setting SOVT to 1, the overtemperature error flag OVT will be set to 1. iC-HT will remain in error state until SOVT is set back to 0.

SOVT	Addr. 0x1D; bit 4	R/W 0
0	No overtemperature event is simulated.	
1	Overtemperature event simulated.	

Table 66: Simulate overtemperature

DIGITAL INTERFACE AND MEMORY INTEGRITY MONITOR

iC-HT provides a microcontroller slave interface by selection on the EMC pin. iC-HT support the interfaces SPI or I²C that are selected by the INS/WKR pin.

EMC	Addr. Pin;
lo	iC-WK-mode, digital interfaces disabled
Open	Not allowed, error signaled
hi	MCU mode, interface selected by INS/WKR enabled

Table 67: Enable microcontroller

INS/WKR	Addr. Pin;
lo	SPI interface selected
Open	Not allowed, error signaled.
hi	I²C interface selected

Table 68: Interface selection I²C or SPI

The configuration memory is integrity monitored and **atomic executable** (all at once: changes of the configurations without any direct effects, the changes are executed at once by command) to the functional blocks of iC-HT.

Integrity monitoring is implemented by a duplication of the configuration registers into a validation page (see description below) where the register are automatically copied with inverted value. Every register bit is compared with its validation copy and in case of difference, a memory error is generated and both laser channels are switched off.

Atomic appliance is achieved by latching the configuration registers. This permits a full configuration (different registers) to be made prior to apply it to the laser channels. iC-HT has two different modes selectable by the MODE(1:0) register (address 0x1C).

MODE(1:0)	Addr. 0x1C; bit 1:0	R/W 01
00	Invalid parameter	
01	Operation mode	
10	Configuration mode	
11	Invalid parameter	

Table 69: Configuration and operation mode

In **Configuration mode**, the *configuration memory* (address 0x10 to 0x1F) can be written and read back to check a correct communication without changing the present configured operation state of the iC-HT. In this mode, the memory integrity check is disabled.

iC-HT will monitor the time elapsed in configuration mode and automatically switch the laser off if it exceeds a configuration mode timeout. The time in configuration mode must less than 40 ms for ensuring that no configuration timeout occurs during configuration (cf. *Electrical Characteristics No. E02*). The timeout can be up to 164 ms.

When writing the configuration is completed, iC-HT is switched to **operation mode** by writing "10" into the MODE register (address 0x1C). In **operation mode** the configuration is applied to the iC-HT and the memory integrity check activated. In this mode configuration registers can only be read (except MODE(1:0) register, which is always accessible). Figure 21 shows the interface to memory structure.

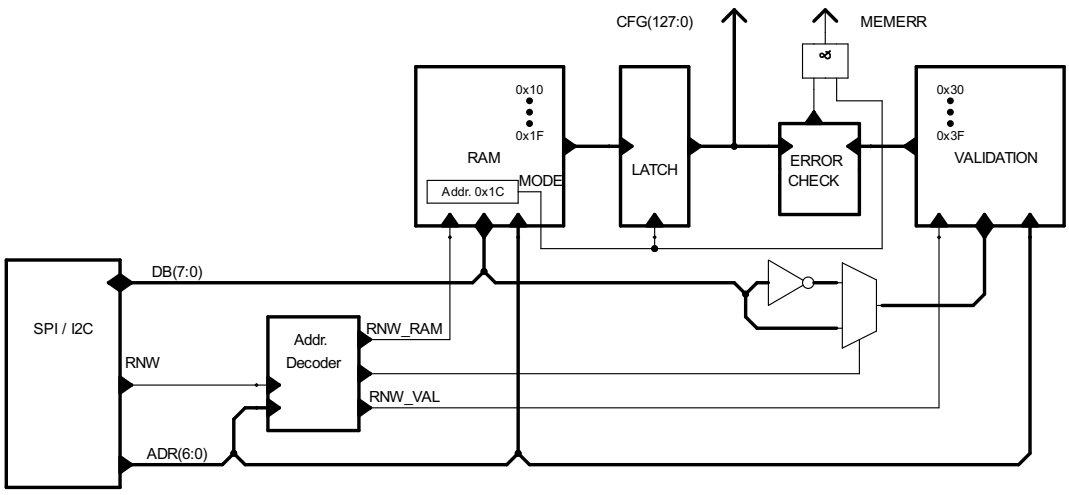


Figure 21: Interface, RAM integrity monitoring and configuration latching

Register map description
The register map consists of 64 addresses subdivided in three different pages:

- Read-only page, address 0x00 to 0x0F: iC-HT status, ADC readouts, thermometer readout and chip revision.
- Configuration page (integrity monitored), read-write registers, address 0x10 to 0x1F.
- Validation page, read-write registers, address 0x30 to 0x3F.

Read-only registers
Read-only registers are sub-divided as well into status registers (address 0x00 to 0x01) and measurement registers. Status registers are normally latched to 1 on events and cleared on read (see individual register description). Measurement registers are dual-port and can be accessed simultaneously with the measurements in progress. ADC1(address 0x03 to 0x04) and ADC2 (address 0x05 to 0x06) are 10 bit registers split into two 8 bit registers each and must be accessed in block mode (automatic address increment) to ensure data not changing during the read.

Configuration page (integrity monitored)
The configuration page (address 0x10 to 0x1F) contains the registers that control the driver. Every write operation to any of the registers of this page will be internally duplicated to the correspondent register at the validation page. After the write operation, the correspondent validation register will contain the inverted value of the configuration register.

Validation page
The validation page (address 0x30 to 0x3F) can be read or written normally. Only when a write procedure is made to any of the configuration registers the correspondent validation pair will be written with the inverted value of the configuration register as well.

Both the configuration and validation pages are initialized during power-up. This event is signaled at the STATUS0 register (bit 0, INITRAM). In standby mode (NSTBY = lo) the RAM is not reset if any write command has been executed and therefore, configuration and validation pages keep the stored information and INITRAM remains unset. Entering standby mode after power-up without any write command, the RAM will be initialized again and the INITRAM bit will be set to 1 again. Any VDD power-down event signaled at the STATUS0 register outside the standby mode (NSTBY = hi) requires a RAM content check regardless of the state of the INITRAM bit to ensure data is not corrupted.

Possible start-up sequence:

1. iC-HT starts in operation mode with default configuration. INITRAM and PDOVDD error bits must be set in STATUS0, DISC1 (address 0x10, bit 3) and DISC2 (address 0x15, bit 3) are set to 1.
2. Write MODE(1:0) = "10" register (Addr. 0x1C) to enable the configuration mode.
3. Configure the laser channels.
4. Read back to verify a correct data transfer.
5. Set the DISC1, DISC2 bits to 0 on used channels.
6. Read the status registers(address 0x00, 0x01, 0x02) to detect possible errors and validate status. If any error exist, read again to ensure its validation.
7. Write MODE(1:0) = "01" register (address 0x1C) to apply the configuration and enable the memory integrity check.
8. During operation: monitor the status registers checking for errors. The NCHK pin signals any set status bit if not masked. This pin can be used to trigger an microcontroller interrupt line.

START-UP

Setting pin NSTBY to lo iC-HT enters standby mode. In stand by mode and with no supply voltage at pin VDD and the current consumption on VB is reduced to less than 10 µA (cf. *Electrical Characteristics No. 002*).

After wake-up (pin NSTBY rising edge), the internal regulated supply VDD is generated again. The required time Tvdd depends on the capacitor connected to the VDD pin (cf. *Electrical Characteristics No. 504*).

Once the VDD voltage level is correct, iC-HT enters an offset compensation procedure regardless of the state of the laser enable pins (EC1, EC2). During this time (Ten), EC1 and EC2 are ignored and laser cannot be switched on (cf. *Electrical Characteristics No. 111*). After this time (Ten), laser channels can be switched on.

The switch-on procedure needs an initial time (Tci) to reach the 80 % of the target light power (in APC mode) or laser current (in ACC mode) (cf. *Electrical Characteristics No. 112*) and an additional time (Tcio) to reach the 99 % of the value (cf. *Electrical Characteristics No. 113*). Figure 22 illustrates an startup example for channel 1 in iC-WK mode.

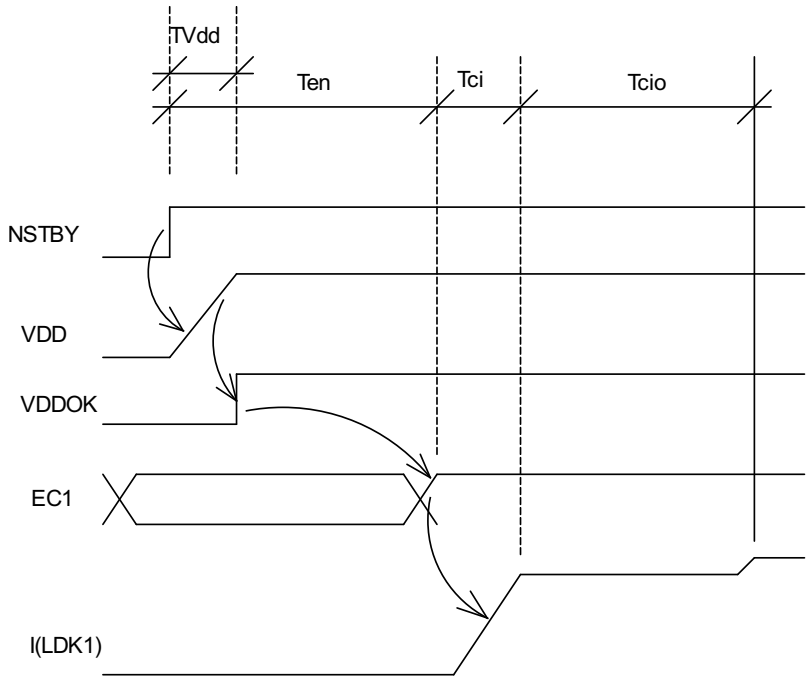


Figure 22: Startup timing diagram

REGISTER OVERVIEW

OVERVIEW

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00 R	CFGTIMO	OSCERR	OVC1	OVC2	OVT	MEMERR	PDOVDD	INITRAM
0x01 R		LDKSAT2	MONC2	MAPC2		LDKSAT1	MONC1	MAPC1
0x02 R	TEMP(7:0)							
0x03 R							ADC1(9:8)	
0x04 R	ADC1(7:0)							
0x05 R							ADC2(9:8)	
0x06 R	ADC2(7:0)							
0x07 R	Not implemented							
...	Not implemented							
0x0F R	Chip revision mark							
0x10	ADCC1(2:0)			EOC1	DISC1	DISP1	ECIE1	EACC1
0x11	ILIM1(7:0)							
0x12	RMD1(7:0)							
0x13		COMP1(2:0)			RLDKS1(1:0)		REF1(9:8)	
0x14	REF1(7:0)							
0x15	ADCC2(2:0)			EOC2	DISC2	DISP2	ECIE2	EACC2
0x16	ILIM2(7:0)							
0x17	RMD2(7:0)							
0x18		COMP2(2:0)			RLDKS2(1:0)		REF2(9:8)	
0x19	REF2(7:0)							
0x1A		ADSNF2		RACC2		ADSNF1		RACC1
0x1B		MERGE	RDCO(5:0)					
0x1C	Not implemented						MODE(1:0)	
0x1D	SOSCERR	SOVC2	SOVC1	SOVT	MLDKSAT2	MLDKSAT1	MMONC	MOSCERR
0x1E	Reserved register. Set to zero							
0x1F	Reserved register(Factory test). Set to zero							
0x20	Not implemented							
...	Not implemented							
0x30	Validation content for 0x10, inverted							
0x31	Validation content for 0x11, inverted							
...	...							
0x3F	Validation content for 0x1F, inverted							

Table 70: Register layout

PARAMETERS

Register	Address	Bits	Default	Description
ADCC1	0x10	7:5	000	Configuration for ADC from channel 1
ADCC2	0x15	7:5	000	Configuration for ADC from channel 2
ADSNF1	0x1A	2	0	MDA force/sense for ADC measurement in channel 1
ADSNF2	0x1A	6	0	MDA force/sense for ADC measurement in channel 2
RACC1	0x1A	0	0	Channel 1 ACC resistor mirror factor
RACC2	0x1A	4	0	Channel 2 ACC resistor mirror factor
COMP1	0x13	6:4	011	Channel 1 regulator delay compensation
COMP2	0x18	6:4	011	Channel 2 regulator delay compensation
DISC1	0x10	3	1	Software disable for channel 1
DISC2	0x15	3	1	Software disable for channel 2
DISP1	0x10	2	0	Disable PLR for channel 1
DISP2	0x15	2	0	Disable PLR for channel 2
EACC1	0x10	0	0	Enable ACC mode for channel 1
EACC2	0x15	0	0	Enable ACC mode for channel 2
ECIE1	0x10	1	0	Enable external CI capacitor for channel 1
ECIE2	0x15	1	0	Enable external CI capacitor for channel 2
EOC1	0x10	4	1	Enable offset compensation for channel 1
EOC2	0x15	4	1	Enable offset compensation for channel 2
ILIM1	0x11	7:0	0xFF	Current limit at channel 1
ILIM2	0x16	7:0	0xFF	Current limit at channel 2
MERGE	0x1B	6	0	MERGE channels 1 and 2, controlled by channel 1
MLDKSAT1	0x1D	2	1	LDKSAT1 error mask
MLDKSAT2	0x1D	3	1	LDKSAT2 error mask
MMONC	0x1D	1	1	MONC error mask
MODE	0x1C	1:0	01	Configuration / Operation mode selection
MOSCERR	0x1D	0	0	OSCERR error mask
RDCO	0x1B	5:0	0x02	DC converter set point
REF1	0x13/0x14	9:0	0x000	Voltage reference at channel 1
REF2	0x18/0x19	9:0	0x000	Voltage reference at channel 2
RLDKS1	0x13	3:2	00	Channel 1 LDK saturation detector threshold
RLDKS2	0x18	3:2	00	Channel 2 LDK saturation detector threshold
RMD1	0x12	7:0	0xFF	Resistor at channel 1
RMD2	0x17	7:0	0xFF	Resistor at channel 2
SOSCERR	0x1D	7	0	Oscillator error simulation (watchdog timeout)
SOVC1	0x1D	5	0	Overcurrent event at channel 1 simulation
SOVC2	0x1D	6	0	Overcurrent event at channel 2 simulation
SOVT	0x1D	4	0	Overtemperature event simulation
Reserved	0x1A	7:0	0x00	Reserved
Reserved	0x1F	7:0	0x00	Reserved

Table 71: Parameter overview

Register	Address	Bits	Default	Description
INITRAM	0x00	0	R/O	RAM initialized.
PDOVDD	0x00	1	R/O	Power-down event at VDD
MEMERR	0x00	2	R/O	RAM memory validation error
OVT	0x00	3	R/O	Overtemperature event
OVC2	0x00	4	R/O	Overcurrent at channel 2
OVC1	0x00	5	R/O	Overcurrent at channel 1
OSCERR	0x00	6	R/O	Oscillator error (watchdog set)
CFGTIMO	0x00	7	R/O	Configuration mode timeout event
MAPC1	0x01	0	R/O	Channel 1 current state
MONC1	0x01	1	R/O	Monitor channel 1 enabled at least once (latched)
LDKSAT1	0x01	2	R/O	Channel 1 LDK saturation event
MAPC2	0x01	4	R/O	Channel 2 current state
MONC2	0x01	5	R/O	Monitor channel 2 enabled at least once (latched)
LDKSAT2	0x01	6	R/O	Channel 2 LDK saturation event

Table 72: Status overview

Register	Address	Bits	Default	Description
TEMP	0x02	7:0	R/O	Chip temperature measurement
ADC1h	0x03	1:0	R/O	Channel 1 ADC 9:8 readout
ADC1l	0x04	7:0	R/O	Channel 1 ADC 7:0 readout
ADC2h	0x05	1:0	R/O	Channel 2 ADC 9:8 readout
ADC2l	0x06	7:0	R/O	Channel 2 ADC 7:0 readout
CHIPREV	0x0F	7:0	R/O	Chip revision identification

Table 73: Measurement overview

Device identification

CHIPREV	Addr. 0x0F; bit 7:0	R
0x00	Initial version iC-HT	
0x01	iC-HT_1	
0x02	iC-HT_Z	
0x08	Reserved	

Table 74: Device identification

Status

INITRAM	Addr. 0x00; bit 0	R
0	RAM not initialized since last read	
1	RAM initialized. Cleared on read	

Table 75: RAM initialization

PDOVDD	Addr. 0x00; bit 1	R
0	VDD power down not occurred since last read	
1	VDD power down event has occurred. Cleared on read	

Table 76: VDD power down

MEMERR	Addr. 0x00; bit 2	R
0	RAM has not been changed since last validation	
1	RAM has changed and has not been validated	

Table 77: Memory validation

OVT	Addr. 0x00; bit 3	R
0	No overtemperature event has occurred since last read	
1	Overtemperature event has occurred. Cleared on read	

Table 78: Overtemperature

OVC2	Addr. 0x00; bit 4	R
0	No overcurrent event at channel 2 has occurred since last read	
1	Overcurrent event at channel 2 has occurred. Cleared on read	

Table 79: Overcurrent channel 2

OVC1	Addr. 0x00; bit 5	R
0	No overcurrent event at channel 1 has occurred since last read	
1	Overcurrent event at channel 1 has occurred. Cleared on read	

Table 80: Overcurrent channel 1

OSCERR	Addr. 0x00; bit 6	R
0	Oscillator functioning OK	
1	Watchdog timeout set on oscillator failure. Cleared on read	

Table 81: Oscillator watchdog

CFGTIMO	Addr. 0x00; bit 7	R
0	iC-HT not in *Configuration Mode* or *Timeout* did not happened till now	
1	iC-HT in *Configuration Mode* and *Timeout* happened. Laser switched off.	

Table 82: Configuration timeout

MAPC1	Addr. 0x01; bit 0	R
0	Channel 1 is off at the precise reading moment	
1	Channel 1 is on at the precise reading moment	

Table 83: EC1 pin state

MONC1	Addr. 0x01; bit 1	R
0	Channel 1 has not been switched on since last read	
1	Channel 1 has been switched on at least once. Cleared on read	

Table 84: Monitor channel 1

LDKSAT1	Addr. 0x01; bit 2	R
0	Channel 1 LDK saturation voltage not reached.	
1	Channel 1 LDK saturation voltage reached at least once, cleared on read	

Table 85: LDK1 saturation

MAPC2	Addr. 0x01; bit 4	R
0	Channel 1 is off at the precise reading moment	
1	Channel 1 is on at the precise reading moment	

Table 86: EC2 pin state

MONC2	Addr. 0x01; bit 5	R
0	Channel 2 has not been switched on since last read	
1	Channel 2 has not been switched on since last read	

Table 87: Monitor channel 2

LDKSAT2	Addr. 0x01; bit 6	R
0	Channel 2 LDK saturation voltage not reached.	
1	Channel 2 LDK saturation voltage reached at least once, Cleared on read	

Table 88: LDK2 saturation

Measurement registers

TEMP	Addr. 0x02; bit 7:0	R
0x00	Minimum temperature	
0xFF	Maximum temperature	

Table 89: Chip temperature

ADC1	Addr. 0x03/04; bit 9:0	R
0x000	ADC minimum value	
0x3FF	ADC maximum value	

Table 90: ADC channel 1

ADC2	Addr. 0x05/06; bit 9:0	R
0x000	ADC minimum value	
0x3FF	ADC maximum value	

Table 91: ADC channel 2

Channel 1 configuration registers

EACC1	Addr. 0x10; bit 0	R/W 0
0	APC mode enabled for channel 1 (light power regulation)	
1	ACC mode enabled for channel 1 (laser current regulation)	

Table 92: Enable APC/ACC channel 1

ECIE1	Addr. 0x10; bit 1	R/W 0
0	External CI capacitor for channel 1 disconnected	
1	External CI capacitor for channel 1 connected	

Table 93: Enable external CI capacitor channel 1

DISP1	Addr. 0x10; bit 2	R/W 0
0	PLR enabled for channel 1	
1	PLR disabled for channel 1	

Table 94: Disable PLR channel 1

DISC1	Addr. 0x10; bit 3	R/W 1
0	Channel 1 can be enabled by EC1 pin	
1	Channel 1 cannot be enabled by EC1 pin	

Table 95: Disable channel 1

EOC1	Addr. 0x10; bit 4	R/W 1
0	Channel 1 regulator offset compensation disabled	
1	Channel 1 regulator offset compensation enabled	

Table 96: Enable offset compensation channel 1

ADCC1(2:0)	Addr. 0x10; bit 7:5	R/W 000
0xx	Channel 1 ADC disabled	
100	Channel 1 ADC sourced by V(MDA1), ADSNF1 = 0	
100	Channel 1 ADC sourced by V(PLR1), ADSNF1 = 1	
101	Channel 1 ADC sourced by V(VB)	
110	Channel 1 ADC sourced by V(VDD)	
111	Channel 1 ADC sourced by V(LDK1)	

Table 97: ADC source selection channel 1

ILIM1	Addr. 0x11; bit 7:0	R/W 0xFF
0x0A	Channel 1 overcurrent threshold set to the minimum current	
...	Channel 1 overcurrent threshold set to $Ilim = (\Delta I(LDK) \cdot n)$, n from 10 to 255	
0xFF	Channel 1 overcurrent threshold set to the maximum current	

Table 98: Overcurrent threshold configuration channel 1

RMD1	Addr. 0x12; bit 7:0	R/W 0xFF
0x00	PLR1 set to the minimum resistance	
...	PLR1 resistor set to $Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$, n from 0 to 255	
0xFF	PLR1 resistor set to the maximum resistance	

Table 99: MDA resistor channel 1

COMP1	Addr. 0x13; bit 6:4	R/W 011
000	Minimum regulator delay compensation for channel 1, slower response	
...		
111	Maximum regulator delay compensation for channel 1, faster response	

Table 100: Regulator delay compensation channel 1

RLDKS1	Addr. 0x13; bit 3:2	R/W 00
00	V(LDK1) < 0.5 V sets the LDKSAT1 alarm bit	
01	V(LDK1) < 0.8 V sets the LDKSAT1 alarm bit	
10	V(LDK1) < 1.0 V sets the LDKSAT1 alarm bit	
11	V(LDK1) < 1.2 V sets the LDKSAT1 alarm bit	

Table 101: LDK saturation threshold selection channel 1

REF1	Addr. 0x13/14; bit 9:0	R/W 0x000
0x000	Channel 1 regulator reference voltage set to minimum voltage	
...	Channel 1 regulator reference voltage set to $Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}$, n from 0 to 1023	
0x3FF	Channel 1 regulator reference voltage set to maximum voltage	

Table 102: Regulator voltage reference channel 1

RACC1	Addr. 0x1A; bit 0	R/W 0
0	Current range high for channel 1	
1	Current range low for channel 1	

Table 103: Current range configuration channel 1

ADSNF1	Addr. 0x1A; bit 2	R/W 0
0	ADC measurement MDA1 pad (force)	
1	ADC measurement PLR1 (sense)	

Table 104: ADC channel 1 sense/force selection

Channel 2 configuration registers

EACC2	Addr. 0x15; bit 0	R/W 0
0	APC mode enabled for channel 2 (light power regulation)	
1	ACC mode enabled for channel 2 (laser current regulation)	

Table 105: Enable APC/ACC channel 2

ECIE2	Addr. 0x15; bit 1	R/W 0
0	External CI capacitor for channel 2 disconnected	
1	External CI capacitor for channel 2 connected	

Table 106: Enable external CI capacitor channel 2

DISP2	Addr. 0x15; bit 2	R/W 0
0	Internal resistor at MDA2 enabled for channel 2	
1	Internal resistor at MDA2 disabled for channel 2	

Table 107: Disable PLR channel 2

DISC2	Addr. 0x15; bit 3	R/W 1
0	Channel 2 can be enabled by EC2 pin	
1	Channel 2 cannot be enabled by EC2 pin	

Table 108: Disable channel 2

EOC2	Addr. 0x15; bit 4	R/W 1
0	Channel 2 regulator offset compensation disabled	
1	Channel 2 regulator offset compensation enabled	

Table 109: Enable offset compensation channel 2

ADCC2(2:0)	Addr. 0x15; bit 7:5	R/W 000
0xx	Channel 2 ADC disabled	
100	Channel 2 ADC sourced by V(MDA2), ADSNF2 = 0	
100	Channel 2 ADC sourced by V(PLR2), ADSNF2 = 1	
101	Channel 2 ADC sourced by V(VB)	
110	Channel 2 ADC sourced by V(VDD)	
111	Channel 2 ADC sourced by V(LDK2)	

Table 110: ADC source selection channel 2

ILIM2	Addr. 0x16; bit 7:0	R/W 0xFF
0x0A	Channel 2 overcurrent threshold set to the minimum current	
...	Channel 2 overcurrent threshold set to $Ilim = (\Delta I(LDK) \cdot n)$, n from 10 to 255	
0xFF	Channel 2 overcurrent threshold set to the maximum current	

Table 111: Overcurrent threshold configuration channel 2

RMD2	Addr. 0x17; bit 7:0	R/W 0xFF
0x00	PLR2 resistor set to the minimum resistance	
...	PLR2 resistor set to $Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$, n from 0 to 255	
0xFF	PLR2 resistor set to the maximum resistance	

Table 112: MDA resistor channel 2

COMP2	Addr. 0x18; bit 6:4	R/W 011
000	Minimum regulator delay compensation for channel 2, slower response	
...		
111	Maximum regulator delay compensation for channel 2, faster response	

Table 113: Regulator delay compensation channel 2

RLDKS2	Addr. 0x18; bit 3:2	R/W 00
00	V(LDK2) < 0.5 V sets the LDKSAT2 alarm bit	
01	V(LDK2) < 0.8 V sets the LDKSAT2 alarm bit	
10	V(LDK2) < 1.0 V sets the LDKSAT2 alarm bit	
11	V(LDK2) < 1.2 V sets the LDKSAT2 alarm bit	

Table 114: LDK saturation threshold selection channel 2

REF2	Addr. 0x18/19; bit 9:0	R/W 0x000
0x000	Channel 2 regulator reference voltage set to minimum voltage	
...	Channel 2 regulator reference voltage set to $Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}$, n from 0 to 1023	
0x3FF	Channel 2 regulator reference voltage set to maximum voltage	

Table 115: Regulator voltage reference channel 2

RACC2	Addr. 0x1A; bit 4	R/W 0
0	Current range high for channel 2	
1	Current range low for channel 2	

Table 116: Current range configuration channel 2

ADSNF2	Addr. 0x1A; bit 6	R/W 0
0	ADC measurement MDA2 pad (force)	
1	ADC measurement PLR2 (sense)	

Table 117: ADC channel 2 sense/force selection

General configuration registers

RDCO	Addr. 0x1B; bit 5:0	R/W 0x02
0x00	No current	
...		
0x3F	140 µA Typ (see spec point D01)	

Table 118: DCO current control

MERGE	Addr. 0x1B; bit 6	R/W 0
0	Channel 1 and 2 operate independently	
1	Power transistor from channel 2 usable in parallel with channel 1, regulation made by channel 1.	

Table 119: Channel combination

MODE(1:0)	Addr. 0x1C; bit 1:0	R/W 01
00	Not allowed, signaled as memory error	
01	Chip set in operation mode (apply configuration, latch transparent)	
10	Chip set in configuration mode (hold previous configuration)	
11	Not allowed, signaled as memory error	

Table 120: Configuration and operation mode

MOSCERR	Addr. 0x1D; bit 0	R/W 0
0	Oscillator error (watchdog) will be signaled at NCHK	
1	Oscillator error (watchdog) will not be signaled at NCHK	

Table 121: Oscillator watchdog error mask

MMONC	Addr. 0x1D; bit 1	R/W 1
0	MONC1 and MONC2 event will be signaled at NCHK	
1	MONC1 and MONC2 event will not be signaled at NCHK	

Table 122: Monitor channel 1 and 2 event mask

MLDKSAT1	Addr. 0x1D; bit 2	R/W 1
0	LDKSAT1 event will be signaled at NCHK	
1	LDKSAT1 event will not be signaled at NCHK	

Table 123: LDK saturation error mask channel 1

MLDKSAT2	Addr. 0x1D; bit 3	R/W 1
0	LDKSAT2 event will be signaled at NCHK	
1	LDKSAT2 event will not be signaled at NCHK	

Table 124: LDK saturation error mask channel 2

SOVT	Addr. 0x1D; bit 4	R/W 0
0	No overtemperature event is simulated.	
1	Overtemperature event simulated.	

Table 125: Simulate overtemperature

SOVC1	Addr. 0x1D; bit 5	R/W 0
0	No Overcurrent event at channel 1 is simulated.	
1	Overcurrent event at channel 1 simulated.	

Table 126: Simulate overcurrent channel 1

SOVC2	Addr. 0x1D; bit 6	R/W 0
0	No overcurrent event at channel 2 is simulated.	
1	Overcurrent event at channel 2 simulated.	

Table 127: Simulate overcurrent channel 2

SOSCERR	Addr. 0x1D; bit 7	R/W 0
0	No oscillator error simulated.	
1	Oscillator error simulated (watchdog timeout).	

Table 128: Simulate oscillator error

REVISION HISTORY

Rel	Rel.Date	Chapter	Modification	Page
A1	13-02-22		Initial Release.	

Rel	Rel.Date	Chapter	Modification	Page
B1	15-02-09	ELECTRICAL CHARACTERISTICS	Item 001: VB max updated from 8 V to 11 V.	6
		ELECTRICAL CHARACTERISTICS	Item 107: Laser overcurrent shutdown threshold updated from 93mA to 80mA	6
		ELECTRICAL CHARACTERISTICS	Item 108: Shutdown threshold resolution updated from 3 mA to 5 mA Item 108: Shutdown threshold resolution updated from 0.3 mA to 0.5 mA	6
		ELECTRICAL CHARACTERISTICS	Item 114: LDKx ACC mode current updated from 60 mA to 50 mA Item 114: LDKx ACC mode current updated from 750 mA to 650 mA Item 114: LDKx ACC mode current updated typical from 905 mA to 750 mA	7
		ELECTRICAL CHARACTERISTICS	Item 115: added TK -1500 ppm/K min, -500 ppm/K typ., 0 ppm/K max	7
		ELECTRICAL CHARACTERISTICS	Item 302: Percentual voltage increments updated from 0.05% to 0.1%	7
		ELECTRICAL CHARACTERISTICS	Item 403: Leakage Current at NCHK updated from ±10 to ±1	7
		ELECTRICAL CHARACTERISTICS	Item 602: Input Threshold Voltage at 2.8 V updated from 0.7 V to 0.6 V	7
		ELECTRICAL CHARACTERISTICS	Item B02: Overtemperature Release updated from 160 °C to 165 °C	8
		OPERATING AND STANDBY MODES	EMC and INS open pin description updated Web link to iC-WK iC-WKL updated	10
		MICROCONTROLLER MODE	MAPCx description updated Figure 10 updated with more details	20
		COMBINING BOTH CHANNELS	ILIM1 and REF1 tables added	22
		SERIAL COMMUNICATION INTERFACES	Figure 14: I^2C frames updated	24
		PARAMETERS	Table 81: MAPC1 description updated Table 84: MAPC2 description updated	40
		PARAMETERS	Table 114: RACC2 updated	42
		PARAMETERS	Table 120: MMONC description updated	43

ORDERING INFORMATION

Type	Package	Order Designation
iC-HT	QFN28 5 mm x 5 mm	iC-HT QFN28-5x5
Evaluation Board	100 mm x 80 mm eval board	iC-HT EVAL HT1D

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