iC-DY6818

preliminary

32 BIT SERIAL INPUT LATCHED PUSH/PULL DRIVER

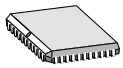
FEATURES

- Pin compatible with Allegro A6818
- 32 bit shift register
- Shift register with data latches and control circuitry
- ±25 mA output current
- 36 V output drivers
- Drivers shut down (tri-state) with over temperature and undervoltage
- Error (NERR) signal with open-drain output
- Direct interfacing with microprocessor based systems
- Integrated free-wheeling diode for inductive loads
- Typical serial data input rates up to 33 MHz

APPLICATIONS

- Driving bi-stable relays
- Peripheral power driver applications
- Microprocessor based systems

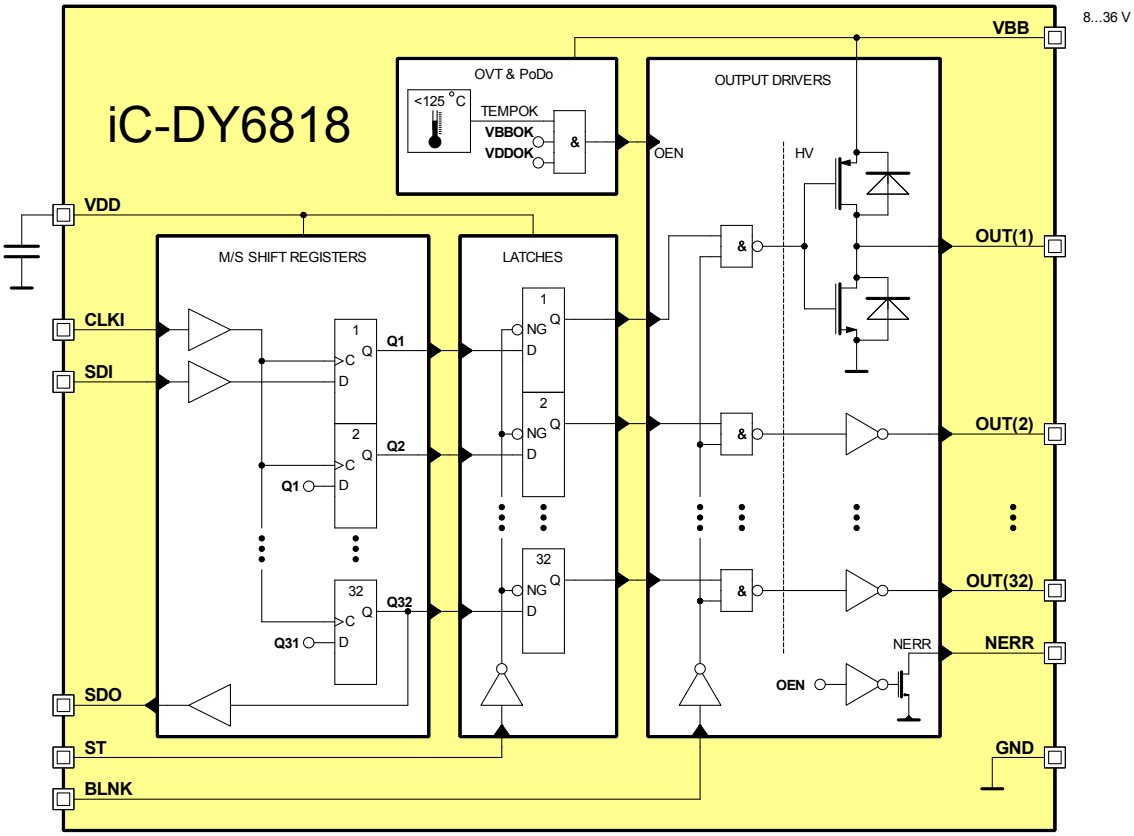
PACKAGES



PLCC44

QFN48-7x7
(on request)

BLOCK DIAGRAM



DESCRIPTION

iC-DY6818 is a 32 bit shift register with 32 output channels with min. 25 mA per channel. The typical serial data input frequency is 33 MHz max.

Output channel supply ranges from 8 to 36 V and input channel supply from 3.3 to 5.5 V for industrial applications.

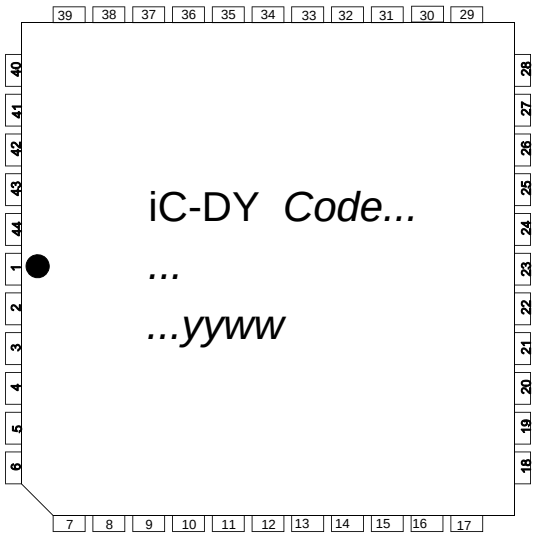
Integrated free-wheeling diodes at the output channels allow operation of inductive loads.

iC-DY6818 allows for daisy chaining of multiple devices.

The iC-DY6818 is pin compatible with the A6818.

PACKAGING INFORMATION

PIN CONFIGURATION PLCC44



PIN FUNCTIONS

No.	Name	Function
1	VBB	Load Supply
2	SDO	Serial Data Output
3	OUT(32)	Driver Output 32
4	OUT(31)	Driver Output 31
5	OUT(30)	Driver Output 30
6	NERR	Error Output (open drain, low active)
7	OUT(29)	Driver Output 29
8	OUT(28)	Driver Output 28
9	OUT(27)	Driver Output 27
10	OUT(26)	Driver Output 26
11	OUT(25)	Driver Output 25

PIN FUNCTIONS

No.	Name	Function
12	OUT(24)	Driver Output 24
13	OUT(23)	Driver Output 23
14	OUT(22)	Driver Output 22
15	OUT(21)	Driver Output 21
16	OUT(20)	Driver Output 20
17	OUT(19)	Driver Output 19
18		n/c
19	OUT(18)	Driver Output 18
20	OUT(17)	Driver Output 17
21	BLNK	Blanking
22	GND	Ground
23	CLKI	Clock Input
24	ST	Strobe
25	OUT(16)	Driver Output 16
26	OUT(15)	Driver Output 15
27	OUT(14)	Driver Output 14
28		n/c
29		n/c
30	OUT(13)	Driver Output 13
31	OUT(12)	Driver Output 12
32	OUT(11)	Driver Output 11
33	OUT(10)	Driver Output 10
34	OUT(9)	Driver Output 9
35	OUT(8)	Driver Output 8
36	OUT(7)	Driver Output 7
37	OUT(6)	Driver Output 6
38	OUT(5)	Driver Output 5
39	OUT(4)	Driver Output 4
40	OUT(3)	Driver Output 3
41	OUT(2)	Driver Output 2
42	OUT(1)	Driver Output 1
43	SDI	Serial Data Input
44	VDD	Logic Supply

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VBB	Voltage at VBB		-0.7	36	V
G002	Vin	Input Voltage Range		-0.3	VDD + 0.3	V
G003	Tj	Operating Junction Temperature		-40	150	°C
G004	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VBB = 8...36 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip/Ambient	SMD assembly, no additional cooling areas		55		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: Ta = -40...125 °C, VDD = 3...5.5 V, VBB = 8...36 V; unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Logic Voltage		3		5.5	V
002	VBB	Permissible Driver Voltage		8		36	V
003	Idc(VBB)	Supply Current in VBB	All outputs high (no load) All outputs low		6 3	8 5	mA mA
004	Idd(VDD)	Logic Supply Current	All outputs high All outputs low		0.5 3	2 5	mA mA
005	Tab	Thermal Shutdown Threshold		125		185	°C
006	VDDon	VDD Power-On Threshold		2.3		3	V
007	VBB	VBB Power-On Threshold		7		8	V
008	fc	Maximum Clock Frequency		10	33		MHz
009	Vc()hi	Clamp Voltage hi at VBB, NERR and OUT(x) vs. GND	I() = 10 mA	36			V
010	Vc()lo	Clamp Voltage lo at VBB, NERR and OUT(x) vs. GND	I() = -10 mA			-36	V
011	Vc()hi	Clamp Voltage hi at SDO, BLNK, CLKI, ST, SDI and VDD vs. GND	I() = 1 mA	7			V
012	Vc()lo	Clamp Voltage lo at SDO, BLNK, CLKI, ST, SDI and VDD vs. GND	I() = -1 mA			-0.5	V
Digital Inputs CLKI, SDI, ST, BLNK							
101	Vt()hi	Input Threshold Voltage hi				68	% VDD
102	Vt()lo	Input Threshold Voltage lo		30			% VDD
103	Vin()hys	Input Hysteresis		600	900		mV
104	Ipd()	Pull-Down Current at CLKI, SDI, ST	V() = 1 V...VDD	2.1		75	µA
105	Ipdb()	Pull-Down Current at BLNK	V() = 1 V...VDD	1		5	µA
106	tdis(BLNK)	Propagation Delay Disable Blanking-to-Output	CL = 30 pF		0.7	2	µs
107	ten(BLNK)	Propagation Delay Enable Blanking-to-Output	CL = 30 pF		1.8	3	µs
108	tdis(ST)	Propagation Delay Disable Strobe-to-Output	RL = 2.3 kΩ, CL = 30 pF		0.7	2	µs
109	ten(ST)	Propagation Delay Enable Strobe-to-Output	RL = 2.3 kΩ, CL = 30 pF		1.8	3	µs
Error Output NERR							
201	I(NERR)	Current in NERR	V(NERR) 8...36 V, error mode	2		12	mA
202	Vsatlo()	Saturation Voltage lo at NERR	I(NERR) = 1 mA			0.4	V
Driver Outputs OUT(x), x = 1...32							
301	Icex()	Output Leakage Current	error condition, output tri-state; V() = 0...VBB	-10	0	+10	µA
302	Vs()hi	Saturation Voltage hi	Vs()hi = VBB − V(), I() = -25 mA			1.8	V
303	Vs()lo	Saturation Voltage lo	I() = 25 mA			1.8	V
304	Isc()lo	Short-Circuit Current lo	V() = 1.8 V...VBB	25		80	mA
305	Isc()hi	Short-Circuit Current hi	V() = 0...VBB − 1.8 V	-80		-25	mA
306	Vfw()lo	Freewheeling Voltage lo	I() = -25 mA, referenced to GND	-1.5			V
307	Vfw()hi	Freewheeling Voltage hi	I() = 25 mA, referenced to (OUT − VBB)			1.5	V
308	tf()	Fall Time	RL = 2.3 kΩ, CL = 30 pF	2.4		12	µs
309	tr()	Rise Time	RL = 2.3 kΩ, CL = 30 pF	2.4		12	µs

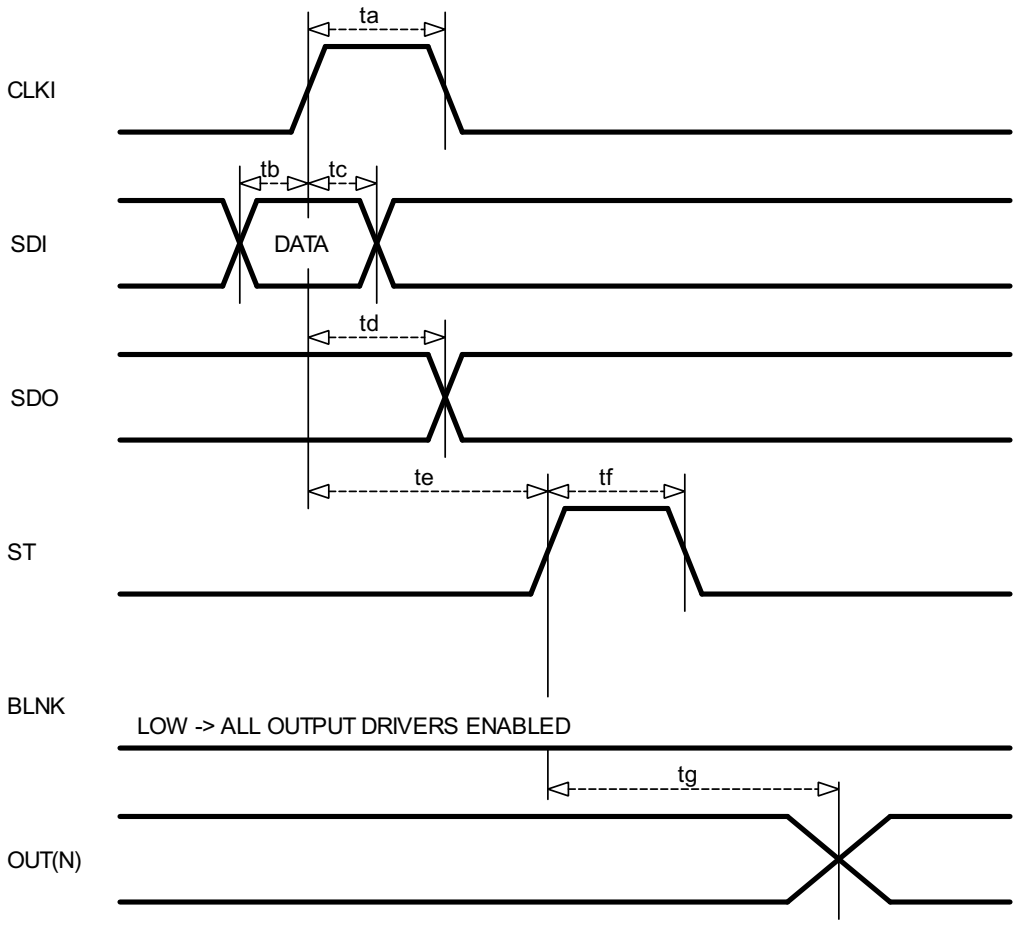
ELECTRICAL CHARACTERISTICS

Operating Conditions: Ta = -40...125 °C, VDD = 3...5.5 V, VBB = 8...36 V; unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Serial Output SDO							
401	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(), I() = -4 mA			450	mV
402	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
403	Isc()hi	Short-Circuit Current hi	V() = 0...VDD	-115			mA
404	Isc()lo	Short-Circuit Current lo	V() = 0...VDD			100	mA
405	tdcdo()	Propagation Delay CLK-to-SDO	Iout = ±200 µA		50		ns

TIMING DIAGRAM

The following timing requirements and specifications are referencing a 10 MHz clock.



ta = 50 ns
tb = 25 ns
tc = 25 ns
td = 50 ns
te = 100 ns
tf = 50 ns
tg = 1.8 us

Figure 1: Example of typical 10 MHz timing diagram

SERIAL CONNECTION OF MULTIPLE CHIPS

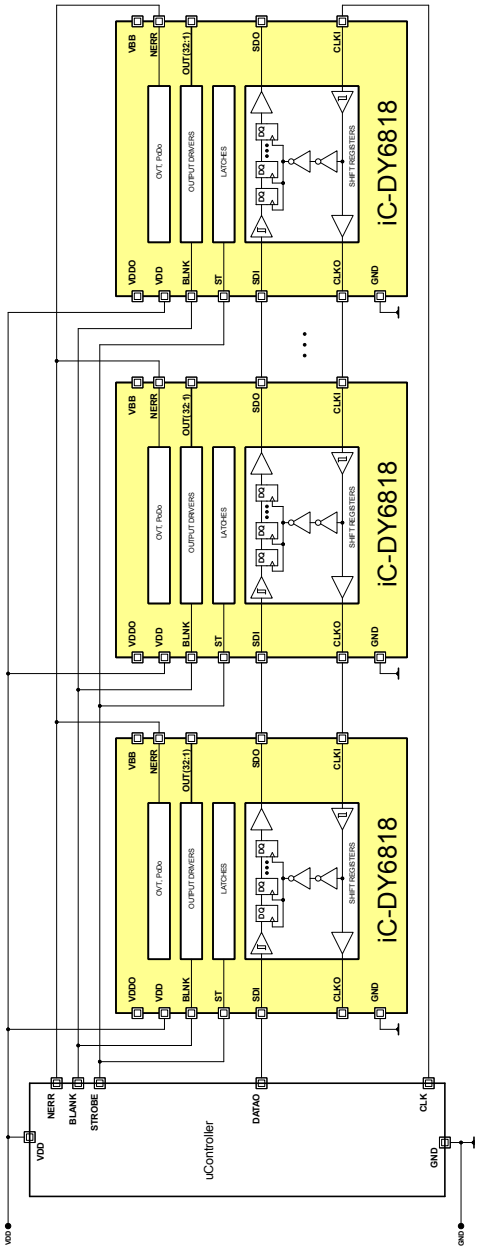


Figure 2: Serial connection of multiple chips

ORDERING INFORMATION

Type	Package	Order Designation
iC-DY6818	PLCC44 QFN48 7 mm x 7 mm (on request)	iC-DY PLCC44 iC-DY QFN48-7x7

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (0) 61 35 - 92 92 - 0
Fax: +49 (0) 61 35 - 92 92 - 192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.com/sales_partners