iC-HX

3-CHANNEL DIFFERENTIAL COLD LINE DRIVER

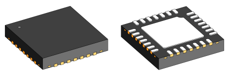
FEATURES

- 6 current-limited and short-circuit-proof push-pull drivers
- Differential 3-channel operation selectable
- Integrated impedance adaption for 30 to 140 Ω lines
- Wide power supply range from 4 to 40 V
- 200 mA output current (at VB = 24 V)
- Low output saturation voltage (< 0.4 V at 30 mA)
- Compatible with TIA/EIA standard RS-422
- Tristate switching of outputs enables use in buses
- Short switching times and high slew rates
- Low static power dissipation
- Dynamic power dissipation reduced with iC-xSwitch
- Schmitt trigger inputs with pull-down resistors, TTL and CMOS compatible; voltage-proof up to 40 V
- Thermal shutdown with hysteresis
- Error message trigger input TNER
- Open-drain error output NER, active low with excessive chip temperature and undervoltage at VCC or VB
- Operating temperature range from -40 to 125 °C

APPLICATIONS

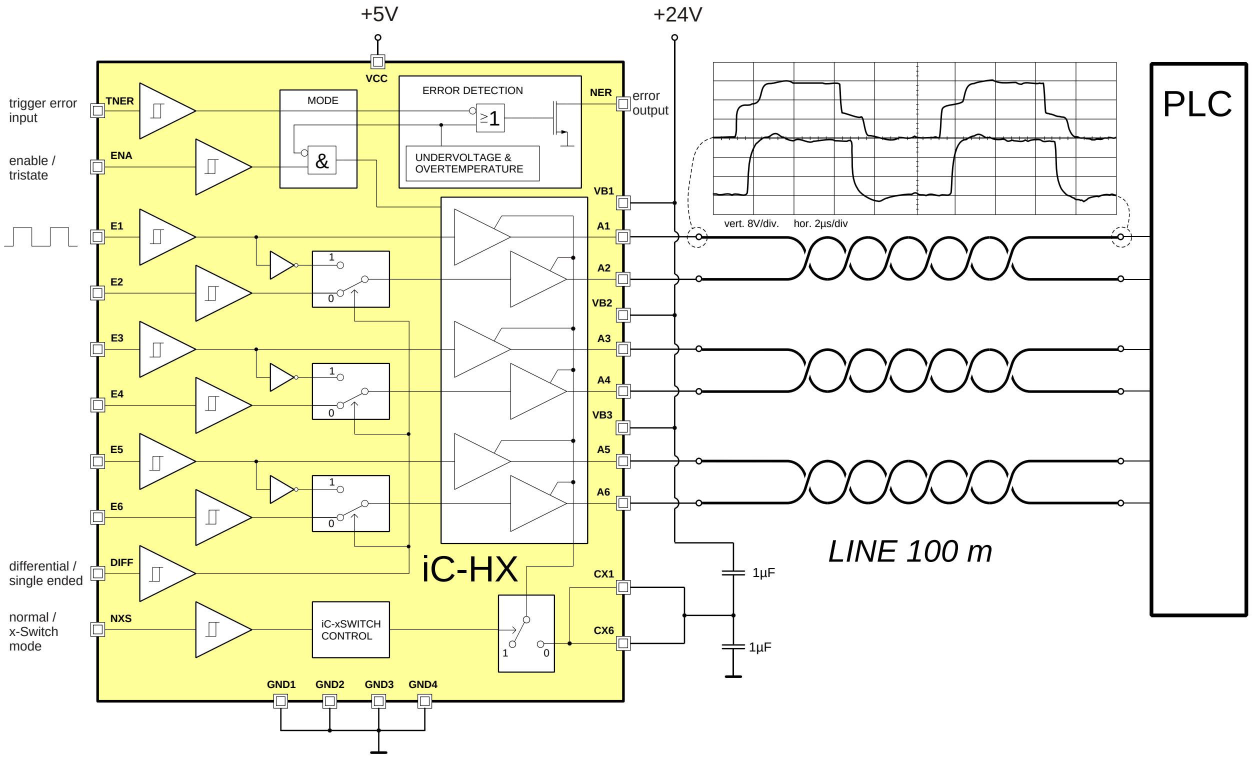
- Line drivers for 24 V control engineering
- Linear scales and encoders
- MR sensor systems

PACKAGES



QFN28 5 x 5 mm^2

BLOCK DIAGRAM



DESCRIPTION

iC-HX is a fast line driver with six independent channels and integrated impedance adaptation for 30 to 140 Ω lines.

Channels are paired for differential 3-channel operation by a high signal at the DIFF input, providing differential output signals for the three inputs E1, E3 and E5. All inputs are compatible with CMOS and TTL levels.

The push-pull output stages have a driver power of typically 200 mA from 24 V and are short-circuit-proof and current-limited, shutting down with excessive temperature. For bus applications the output stages can be switched to high impedance using input ENA.

To reduce the dynamic power dissipation in applications with long lines the iC-HX uses the iC-xSwitch.

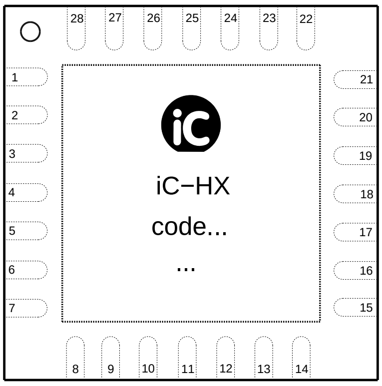
iC-HX monitors supply voltages VB and VCC and the chip temperature, switching all output stages to high impedance in the event of error and set NER active low. In addition, the device also monitors voltage differences at the pins VB1, VB2 and VB3 and generates an error signal if the absolute value exceeds 0.75 V.

The open-drain output NER allows the device to be wired-ORed to the relevant NER error outputs of other iC-HXs and iC-DLs. Via input TNER the message outputs of other ICs can be extended to generate system error messages. NER switches to high impedance if supply voltage VCC ceases to be applied.

The device is protected against ESD.

PACKAGING INFORMATION QFN28 to JEDEC Standard

PIN CONFIGURATION QFN28 5 x 5 mm^2



PIN FUNCTIONS

No.	Name	Function
1	E1	Input Channel 1
2	E2	Input Channel 2
3	E3	Input Channel 3
4	n.c.	
5	E4	Input Channel 4
6	E5	Input Channel 5
7	E6	Input Channel 6
8	VCC	+5 V Supply
9	CXS6	Capacitor iC-xSwitch
10	TNER	Error Input, low active
11	NER	Error Output, active low
12	A6	Output Channel 6
13	GND4	Ground
14	VB3	+4.5 ... 40 V Power Supply
15	A5	Output Channel 5
16	GND3	Ground
17	A4	Output Channel 4
18	VB2	+4.5 ... 40 V Power Supply
19	A3	Output Channel 3
20	GND2	Ground
21	A2	Output Channel 2
22	VB1	+4.5 ... 40 V Power Supply
23	GND1	Ground
24	A1	Output Channel 1
25	NXS	Enable iC-xSwitch, low active
26	ENA	Enable Input, high active
27	CXS1	Capacitor iC-xSwitch
28	DIFF	Differential Mode Input, high active

The pins VB1, VB2 and VB3 must be connected to the same driver supply voltage VB. The pins GND1, GND2, GND3 and GND4 must be connected to GND. To improve heat dissipation, the *thermal pad* at the bottom of the package should be joined to an extended copper area which must have GND potential.

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed. Absolute Maximum Ratings are no Operating Conditions. Integrated circuits with system interfaces, e.g. via cable accessible pins (I/O pins, line drivers) are per principle endangered by injected interferences, which may compromise the function or durability. The robustness of the devices has to be verified by the user during system development with regards to applying standards and ensured where necessary by additional protective circuitry. By the manufacturer suggested protective circuitry is for information only and given without responsibility and has to be verified within the actual system with respect to actual interferences.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		0	7	V
G002	VBx	Voltages at VB1, VB2, VB3		0	40	V
G003	V()	Voltage at E1...6, A1...6, DIFF, ENA, TNER		0	40	V
G004	I(Ax)	Current in Ax (x=1...6)		-800	800	mA
G005	I(Ex)	Current in E1...E6, Diff, ENA, TNER		-4	4	mA
G006	V(NER)	Voltage at NER		0	40	V
G007	I(NER)	Current in NER		-4	25	mA
G008	V()	ESD Suceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G009	Tj	Operating Junction Temperature		-40	140	°C
G010	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating conditions: VB1. . . 3 = 4.5. . . 40 V, VCC = 4.5. . . 5.5 V or VB1. . . 3 = VCC = 4. . . 5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	surface mounted, *thermal pad* soldered to approx. 2 cm² heat sink		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB1...3 = 4.5...32 V, VCC = 4...5.5 V, Tj = -40...140 °C, unless otherwise noted
input level lo = 0...0.45 V, hi = 2.4 V...VCC, timing diagram see Fig. 2

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VBx	Supply Voltage Range (Driver)	for VB1...3 voltages below 7V use setup given in Fig. 1	4		40	V
002	I(VBx)	Supply Current in VB1...3	Ax = lo			8	mA
003	I(VBx)	Supply Current in VB1...3	Ax = hi			8	mA
004	I(VBx)	Supply Current in VB1, Outputs A1...2 Tri-State	ENA = lo, V(A1...2) = -0.3...(VB + 0.3 V)			4	mA
005	I(VBx)	Supply Current in VB2...3, Outputs A3...6 Tri-State	ENA = lo, V(A3...6) = -0.3...(VB + 0.3 V)			2	mA
006	IO(Ax)	Output Leakage Current	ENA = lo, V(Ax) = 0 ... VB	-50		50	µA
007	VCC	Supply Voltage Range (Logic)	for VB1...3 voltages below 7V use setup given in Fig. 1	4		5.5	V
008	I(VCC)	Supply Current in VCC	ENA = hi, Ax = lo			10	mA
009	Vc()lo	Clamp Voltage low at pins VB1...3, A1...6, E1...6, DIFF, ENA TNER, NER, VCC	I() = -10 mA, all other pins open	-1.2		-0.35	V
010	Vc()hi	Clamp Voltage high at pins VB1...3, A1...6, E1...6, DIFF, ENA TNER, NER	I() = 1 mA, all other pins open	41		64	V
011	I(VB)	Supply Current in VB1...3	ENA = hi, f(E1...6) = 1 MHz			50	mA
Driver Outputs A1...6, Low-Side-action (x = 1...6)							
101	Vs(Ax)lo	Saturation Voltage low	I(Ax) = 10 mA, Ax = low			0.2	V
102	Vs(Ax)lo	Saturation Voltage low	I(Ax) = 30 mA, Ax = low			0.4	V
103	Isc(Ax)lo	Short circuit current low	V(Ax) = 1.5 V	30	50	70	mA
104	Isc(Ax)lo	Short circuit current low	V(Ax) = VB, Ax = low			800	mA
105	Rout(Ax)	Output resistance	VB = 10...40 V, V(Ax) = 0.5 * VB	40	75	100	Ohm
106	SR(Ax)lo	Slew Rate low	VB = 40 V, Cl(Ax) = 100 pF	200		1000	V/µs
107	Vc()lo	Free Wheel Clamp Voltage low	I(Ax) = -100 mA	-1.4		-0.5	V
Driver Outputs A1...6, High-Side-action (x = 1...6)							
201	Vs(Ax)hi	Saturation Voltage high	Vs(Ax)hi = VB - V(Ax), I(Ax) = -10 mA, Ax = hi			0.2	V
202	Vs(Ax)hi	Saturation Voltage high	Vs(Ax)hi = VB - V(Ax), I(Ax) = -30 mA, Ax = hi			0.5	V
203	Isc(Ax)hi	Short circuit current high	V(Ax) = VB - 1.5 V, Ax = hi	-70	-50	-30	mA
204	Isc(Ax)hi	Short circuit current high	V(Ax) = 0 V, Ax = hi	-800			mA
205	Rout(Ax)hi	Output resistance	VB = 10...40 V, V(Ax) =0.5 * VB	40	75	100	Ohm
206	SR(Ax)hi	Slew Rate high	VB= 40 V, Cl(Ax) = 100 pF	200		1000	V/µs
207	Vc(Ax)hi	Free Wheel Clamp Voltage high	I(Ax) = 100 mA, VB = VCC = GND	0.5		1.4	V
iC-xSwitch CXS1, CXS6, A1 . . . 6, VB1 . . . 3							
301	VBxs,on	Turn-on threshold iC-xSwitch				12.5	V
302	VBxs,off	Turn-off threshold iC-xSwitch		11			V
303	VBxs,hys	Hysteresis		150			mV
304	Ron()	On-resistance iC-xSwitch	VBx = 40 V, V(CXSx)= 20 V, I(Ax) = ± 350 mA			7	Ohm
305	Vth(Ax)hi	Higher threshold hi	VBx = 12.5 . . . 40 V			73	%VB
306	Vth(Ax)lo	Higher threshold lo	VBx = 12.5 . . . 40 V	63			%VB
307	Vth(Ax)hys	Higher hysteresis	VBx = 12.5 . . . 40 V	100			mV
308	Vtl(Ax)hi	Lower threshold hi	VBx = 12.5 . . . 40 V			40	%VB
309	Vtl(Ax)lo	Lower threshold lo	VBx = 12.5 . . . 40 V	30			%VB
310	Vtl(Ax)hys	Lower hysteresis	VBx = 12.5 . . . 40 V	100			mV
Switch control							
401	tdmin	Minimum time for line reflection	VB = 12.5 . . . 40 V	100	200	300	ns
402	tXSon(Ax)	On-time iC-xSwitch	f(Ex) = 500KHz, td = 800 ns, VB = 12.5 . . . 40 V	400		700	ns

ELECTRICAL CHARACTERISTICS

Operating Conditions: VB1...3 = 4.5...32 V, VCC = 4...5.5 V, Tj = -40...140 °C, unless otherwise noted
input level lo = 0...0.45 V, hi = 2.4 V...VCC, timing diagram see Fig. 2

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
403	tXSon(Ax)	On-time iC-xSwitch	f(Ex) = 100 KHz, td = 4 µs, VB = 12.5 . . . 40 V	3.1		3.9	µs
CXS-generation CXS1, CXS6							
501	V()	Voltage at CXS1, CXS6	VB = 12.5 . . . 40 V,I(CXSXx)= ± 100 µA	47	50	53	%VB
502	Isc()lo	Short circuit current lo	VB = 12.5 . . . 40 V, CXSx = 0 V	2		20	mA
503	Isc()hi	Short circuit current hi	VB = 12.5 . . . 40 V, CXSx = VB	-20		-2	mA
504	Vc()hi	Clamp Voltage hi	I() = 10 mA, VB = VCC = GND	0.5		1.4	V
505	Vth()hi	higher turn-off threshold iC-xSwitch	VB = 12.5 . . . 40 V			73	%VB
506	Vth()lo	higher turn-on threshold iC-xSwitch	VB = 12.5 . . . 40 V	63			%VB
507	Vth()hys	Hysteresis	Vth()hys = Vth()hi - Vth()lo	100			mV
508	Vtl()hi	lower turn-on threshold iC-xSwitch	VB = 12.5 . . . 40 V			40	%VB
509	Vtl()lo	lower turn-off threshold iC-xSwitch	VB = 12.5 . . . 40 V	30			%VB
510	Vtl()hys	Hysteresis	Vtl()hys = Vtl()hi - Vtl()lo	100			mV
Inputs E1...6, DIFF, ENA, TNER							
601	Vt()hi	Threshold Voltage high				2.1	V
602	Vt()lo	Threshold Voltage low		0.8			V
603	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi - Vt()lo	200	400	800	mV
604	Ipd()	Pull-Down-Current	V() = 0.8 V	10		80	µA
605	Ipd()	Pull-Down-Current	V() ≤ 40 V	15		160	µA
606	Il(E1. . . 6)	Leakage current at E1. . . 6	ENA = lo	-10		10	µA
Supply Voltage Control VB							
701	VBon	Threshold Value at VB for Undervoltage Detection on	|VB1 - VB2| & |VB2 - VB3| & |VB1 - VB3| < 0.75 V			3.95	V
702	VBoff	Threshold Value at VB for Undervoltage Detection off	|VB1 - VB2| & |VB2 - VB3| & |VB1 - VB3| < 0.75 V	3			V
703	VBhys	Hysteresis	VBhys = VBon - VBoff	150			mV
Supply Voltage Difference Control VB1...3							
801	Vth(VBx)	Threshold Condition for Supply Voltage Difference Control	ΔV(VBx) = MAX (|VB1 - VB2| , |VB2 - VB3| , |VB1 - VB3|) NER ⇒ low	0.75		1.85	V
Supply Voltage Control VCC							
901	VCCon	Threshold Value at VCC for Undervoltage Detection on				3.95	V
902	VCCoff	Threshold Value at VCC for Undervoltage Detection off		3			V
903	VCChys	Hysteresis	VCChys = VCCon - VCCoff	100			mV
Temperatur Control							
A01	Toff	Thermal Shutdown Threshold	increasing temperature	145		175	°C
A02	Ton	Thermal Lock-on Threshold	decreasing temperature	130		165	°C
A03	Thys	Thermal Shutdown Hysteresis	Thys = Ton - Toff	4	12		°C
Error Output NER							
B01	Vs()	Saturation Voltage low at NER	I(NER) = 5 mA, NER = lo			0.6	V
B02	Isc()	Short Circuit Current low at NER	V(NER) = 2...40 V, NER = lo	6	12	20	mA
B03	IO()	Leakage Current at NER	V(NER) = 0 V...VB, NER = hi	-10		10	µA
B04	VCC	Supply Voltage for NER function	I(NER) = 5 mA, NER = lo, Vs(NER) < 0.6 V	2.9			V

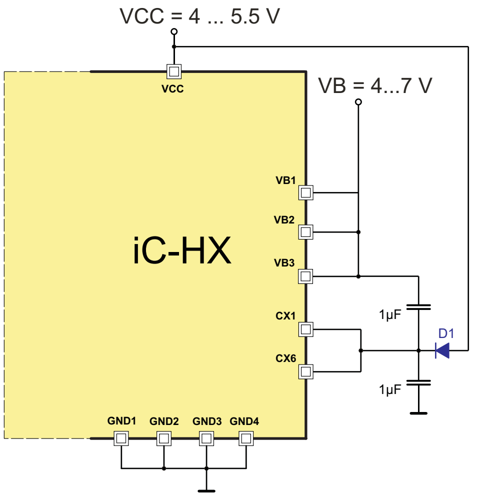


Figure 1: Operating setup for VBx voltages below 7V using additional diode D1 (1N4148 or equivalent)

OPERATING REQUIREMENTS

Operating Conditions: VB1...3 = 4.5...32 V, VCC = 4...5.5 V, Tj = -40...140 °C, unless otherwise noted
input level lo = 0...0.45 V, hi = 2.4 V...VCC, timing diagram see fig. 2

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Time Delays						
I001	tplh(E-A)	Propagation Delay Ex ⇒ Ax	DIFF = lo, Cl() = 100 pF		400	ns
I002	tphl(E-A)	Propagation Delay Ex ⇒ Ax	DIFF = lo, Cl() = 100 pF		200	ns
I003	Δtplh(Ax)	Propagation Delay Skew |A1 ⇒ A2|, |A3 ⇒ A4|, |A5 ⇒ A6|	DIFF = hi, Cl() = 100 pF		100	ns
I004	Δtphl(Ax)	Propagation Delay Skew |A1 ⇒ A2|, |A3 ⇒ A4|, |A5 ⇒ A6|	DIFF = hi, Cl() = 100 pF		100	ns
I005	tplh(ENA)	Propagation Delay ENA ⇒ Ax	Ex = hi, DIFF = lo, Cl() = 100 pF, Rl(Ax, GND) = 5 kΩ		300	ns
I006	tplh(ENA)	Propagation Delay ENA ⇒ Ax	Ex = lo, DIFF = lo, Cl() = 100 pF, Rl(VB, Ax) = 100 kΩ		200	ns
I007	tphl(ENA)	Propagation Delay ENA ⇒ Ax	Ex = lo, DIFF = lo, Rl(VB, Ax) = 5 kΩ		500	ns
I008	tphl(ENA)	Propagation Delay ENA ⇒ Ax	Ex = hi, DIFF = lo, Rl(Ax, GND) = 5 kΩ		500	ns
I009	tphl(DIFF)	Propagation Delay DIFF ⇒ A2, A4, A6	E1, E3, E5 = hi, Cl() = 100 pF		250	ns
I010	tplh(DIFF)	Propagation Delay DIFF ⇒ A2, A4, A6	E1, E3, E5 = lo, Cl() = 100 pF		400	ns
I011	tplh(TNER)	Propagation Delay TNER ⇒ NER	Rl(VB, NER) = 5 kΩ, Cl() = 100 pF		2	µs
I012	tpoff(VBx)	Turn-off delay, VBx ⇒ NER	| VBx - VBy | > Vth(VBx), x<>y, x, y = 1..3	0.3	3	µs

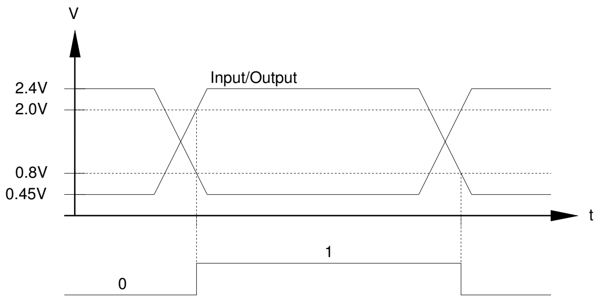


Figure 2: Reference levels for delays

DESCRIPTION

Line drivers for control engineering couple TTL- or CMOS-compatible digital signals with 24 V systems via cables. The maximum permissible signal frequency is dependent on the capacitive load of the outputs (cable length) or, more specifically, the power dissipation in iC-HX resulting from this. To avoid possible short circuiting the drivers are current-limited and shutdown with excessive temperature.

When the output is open the maximum output voltage corresponds to supply voltage VB (with the exception of any saturation voltages). Figure 3 gives the typical DC output characteristic of a driver as a function of the load. The differential output resistance is typically 75 Ω over a wide voltage range.

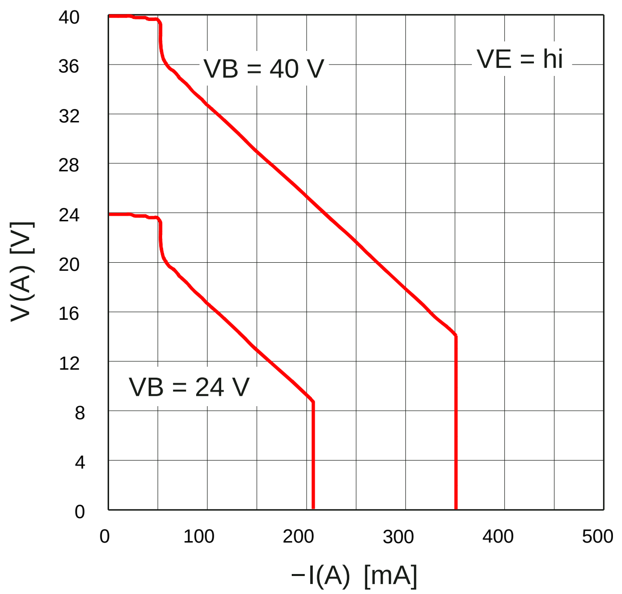


Figure 3: Load dependence of the output voltage (High-side stage)

Each open-circuited input is set to low by an internal pull-down current source; an additional connection to GND increases the device's immunity to interference. The inputs are TTL- and CMOS-compatible. Due to their high input voltage range, the inputs can also be set to high-level by applying VCC or VB.

LINE EFFECTS

In PLC systems data transmission using 24 V signals usually occurs without a matched line termination. A mismatched line termination generates reflections which travel back and forth if there is also no line adaptation on the driver side of the device. With rapid pulse trains transmission is disrupted. In iC-HX, however, further reflection of back travelling signals is prevented by an integrated impedance network, as shown in Figure 4.

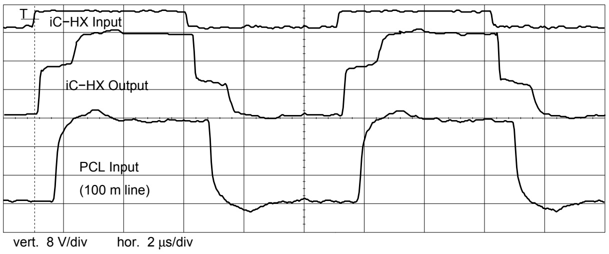


Figure 4: Reflections caused by a mismatched line termination

During a pulse transmission the amplitude at the iC-output initially only increases to half the value of supply voltage VB as the internal driver resistance and characteristic line impedance form a voltage divider. A wave with this amplitude is coupled into the line and experiences after a delay a total reflection at the high-impedance end of the line. At this position, the reflected wave superimposes with the transmitted wave and generates a signal with the double wave amplitude at the receiving device.

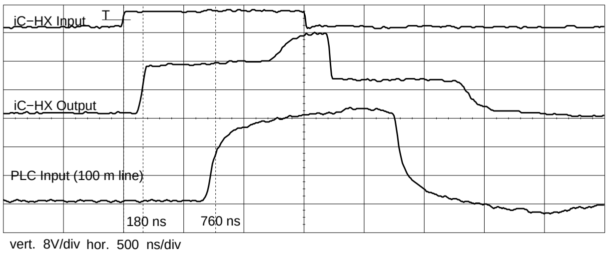


Figure 5: Pulse transmission and transit times

After a further delay, the reflected wave also increases the driver output to the full voltage swing. iC-HX's integrated impedance adapter prevents any further reflection and the achieved voltage is maintained along and at the termination of the line.

A mismatch between iC-HX and the transmission line influences the level of the signal wave first coupled into the line, resulting in reflections at the beginning of the line. The output signal may then have a number of graduations. Voltage peaks beyond VB or below GND are capped by integrated diodes. By this way, transmission lines with a characteristic impedance of between 30 and 140 Ω thus permit correct operation of the device.

iC-xSwitch

Power dissipation in the driver occurs with each switching edge when over the double signal run time the internal resistor forms a voltage divider with the characteristic line impedance and is proportional to the length of the connected line and the switching frequency. If the internal resistor is perfectly matched to the characteristic line impedance, the voltage divider generates half the supply voltage at the line input, only supplying the full voltage when an echo occurs. iC-HX exploits this behavior of the open line in order to reduce the power dissipation in the driver. A switch is triggered by applying the halved low-impedance supply voltage, buffered with capacitors, to the line input and terminated by applying the internal resistor shortly before the echo occurs. Power dissipation occurs regardless of the length of the connected line in the time between the application of the resistor to the line and the beginning of the echo. In order to control this process iC-HX must recognize the length of the connected line. The line is measured using an integrated procedure which evaluates the line echo. This principle of power dissipation reduction only functions when a single wave travels along the line. The maximum transmission frequency with a reduced power dissipation is directly proportional to the line length. If the transmission frequency is too high for the line length, iC-xSwitch is no longer used, resulting in increased power dissipation in the driver. The required halved supply voltage is generated internally in the chip and must be buffered by capacitors. On a rising edge current flows from the capacitor into the line and back into the capacitor on a falling edge. With the differential operation of two lines the currents flow from one line to the other and back again.

Figure 6 shows the three switches, the integrated resistor to match the characteristic line impedance and the connected line. VB is the positive power supply and VB/2 is the half of it. The control of the switches depends on the input signals of the device and the length of the connected line. With all enable-signals at lo-level the output A is high impedance (tristate).

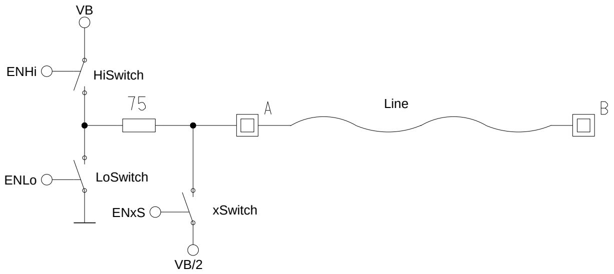


Figure 6: Circuit diagram with switches and line

Figures 7 and 8 show the input signal V(E), the switch trigger signals derived from this and the voltage curve at the beginning (A) and end (B) of the line at intervals t1 to t8. Figure 7 shows operation without iC-Xswitch. Power dissipation $\mathrm{P_D(HX)}$ occurs at intervals t1 to t4 and t5 to t8. Figure 8 describes operation with iC-xSwitch; power dissipation $\mathrm{P_D(HX)}$ occurs between t3 and t4 and t7 and t8. The mean power dissipation is significant for the warming of the device, which is proportional to the duty cycle. This results in a reduced power dissipation (at the same frequency), meaning there is less power dissipation with a shorter line or through the use of iC-xSwitch with a long line, for example.

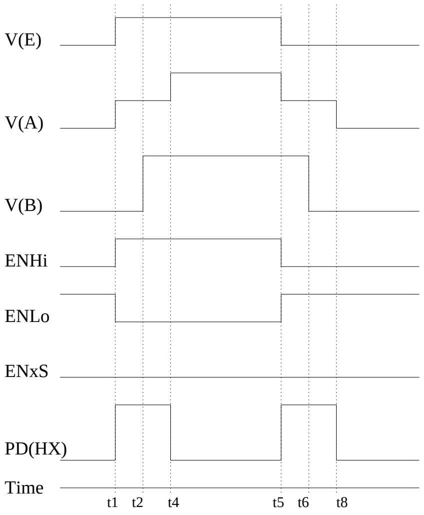


Figure 7: Power dissipation $\mathrm{P_D(HX)}$ without iC-xSwitch

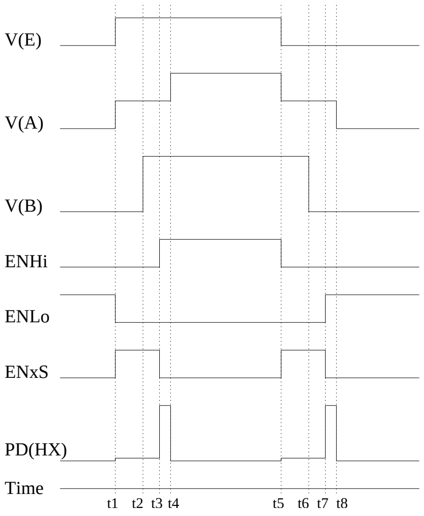


Figure 8: Power dissipation $\mathrm{P_D(HX)}$ with iC-xSwitch

An example for the power dissipation is given in figure 9. When xSwitch is not used by setting NXS to high, the iC-HX behaves like the iC-DL.

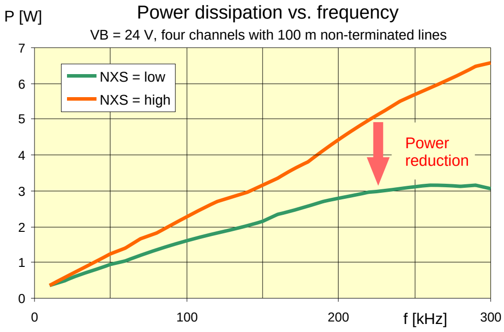


Figure 9: Power dissipation with and without xSwitch-Mode

DEMO BOARD

iC-HX is in a QFN28 package and comes with a demo board for test purposes. Figures 10 to 11 shows the wiring and the top of the demo board.

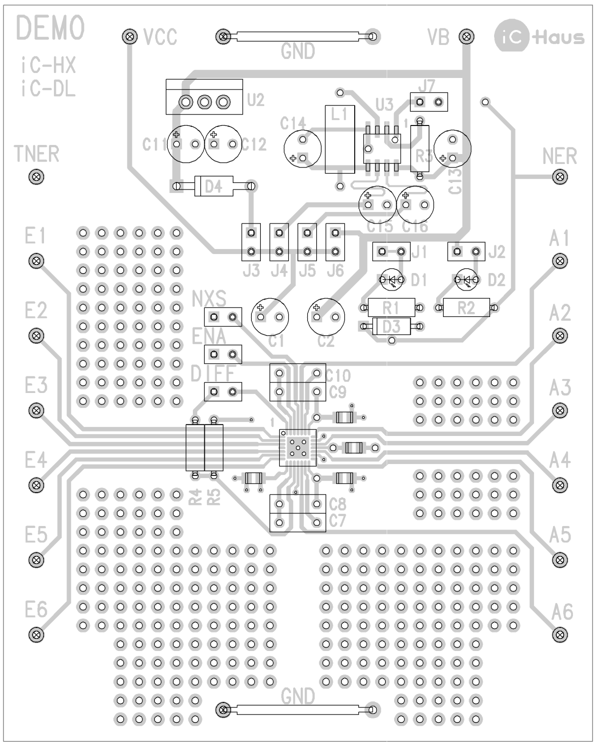


Figure 10: Demo-Board ,top view

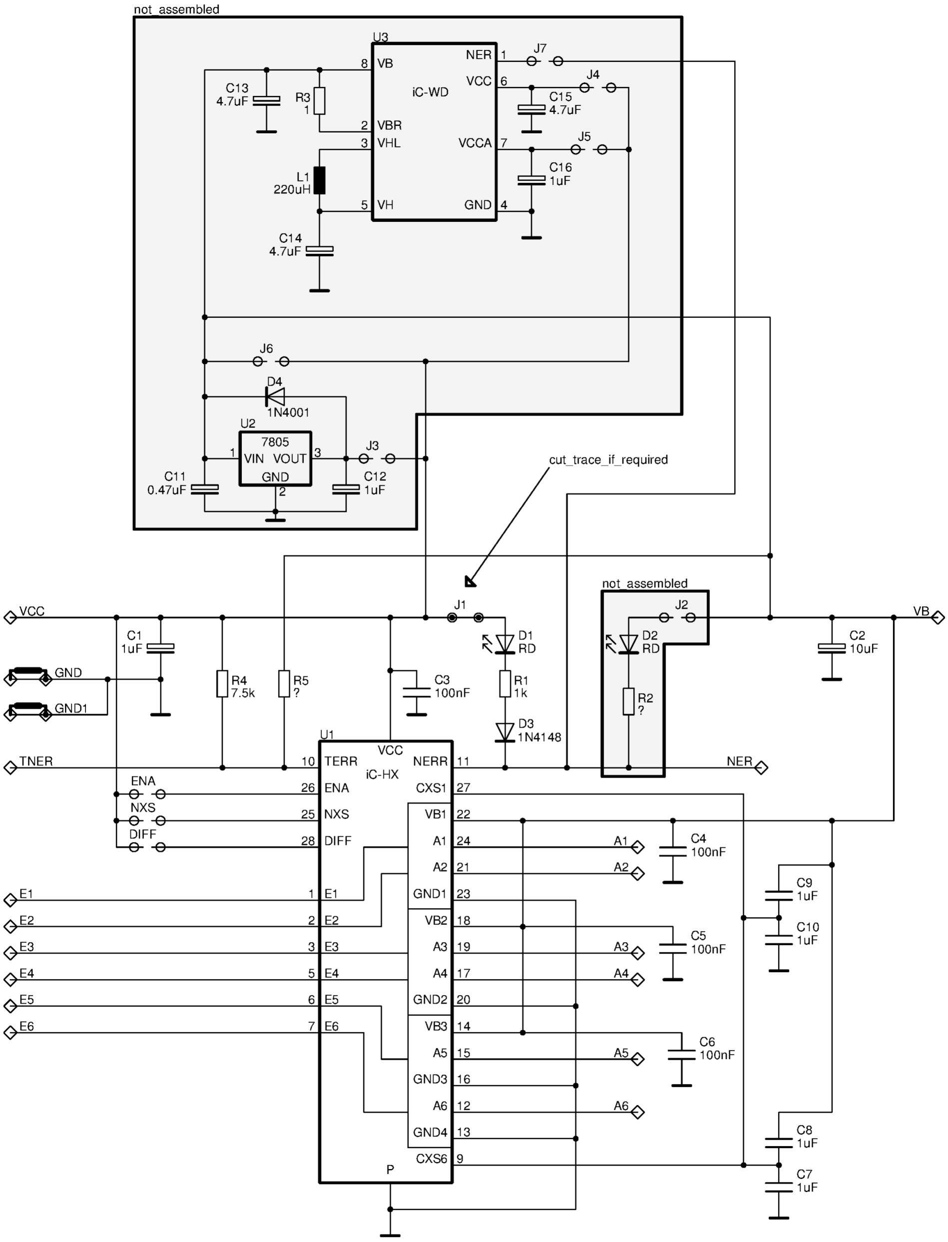


Figure 11: Circuit diagram of the demo board

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
B2	2016-07-28		Label ”preliminary” removed	1
		ELECTRICAL CHARACTERISTICS	Items 001, 007: Conditions for operation at VBx voltages below 7V introduced	4
		ELECTRICAL CHARACTERISTICS	Figure 1 introduced showing operating setup for VBx voltages below 7 V	6
		OPERATING CONDITIONS	Item I012: Parameter and condition added	6

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* Release Date format: *YYYY-MM-DD*

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Type	Package	Order Designation
iC-HX	QFN28 5 x 5 mm²	iC-HX QFN28
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