iC-LO
TRIANGULATION SENSOR

preliminary

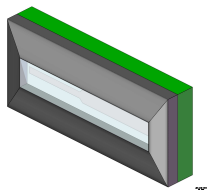
FEATURES

- Specially formed line image sensor comprising 129 elements
- High ambient light suppression of up to 100 kLux with filter glass
- Dynamic range of 100 dB
- 2 antivalent switching outputs
- Alarm message output
- High switching frequencies
- Low latency
- Power-down reset output
- Write protection for internal registers

APPLICATIONS

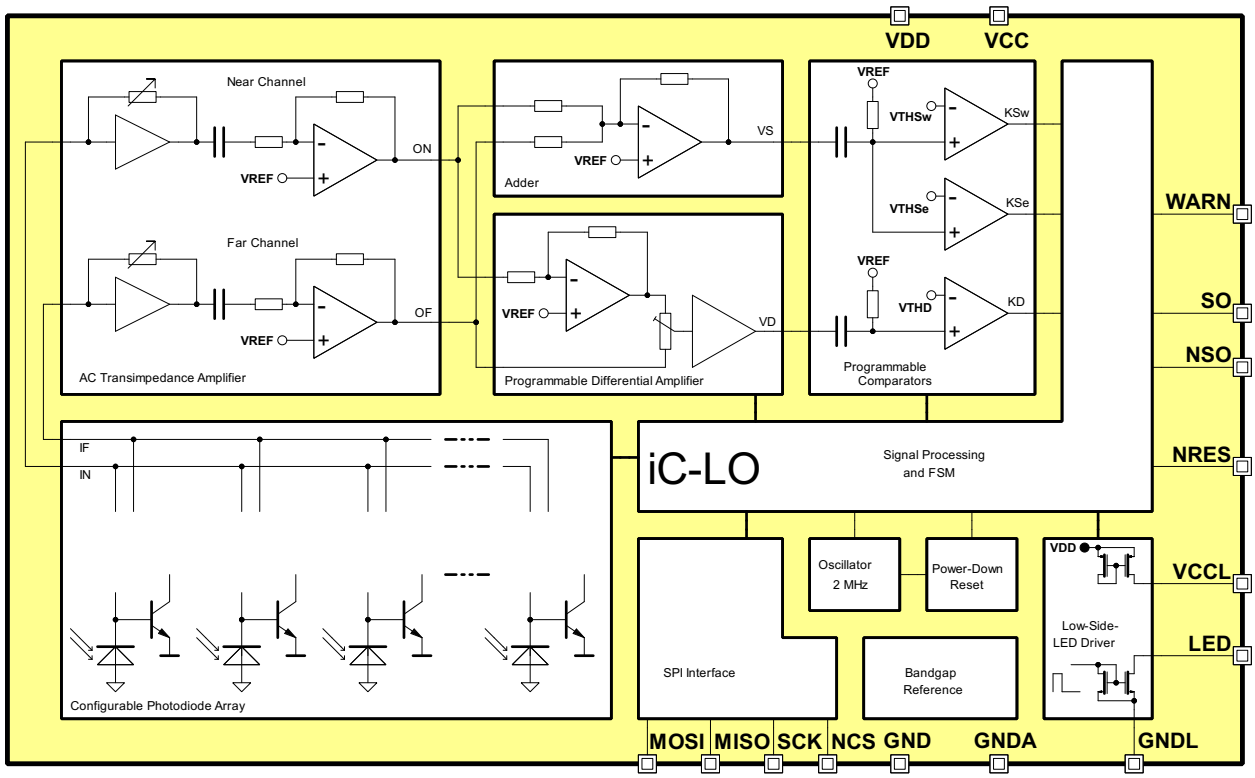
- Diffuse reflective photoelectric sensors

PACKAGES



optoBGA LO1C

BLOCK DIAGRAM



DESCRIPTION

iC-LO is suitable for the assembly of diffuse reflective photoelectric sensors based on the principle of triangulation. Besides iC-LO, all that is required to create such a setup is a transmitting LED, a low-cost microcontroller, and a driver device for the switching output.

The iC contains a photodiode array, consisting of one near diode, 127 middle diodes, and one far diode.

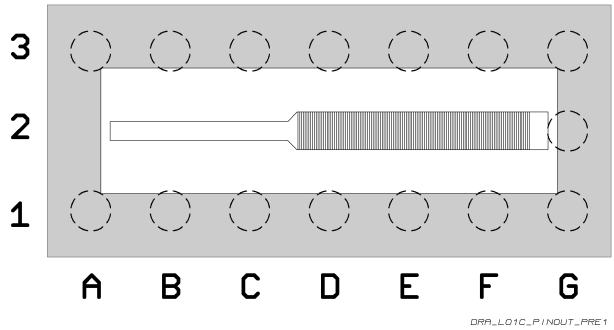
The diode photocurrents are segmented on two AC amplifiers (near and far channel). The AC amplifiers ensures a very good suppression of low-frequency interference. The sum and difference are calculated from the output voltages of the amplifiers; these are evaluated by comparators. From the comparator signals a programmable filter for the evaluation of multiple measurements generates the switching signal for the light sensor and also a warning on weak received light. The gain characteristic is dynamically adjusted to the intensity of the received light and becomes a logarithmic characteristic with very powerful input signals (reflective objects). This results in a very high dynamic range. The integrated low side driver can drive an LED directly or control an external driver by CMOS output.

iC-LO is configured using an SPI interface. The internal registers can be protected against overwriting.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION optoBGA LO1C



PIN FUNCTIONS

No.	Name	Function
A1	MOSI	Master Output Slave Input
A3	NSO	Antivalent Switching Output
B1	SCK	SPI Clock
B3	SO	Switching Output
C1	MISO	Master Input Slave Output
C3	WARN	Warning Output
D1	NCS	SPI Chip Select
D3	NRES	Power-Down Reset
E1	GNDA	Analogue Ground
E3	VDD	Digital Supply
F1	VCC	Analogue Supply
F3	GND	Digital Ground
G1	VCCL	LED Driver Supply
G2	LED	LED Driver Output
G3	GNDL	LED Driver Ground

Physical dimensions see optoBGA package specification LO1C.

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Supply Voltage at VCC, VDD		-0.3	6	V
G002	V()	Voltage at digital inputs MOSI, SCK, NCS		-0.3	VDD + 0.3	V
G003	I()	Current in WARN, NSO, SO, MISO, MOSI, SCK, NCS, NRES, GND		-40	40	mA
G004	I()	Current in VCC, GNDA		-50	50	mA
G005	I()	Current in VDD		-40	70	mA
G006	I()	Current in VCCL		-70	40	mA
G007	I()	Current in LED		-40	1600	mA
G008	I()	Current in GNDL		-1600	40	mA
G009	Tj	Chip-Temperature		-40	125	°C
G010	Ts	Storage Temperature Range	see package specification			
G011	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV

THERMAL DATA

Operating Conditions: VDDA = VDD = 5 V ±10%

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	see package specification	-40		85	°C

All voltages are referenced to Pin GNDA unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = VDD = 5 V±10 %, Tj = -40...85 °C, f_{OSC} = 2 MHz, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	V(VCC)	Permissible supply voltage analog		4.5	5	5.5	V
002	V(VDD)	Permissible supply voltage digital		4.5	5	5.5	V
003	I(VCC)	Supply Current in VCC	Iph() = 0		4		mA
004	I(VDD)	Supply Current in VDD	I(VCCL) = 0		0.8		mA
005	Vc()hi	Clamp Voltage hi at NCS, CLK, VZAP	Vc()hi = V() − V(VDD), I() = 1 mA	0.3		1.6	V
006	Vc()hi	Clamp Voltage hi at VCCL	Vc()hi = V() − V(VDD), I() = 1 mA	0.3		1.6	V
007	Vc()hi	Clamp Voltage hi at LED, GND	Vc()hi = V() − V(VDD), I() = 1 mA	0.3		1.2	V
008	Vc()hi	Clamp Voltage hi at NRES	Vc()hi = V() − V(VDD), I() = 1 mA	0.6		2.6	V
009	Vc()hi	Clamp Voltage hi at WARN, SO, NSO, MISO	Vc()hi = V() − V(VDD), I() = 1 mA	0.3		1.6	V
010	Vc()lo	Clamp Voltage lo at MOSI, SCK, MISO, NCS, GND, VDD, NRES, WARN, SO, NSO	I() = -1 mA	-1.2		-0.3	V
011	Vc()lo	Clamp Voltage lo at VCC, VCCL, LED, GNDL	I() = -1.3 mA	-1.2		-0.3	V
Fotodiodes (D0..D128) with cascode							
101	L()	Overall length of diode array			7		mm
102	A(D0)	Active area near-diode	3000 µm x (300...600) µm		0.927		mm^2
103	A()	Active area mid-diodes D1 to D127	29.35 µm x 600 µm		17610		$µm^2$
104	A(D128)	Active area far-diode	272.55 µm x 600 µm		163530		$µm^2$
105	S(λ)max	Efficiency	λ = 680 nm		0.38		A/W
106	λar	Spectral Application Range	S(λar) = 0.25 x S(λ)max	400		950	nm
107	I_{max}(D0)	Maximum photocurrent near-diode		8			mA
108	I_{max}()	Maximum photocurrent mid-diodes D1 to D127		750			µA
109	I_{max}(D128)	Maximum photocurrent far-diode		7.5			mA
AC Transimpedance Amplifier							
201	Iph()dc	DC Photocurrent				260	µA
202	Iph()ac	AC Photocurrent				12	mA
203	Iph()lin	Linear Transimpedance range	-3 dB corner of R_{ac}, Iph()lin = 0...Iph()ac; TIM = 0x0 TIM = 0x1 TIM = 0x2 TIM = 0x3		 10 71 1050 15650		 µA µA µA µA
204	R_{ac}	Transimpedance	linear range, Iph()ac < Iph()lin; TIM = 0x0 TIM = 0x1 TIM = 0x2 TIM = 0x3		 112.5 k 17.5 k 1350 101		 Ω Ω Ω Ω
206	deltaR$_{ac}$	Transimpedance change in logarithmic range	deltaR$_{ac}$ per decade Iph()ac		-19		dB
208	f_u	Lower Cut-off Frequency	linear range, Iph()ac < Iph()lin, -3 dB corner		25		kHz
209	f_o	Upper Cut-off Frequency	linear range, Iph()ac < Iph()lin, -3dB corner		200		kHz
Adder							
301	Av_{sum}	Gain		1.8	2	2.2	
302	f_o	Upper Cut-off Frequency	-3 dB corner		230		kHz

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = VDD = 5 V±10 %, Tj = -40...85 °C, f_{OSC} = 2 MHz, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Programmable Differential Amplifier (x = F, N)							
401	Avn	Near-Channel Gain	POTx = 0x00 POTx = 0xFF		8.5 26		
402	Avf	Far-Channel Gain	POTx = 0x00 POTx = 0xFF		26 8.5		
403	f_o	Upper Cut-off Frequency	-3 dB corner		150		kHz
Programmable Comparator							
501	V_{off}	Offset	save by design	-2		2	mV
502	V_{hys}(KD)	Hysteresis KD	DISHYS = 0; HYSD = 0x0 HYSD = 0xF		 2.65 63.6		 mV mV
503	V_{hys}(KS)	Hysteresis KSw, KSe	DISHYS = 0; HYSS = 0x0 HYSS = 0x3		 2 8		 mV mV
504	V_{THSw}	Threshold Voltage for *warning*	THSw = 0x00 THSw = 0x1F		2.8 89.6		mV mV
505	V_{THSe}	Threshold Voltage for *error*	THSe = 0x00 THSe = 0x1F		2.8 89.6		mV mV
506	f_u	Cut-off Frequency High-pass Input	-3 dB corner		12		kHz
Oscillator							
701	f_{OSC}	Oscillator Frequency	OSC = 0x8		2		MHz
SPI Interface NCS, SCK, MOSI, MISO							
I01	Vt()hi	Threshold Voltage hi at NCS, SCK, MOSI				2	V
I02	Vt()lo	Threshold Voltage lo at NCS, SCK, MOSI		0.8			V
I03	Vt()hys	Hysteresis at NCS, SCK, MOSI		50		450	mV
I04	Ipu(NCS)	Pull-Up Current in NCS	V(NCS) = 0...VDD − 1 V	-70	-30	-5	µA
I05	Ipd()	Pull-Down Current in SCK and MOSI	V(SCK) = 1 V...VDD	3	30	80	µA
I06	Vs(MISO)hi	Saturation Voltage hi at MISO	Vs(MISO)hi = VDD − V(MISO); I(MISO) = -1.6 mA			350	mV
I07	Vs(MISO)lo	Saturation Voltage lo at MISO	I(MISO) = 1.6 mA			300	mV
I08	Isc()hi	Short-Circuit Current hi in MISO		-35		-1.7	mA
I09	Isc()lo	Short-Circuit Current lo in MISO		1.7		35	mA
I10	f(SCK)	Clock Frequency at SCK				1	MHz

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = VDD = 5 V±10 %, Tj = -40. . . 85 °C, f_{OSC} = 2 MHz, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Low-Side LED driver VCCL, GNDL, LED							
L01	I(VCCL)	Short-Circuit Current from VCCL	V(VCCL) = V(GNDA)	-57		-39	mA
L02	Vs()hi	Saturation Voltage hi at VCCL	Vs(VCCL)hi = V(VDD) – V(VCCL); I(VCCL) = -35 mA			0.85	V
L03	I(LED)nom	Nominal Current in LED	LCC = 0x00 LCC = 0x07 LCC = 0x08 LCC = 0x0F LCC = 0x10 LCC = 0x17 LCC = 0x18 LCC = 0x1F	86 180 155 320 295 636 593 1150			mA mA mA mA mA mA mA mA
L04	C	Backup Capacitor for LED driver	between VCCL and GNDL	10			µF
L05	Vs(LED)lo	Saturation Voltage lo at LED	Vs(LED)lo = V(LED) – V(GNDL); LCO = 0x1 (LED-driver mode), I(LED) = I(LED)nom			2	V
L06	Vs(LED)hi	Saturation Voltage hi at LED	Vs(LED)hi = VDD – V(LED); LCO = 0x0 (CMOS-Output), I(LED) = -1.6 mA			350	mV
L07	Vs(LED)lo	Saturation Voltage lo at LED	LCO = 0x0 (CMOS-Output), I(LED) = 1.6 mA			300	mV
L08	Isc()hi	Short-Circuit Current hi at LED	LCO = 0x0 (CMOS-Output)	-35		-1.7	mA
L09	Isc()lo	Short-Circuit Current lo at LED	LCO = 0x0 (CMOS-Output)	1.7		35	mA
L10	f_{PER}	Pulse Frequency	PER = 0x1 PER = 0x3		13.9 5		kHz kHz
L11	t_{PW}	Pulse Width	PW = 0x0 PW = 0xF		2 9.5		µs µs
L12	I(LED)err /I(LED)typ	Current monitoring threshold	I(LED)typ = I(LED)@V(LED)=2V LCO = 0x1 LCC = 0x00 . . . 0x0F LCC = 0x10 . . . 0x1F	 10 5	 40 30	 70 50	 % %
Digital Outputs SO, NSO, WARN, NRES							
O01	Vs()hi	Saturation Voltage hi at SO, NSO, WARN, NRES	Vs()hi = VDD – V(); I() = -1.6 mA			350	mV
O02	Vs()lo	Saturation Voltage lo at SO, NSO, WARN, NRES	I() = 1.6 mA			300	mV
O03	Isc()hi	Short circuit current hi at SO, NSO, WARN, NRES		-35		-1.7	mA
O04	Isc()lo	Short circuit current lo at SO, NSO, WARN, NRES		1.7		35	mA
Power-Down Reset NRES							
R01	Vt(VCC)hi	Turn-on Threshold VCC				3.9	V
R02	Vt(VCC)lo	Turn-off Threshold VCC		3.0			V
R03	Hys(VCC)	Hysteresis VCC		150		400	mV
R04	td	Delay at NRES	VCC switched on	20		40	ms

OPERATING REQUIREMENTS: SPI Interface

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	t_{C1}	Permissible Cycle Time	see Elec. Char. No.: I10	1/f(SCK)		
I002	t_{W1}	Wait Time: between NCS lo → hi and NCS hi → lo	without measurement with measurement	2 100		µs µs
I003	t_{S1}	Setup Time: NCS lo before SCK lo → hi		50		ns
I004	t_{P1}	Propagation Delay: MISO stable after NCS hi → lo			100	ns
I005	t_{P2}	Propagation Delay: MISO high impedance after NCS lo → hi			100	ns
I006	t_{H1}	Hold Time: NCS lo after SCK lo → hi		100		ns
I007	t_{S2}	Setup Time: MOSI stable before SCK lo → hi		100		ns
I008	t_{H2}	Hold Time: MOSI stable after SCK lo → hi		100		ns
I009	t_{P3}	Propagation Delay: MISO stable after MOSI change	mode: repeating MOSI on MISO		100	ns
I010	t_{P4}	Propagation Delay: MISO stable after SCK hi → lo	mode: sending data on MISO		125	ns

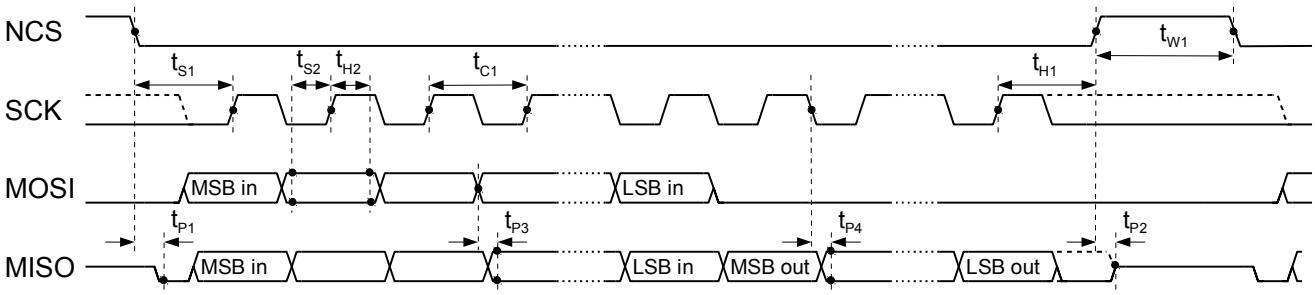


Figure 1: Timing SPI Interface

CONFIGURATION PARAMETERS

Thresholds

TIM: Transimpedance (page 13)
THSW: Warning Threshold *weak received light* (page 15)
THSE: Error Threshold *weak received light* (page 15)
HYSD: Comparator hysteresis *difference* (page 14)
HYSS: Comparator hysteresis *sum* (page 14)
DISHYS: Disable Comparator hysteresis (page 14)

Parameter set OBF (object far)

SPF: Diode segmentation (page 14)
POTF: Digital potentiometer (page 14)

Parameter set OBN = (objekt near)

SPN: Diode segmentation (page 14)
POTN: Digital potentiometer (page 14)

LED Driver

LCO: LED driver mode (page 23)
LCC: LED pulse current (S. 23)
PW: Pulse width (page 12)
PER: Pulse frequency (page 12)

Digital Filter

FIN: Number of averaged measurements (page 15)
FIM: Number of complementary measurements (page 15)
SKO: Sample point in time (page 16)

Internernal Oscillator

OSC: Frequency trimming (page 17)

Output Configuration

SOCNO: Output mode (page 16)
SOEN: Output enable (page 16)
TAR: Turn-on delay (page 16)
TAF: Minimum on-time (page 17)

Opcode/Status Register

OP: Operating modes (page 18)
SOI: Last output (page 18)
WARNI: Last output status / warning (page 18)
TII: Last transimpedance value (page 18)
NKDF: Last comparator result (page 18)
KSW: Last warning threshold result (page 18)
KSE: Last error threshold result (page 18)
LEDOK: LED status (page 18)

Device Designator

REV: Revision (page 21)

REGISTER MAP

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
THRESHOLDS								
0x00		SPF(6:0)						
0x01	POTF(7:0)							
0x02		SPN(6:0)						
0x03	POTN(7:0)							
0x04	TIM(2:0)			DISHYS	HYSD(3:0)			
0x05	HYSS(1:0)			THSW(4:0)				
0x06				THSE(4:0)				
LED DRIVER								
0x07			LCO	LCC(4:0)				
0x08			PER(1:0)		PW(3:0)			
DIGITAL FILTERING								
0x09	FIM(3:0)				FIN(3:0)			
0x0A	SKO(3:0)				TAR(1:0)		TAF(1:0)	
OSCILLATOR								
0x0B				0	OSC(3:0)			
OUTPUT CONFIGURATION								
0x0C				SOEN				SOCNO
0x0D								
INSTRUCTION REGISTER								
0x0E	OP(7:0)							
STATUS REGISTER (read only)								
0x0F	SOI	WARNI	TII(1:0)		NKDF	KSW	KSE	LEDOK
DEVICE DESIGNATOR (ROM)								
0x10	0x4C ≙ 'L'							
0x11	0x4F ≙ 'O'							
0x12	REV(7:0)							
0x13	0x69 ≙ 'i'							
0x14	0x43 ≙ 'C'							

Table 5: Register layout

MEASURING SEQUENCE

In order to determine whether the distance between an object and the sensor falls below a defined value, iC-LO initiates a light pulse that is then diffuse reflected and pictured onto the photodiode array. The spot of light diffuse reflected by the object moves along the diode array depending on the distance object to sensor.

After the light pulse has been transmitted, at a defined point in time the signal from the photodiode array is evaluated and decided whether the distance between the object and sensor has fallen below a defined value or not.

LED DRIVER

iC-LO can drive a transmitting LED directly or trigger an external driver using the CMOS level output. A lowside driver is integrated to drive the LED and can supply diode currents of up to approx. 1 A with an external back-up capacitor.

The type of output at pin LED (low-side driver or CMOS output) is set by parameter LCO.

LCO	Addr. 0x07; bit 5	RW
Code	Description	
0x0	CMOS output at pin LED	
0x1	Low-side driver at pin LED	

Table 6: Configuration LED Output Type

The parameter LCC configures the LED current.

LCC	Addr. 0x07; bit 4:0	RW
Code	Description	
0x0	112 mA	
0x1	126 mA	
...		
0x7	210 mA	
0x8	193 mA	
0x9	221 mA	
...		
0xF	389 mA	
0x10	368 mA	
0x11	423 mA	
...		
0x17	753 mA	
0x18	696 mA	
0x19	796 mA	
...		
0x1F	1396 mA	

Table 7: Current in LED (low-side driver)

LED error monitoring

In order to monitor the system function it is possible to read out status bit LEDOK (address 0x08, bit 0 R) which correspond to high impedance of the transmitting LED.

LEDOK	Addr. 0x08; bit 0	R
Code	Description	
0x0	No LED current monitoring, on CMOS output operation	
0x0	LED current not ok, on low-side driver operation	
0x1	LED current ok, on low-side driver operation	

Table 8: LED Current Ok

This monitoring is only valid in low-side driver operation pin LED. When using the integrated LED driver the current flowing out of the iC-LO is monitored. So an eventual damage of the LED can be detected while in use. For details see table 28 (status register).

LED frequency and pulse width

The frequency of the light pulses in multiple measurement mode (see table 18) and the duration of a light pulse is set by parameters PER and PW.

PER	Addr. 0x08; bit 5:4	RW
Code	Description	
0x0	reserved	
0x1	13.9 kHz	
0x2	10.4 kHz	
0x3	5 kHz	

Table 9: Pulse Frequency

PW	Addr. 0x08; bit 3:0	RW
Code	Description	
0x0	2 µs	
0x1	2.5 µs	
...		
0xF	9.5 µs	

Table 10: Pulse Width

The effect of the individual parameters is shown in figure 2.

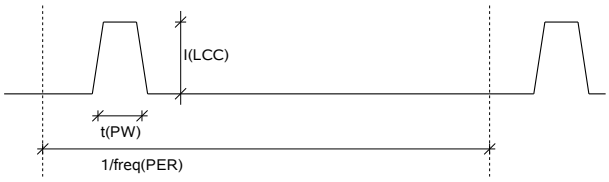


Figure 2: Light pulse

NEAR/FAR CHANNEL PARTITION AND AMPLIFICATION

The typical spectral sensitivity is shown in figure 3.

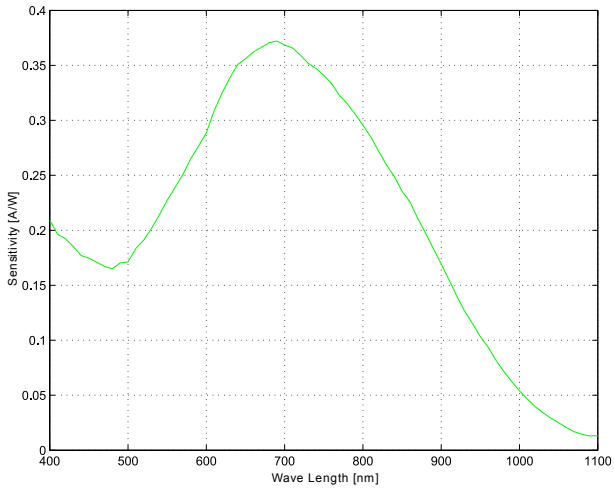


Figure 3: Spectral sensitivity of the photodiode

The diode array is partitioned into two channels (one near and one far channel). The channelwise received photocurrents are added, converted to voltages and amplified. Afterwards a differential comparator decides whether the signal of the near or far channel is greater. A greater signal in the near channel indicates an object within the defined near range and the switching output is activated.

Current/voltage conversion
The transimpedance of the current/voltage conversion can be configured according to the expected photocurrents. In the static transimpedance setting modes this configuration is not altered by iC-LO. If the transimpedance amplifier exceeds a high set point it continues with a logarithmic characteristic. In the logarithmic range the parametrized switching point can shift if the digital potentiometer is used (table 13). iC-LO thus has an automatic mode which selects the transimpedance depending on the received sum light current. The transimpedance set in the automatic modes represents the start value in operating mode **STARTUP/RESET**. Two comparators monitor the sum light current and switch up or down one transimpedance step when the fixed thresholds are either overshot or undershot. If the transimpedance setting is to be changed during operation, after programming the device must be reset (operating mode **STARTUP/RESET**).

TIM	Addr. 0x04; bit 7:5		RW
Code	Mode	R Transimpedance	R_{ac} Transimpedance
0x0	static	50 kΩ	112.5 kΩ
0x1	static	7765 Ω	17.5 kΩ
0x2	static	600 Ω	1350 Ω
0x3	static	45 Ω	101 Ω
0x4	auto	50 kΩ	112.5 kΩ
0x5	auto	7765 Ω	17.5 kΩ
0x6	auto	600 Ω	1350 Ω
0x7	auto	45 Ω	101 Ω

Table 11: Transimpedance Mode

Channel partitioning
The block diagram on page 1 depicts the signal chain. There are two ways in which the differential comparator input signals and thus the necessary sensing distance can be configured in iC-LO. The two *setting parameters* are implemented in two sets of parameters twice. One of these sets of parameters is active when the switching state is *off* - i.e. the object was in the far range during the last measurement (parameter set OBF). The other is used in switching state *on* (parameter set OBN). Depending on the difference of the switching points of the two sets of parameters, a freely selectable switching hysteresis can be set.

Setting parameters for the near/far channel Diodes are partitioned to the near and far channels using parameters SPF and SPN. SPF belongs to parameter set OBF and SPN to parameter set OBN. Diodes from 0 (near diode) to the set value are assigned to the near

channel, with the remaining diodes up to diode 128 (far diode) assigned to the far channel.

SPF	Addr. 0x00; bit 6:0	RW
SPN	Addr. 0x02; bit 6:0	RW
Code	Description	
0x0	0	
0x1	1	
...		
0x7F	127	

Table 12: Diode Assignment

If the parameters SPF and SPN are configured that SPF < SPN then the numeric gap between both numbers representes the hysteresis of the sensor (indicated blue for hysteresis in the evaluation software).

Configuring SPF > SPN is not recommended due to a negative hysteresis.

Setting parameter gain ratio In the subtractor the gain ratio between the near and far channel can be adjusted using a digital potentiometer. This achieves a higher measurement resolution than only partitioning the diode array. Parameters POTF (parameter set OBF) and POTN (parameter set OBN) configure the potentiometer.

POTF	Addr. 0x01; bit 7:0	RW
POTN	Addr. 0x03; bit 7:0	RW
Code	Gain Ratio Near/Far Channel	
0x00	0.327	
0x01	0.330	
...		
0x7E	0.988	
0x7F	0.996	
0x80	1.004	
0x81	1.012	
...		
0xFE	3.026	
0xFF	3.059	

Table 13: Digital Potentiometer

A gain ratio of > 1 shifts the switching point towards shorter distances and vice versa.

Comparator hysteresis
To stabilize the comparator outputs the system hysteresis of the three comparators KD(comparator difference signal), KSw(comparator warning threshold), and KSe(comparator error threshold) can be configured. The system hysteresis is switched with the sampled and filtered comparator output signals KDF, KSwF, and KSeF. Parameter HYSD is used to set the hysteresis of differential comparator KD and parameter HYSS that of sum comparators KSw and KSe.

HYSD	Addr. 0x04; bit 3:0	RW
Code	Hysteresis KD	
0x0	2.65 mV	
0x1	5.30 mV	
0x2	7.95 mV	
0x3	10.6 mV	
0x4	13.25 mV	
0x5	15.90 mV	
0x6	18.55 mV	
0x7	21.20 mV	
0x8	26.50 mV	
..		
0xF	63.60 mV	

Table 14: Comparator Hysteresis

HYSS	Addr. 0x05; bit 7:6	RW
Code	Hysteresis KSw, KSe	
0x0	2 mV	
0x1	4 mV	
0x2	6 mV	
0x3	8 mV	

Table 15: Comparator Hysteresis

If the parameters THSE or THSW are configured that the voltage levels of THSE or THSW are smaller than the voltage level of HYSS/2 then the compared voltage can not fall below 0 V and then the related comparator output can not turn to 0 any more (indicated yellow for warning this parameter conflict of HYSS and THSE and THSW in the evaluation software).
Configuring the voltage levels of THSE < HYSS/2 is not recommended.
Configuring the voltage levels of THSW < HYSS/2 is not recommended.

The hysteresis can be deactivated by DISHYS.

DISHYS	Addr. 0x04; bit 4	RW
Code	Description	
0x0	Hysteresis set by HYS	
0x1	Hysteresis deactivated	

Table 16: Hysteresis Deactivation

RECEIVED SIGNAL MONITORING

Two sum comparators have been integrated to monitor the system and evaluate the intensity of the received light pulse. A switching threshold can be configured separately for each of the comparators. The warning threshold is configured by using VTHSW and an error threshold by using VTHSE. If the received light pulse undershoots the relevant set threshold, the corresponding comparator output (KSw and KSe, see block diagram) is set to low. It makes sense to set the warning threshold higher than the error threshold. The warning threshold could indicate that the sensor is contaminated. If the intensity of the received light pulse undershoots the error threshold, the switching output is deactivated as a decision cannot be safely made (see table 21).

THSW	Addr. 0x05; bit 4:0	RW
THSE	Addr. 0x06; bit 4:0	RW
Code	Description	
0x00	VTHSx = 2.8 mV	
0x01	VTHSx = 5.6 mV	
..		
0x1F	VTHSx = 89.6 mV	

Table 17: Thresholds Sum Comparators, x = W, E

SAMPLE POINT, DIGITAL SIGNAL CONDITIONING, AND OUTPUT CONFIGURATION

The signal conditioning chain between the comparator outputs and the switching outputs is shown in figure 4.

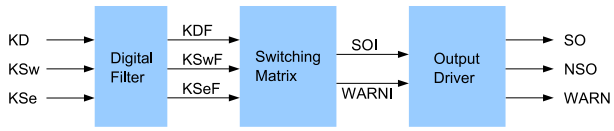


Figure 4: Digital processing and signal output

Digital filter

To improve noise immunity a measurement cycle (see figure 5), which results in an update of the switching and warning outputs, can consist of several individual measurements (see figure 6). The number of individual measurements in a measurement cycle is set using FIN. After each individual measurement the last individual measurements set through FIN are collated to form a measurement cycle and evaluated.

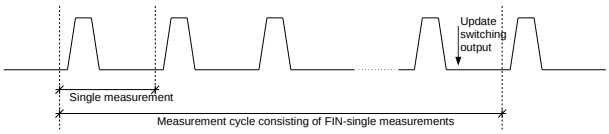


Figure 5: Measurement cycle

In doing so, each comparator output (KD, KSw, and KSe) is separately filtered. There must then be a minimum number of individual measurements complementary to the current filtered comparator output (KDF, KSwF, and KSeF) so that the corresponding filtered comparator output changes its state. This number is configured using FIM.

FIN	Addr. 0x09; bit 3:0	RW
Code	Description	
0x0	1	
0x1	2	
0x2	3	
...		
0xF	16	

Table 18: Number of Measurements Per Cycle

FIM	Addr. 0x09; bit 7:4	RW
Code	Description	
0x0	1	
0x1	2	
0x2	3	
...		
0xF	16	

Table 19: Number of Measurements Complementary to Current Comparator State

Sample point in time

The point in time at which the outputs of the three comparators are sampled during an individual measurement (t_{sample}, see figure 6) can be shifted using parameter SKO. This shift is always referenced to the rising edge of the light pulse generated in the LED driver.

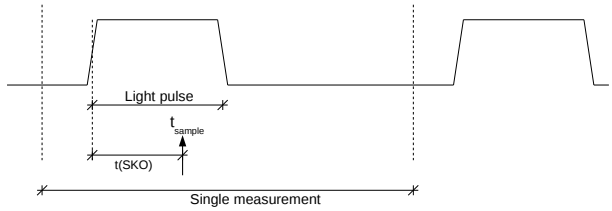


Figure 6: Single measurement

SKO	Addr. 0x0A; bit 7:4	RW
Code	Description	
0x0	1.5 µs	
0x1	2 µs	
...		
0xF	9 µs	

Table 20: Sample Timing

Switching matrix
Internal switching state SOI and warning state WARNI are determined from the filtered comparator outputs according to the following truth table (table 21):

KDF	KSwF	KSeF	SOI	WARNI	System state
0	1	1	0	0	Object detected far, enough light
0	0	1	0	0	Object detected far, low light
0	0	0	0	0	Object detection impossible, not enough light
0	1	0	0	0	Invalid configuration (see page 15)
1	1	1	1	0	Object detected near, enough light
1	0	1	1	1	Object detected near, low light
1	0	0	0	0	Object detection impossible, not enough light
1	1	0	0	0	Invalid configuration (see page 15)

Table 21: Switching Matrix

Output drivers
The polarity of the switching output can be selected due to the connected switch using SOCNO. Output WARN is equivalent to the internal WARNI signal.

SOCNO	Addr. 0x0C; bit 0	RW
Code	Description	
0	Configures the output SO as *normally open* and NSO as *normally closed* (SO = SOI)	
1	Configures the output SO as *normally closed* and NSO as *normally open* (SO = $\overline{SOI}$)	

Table 22: Output Configuration

If the switching outputs SO and NSO are not required, they can be disabled by SOEN. A zero is then output at both outputs.

SOEN	Addr. 0x0C; bit 4	RW
Code	Description	
0	SO and NSO disabled	
1	SO and NSO enabled	

Table 23: Output Activation

Furthermore, in mode **PERIODIC_MEASURE** (table 27) a rise and fall delay can be configured for the warning and switching outputs (see figure 7 by way of example).

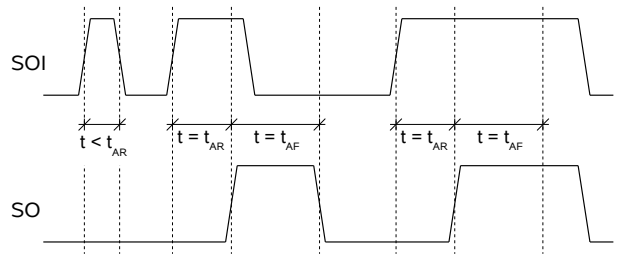


Figure 7: Rise and fall delay

Rise delay t_{AR} suppresses peaks that are shorter than t_{AR} (first SOI peak in figure 7). If SOI is active for longer than t_{AR}, switching output SO is activated. If SOI then drops to 0, SO only switches back when fall delay time t_{AF} has elapsed (second SOI peak in figure 7). If SOI remains at 1 after the fall delay time has elapsed, SO trails the falling edge at SOI directly (third SOI peak in figure 7). The fall delay time is thus equivalent to a minimum pulse duration at the outputs. Warning output WARN can only be switched on at the same time as the switching output and is reset as soon as sufficient received light is detected.

The delay times are configured using parameters TAR and TAF.

TAR	Addr. 0x0A; bit 3:2	RW
Code	Description	
0x0	0 ms	
0x1	5 ms	
0x2	20 ms	
0x3	50 ms	

Table 24: Rise Delay

TAF	Addr. 0x0A; bit 1:0	RW
Code	Description	
0x0	0 ms	
0x1	5 ms	
0x2	20 ms	
0x3	50 ms	

Table 25: Fall Delay

SYSTEM CLOCK

The frequency of the internal oscillator must be trimmed to ensure correct timing. For this purpose the system clock can be output at pin WARN using the command **OSC_OUT_ON** (table 27).

OSC	Addr. 0x0B; bit 3:0	RW
Code	Description	
0x0	-20%	
0x1	-17.5%	
...		
0x8	0%	
...		
0xF	17.5%	

Table 26: System Clock Setting

STARTUP BEHAVIOR, OPERATING MODES, AND STATUS REGISTER

Startup behavior and operating modes

After iC-LO has started up all internal registers and counters are reset to 0. Switching outputs SO and NSO are thus at 0. The warning output is activated. The device waits for further commands (operating mode **STARTUP/RESET**).

Implemented commands

By writing to address 0x0E commands can be executed and the device operating mode changed.

OP	Addr. 0x0E; bit 7:0	W
Code	Command	Description
0x00	STARTUP/RESET	Operating mode after power-down (reset of digital filters)
0x02	SINGLE_MEASURE	Single measurement cycle started with rising NCS edge
0x03	PERIODIC_MEASURE	Periodic measurement cycles, paused with NCS = '0' (normal operation mode)
0x04	OSC_OUT_ON	Output 1 MHz clock at pin WARN
0x06	REG_PROT_ON	Disable write access to registers 0x0-0xD
0x07	REG_PROT_OFF	Enable write access to registers 0x0-0xD
0x08	TST_SO_ON	Output active
0x09	TST_SO_OFF	Output inactive
0x0A	TST_WARN_ON	Set warning output to '1'
0x0B	TST_WARN_OFF	Set warning output to '0'
...0xFF	reserved for device test	

Table 27: Implemented Commands

With command **STARTUP/RESET** internal state machines, counters, and the status register are reset. The device waits for further commands.

Command **OSC_OUT_ON** enables the output of a 1 MHz clock (based on the system clock) through pin WARN.

With command **REG_PROT_ON** the internal configuration register addresses 0x00 . . . 0x0D are protected against overwriting. This write protection can be cancelled by command **REG_PROT_OFF**.

Command **TST_SO_ON** sets switching output SO to active and NSO to inactive regardless of the internal SOI state (observe SOCNO and SOEN programming).

Command **TST_SO_OFF** sets switching output SO to inactive and NSO to active regardless of the internal SOI state (observe SOCNO and SOEN programming).

Command **TST_WARN_ON** sets warning output WARN to 1 regardless of the internal WARNI state.

Command **TST_WARN_OFF** sets warning output WARN to 0 regardless of the internal WARNI state.

Status register

The status register is read out on a read access to register 0x0F. The switching state, warning, and transimpedance mode from the last measurement cycle are stored here, plus the last comparator results of the differential- (NKDF), warning- (KSW) and errorcomparator (KSE). The result of the differentialcomparator is stored invertedly. Additionally the result of the LED driver current monitoring LEDOK is stored. Its vaule is '1' when the integrated LED driver is used and the LED is functioning properly. Otherwise its value is '0'. The switching state (SOI) stored in the register is independent of SOCNO (see page 16). Coding of TII is equivalent to that of TIM(1:0) (table 11).

STATUS	Addr. 0x0F; bit 7:0	R
Bit	Name	Description
7	SOI	Output from last measurement cycle
6	WARNI	Warning from last measurement cycle
5:4	TII	Transimpedance of last measurement
3	NKDF	Last comparator result
2	KSW	Last warning threshold result
1	KSE	Last error threshold result
0	LEDOK	LED current status

Table 28: Status Register 0x0F

SPI INTERFACE

General description

SPI name	pin name	description
NCS	NCS	not chip select
SCLK	SCK	clock
MOSI	MOSI	master out slave in
MISO	MISO	master in slave out

Table 29: SPI Connector Pin List

During SPI communication (NCS low) an ongoing measurement sequence in iC-LO is halted (LED off, switching output off).

OPCODE summary

SPI OPCODES	
Opcode	Description
0xB0	not implemented
0xA6	not implemented
0xF5	not implemented
0x97	not implemented
0xD2	not implemented
0x8A	Read REGISTER (cont.)
0xCF	Write REGISTER (cont.)
0xAD	REGISTER status/data
0x9C	Read STATUS
0xD9	Write INSTRUCTION

Table 30: OPCODE Table

iC-Haus SPI data transmission

SPI modes 0 and 3 are supported, i.e. an idle polarity of SCLK 0 or 1 and acceptance of data with a rising edge of SCLK.

The idle level (NCS high) of the MISO line is tristate. The slave passes MOSI to MISO on a falling edge at NCS.

Data is sent bytewise with the MSB first. Each data transmission begins with the master sending an opcode. To be compatible to Microwire™, all opcodes start with a 1.

The following describes the typical sequence of an SPI data transmission, taking the command **Read REGISTER (cont.)** as an example (see figure 8):

1. The master initializes a transmission with a falling edge at NCS.
2. The slave passes the level on from MOSI to MISO.
3. The master transmits the **Read REGISTER (cont.)** opcode and address ADR via MOSI; the slave immediately outputs OPCODE and ADR via MISO.
4. The slave transmits the addressed data.
5. The master quits the command with a rising edge at NCS.
6. The slave switches its MISO output to tristate.

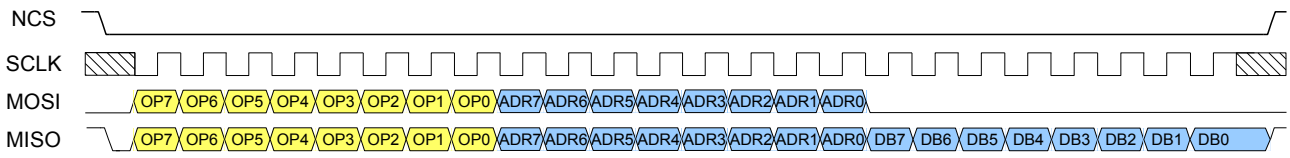


Figure 8: SPI transmission, using opcode Read REGISTER (cont.) as an example

Description of the SPI-Opcodes

REGISTER status/data

The **REGISTER status/data** command can be used to request the status of the last register communication and/or the last data transmission. The STATUS byte contains the information summarized in table 31.

STATUS		
Bit	Name	Description of the status report
7	ERROR	Opcode not implemented.
6..4	-	Reserved
3	DISMISS	Address refused
2	FAIL	Data request has failed
1	BUSY	Slave is busy with a request
0	VALID	DATA is valid
Note	Display logic: 1 = true, 0 = false	

Table 31: Communication Status Byte

All status bits are updated with each register access. The exception to the rule is the ERROR bit; this bit indicates whether an error occurred during the last SPI-communication with the slave.

The master transmits the **REGISTER status/data** opcode. The slave immediately passes the opcode on to MISO. The slave then transmits the STATUS byte and a DATA byte. The DATA-Byte is undefined in the actual configuration.

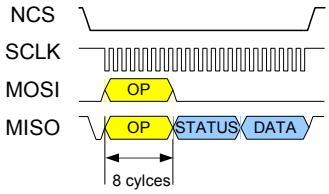


Figure 9: REGISTER status/data

Read REGISTER (cont.)
Reading data from internal registers the slave does not need any processing time. These registers can be read out in continous mode.

The master transmits the **Read REGISTER (cont.)** opcode. In the second byte the start address ADR is transmitted. The slave immediately outputs the opcode, address and then transmits the DATA1 data. The internal address counter is incremented following each data packet.

If an error occurs during register readout in continuous mode (e.g. the address is invalid or the requested data is not yet valid on data byte clockout), the internal address counter is no longer incremented and the error bit FAIL is set in the communication status register (see page 20).

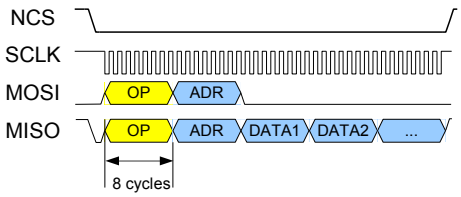


Figure 10: Read REGISTER (cont.)

Write REGISTER (cont.)

Writing data into internal registers the slave does not need any processing time. These registers can be written in continous mode.

The master transmits the **Write REGISTER (cont.)** opcode. In the second byte start address ADR is transmitted, followed by the DATA1-DATAn data packets to be written. The slave immediately outputs the opcode, address and data at MISO. The slave increments its internal address counter following each data packet.

If an error occurs during write to register in continuous mode (e.g. the address is invalid or the data write process of the last address was not finished), the internal address counter is no longer incremented and the error bit FAIL is set in the communication status register (see page 20).

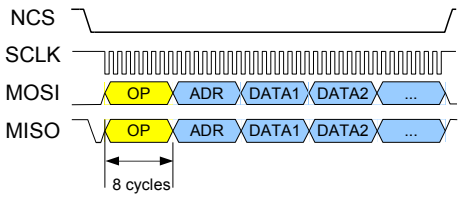


Figure 11: Write REGISTER (cont.)

Read STATUS

The command **Read STATUS** is designed to enable a fast readout of the internal, slave-specific status registers of a slave (STAT1-STATn). The opcode sets the address in the slave to the lowest STAT address. The internal address counter is incremented following each STAT byte. This command largely corresponds to the Read REGISTER (cont.) command, with the difference that here the addressing sequence is missing and the master does not need to know the slave's exact STAT address.

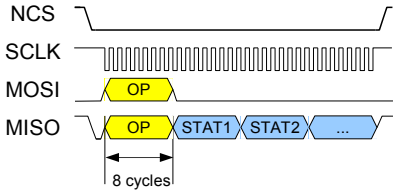


Figure 12: Read STATUS

Write INSTRUCTION

The command **Write INSTRUCTION** is designed to enable a fast setting of the internal, slave-specific command registers. The opcode sets the address in the slave to the lowest command register address. The instruction data bytes (INST1-INSTn) are send directly after the OPCODE byte. This command largely corresponds to the **Write REGISTER (cont.)** command, with the difference that here the addressing sequence is missing and the master does not need to know the slave's exact INST address.

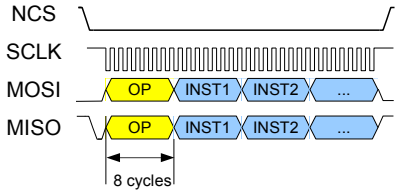


Figure 13: Write INSTRUCTION

POWER DOWN RESET

The internal power-down reset (low active) is output through NRES. The enable (rising edge) is delayed (see R04).

CONFIGURATION NOTES

- Parameter SKO should be programmed to 0x5 so that it is adjusted to suit the signal conditioning chain in iC-LO (see table 20).
- The light pulse width programmed using parameter PW (see table 10) should be at least 0.5 µs longer than SKO (see table 20).
- External laser/LED driver latency needs to be considered with the sampling time of iC-LO (parameter SKO see table 20).
- Operating mode **SINGLE_MEASURE** only functions when FIN = FIM = 0x0 (see table 18/19).

CHIP REVISION

The parameter REV in the iC-LO ROM provides the chip revision.

REV	Addr. 0x12; bit 7:0	R
Code	Chip revision	
0x0	iC-LO 0	
0x1	iC-LO 1	
0x2	iC-LO ZA	
0x3	iC-LO ZB	
0x4	iC-LO ZA1	
0x5	iC-LO Y	
0x6	reserved	
...		
0xFF	reserved	

Table 32: Chip Revision

APPLICATION NOTES

The diagram shows a possible IO-Link compatible system with iC-GF acting as a switch and reverse polarity protection for supply voltages of between 9 and 30 V.

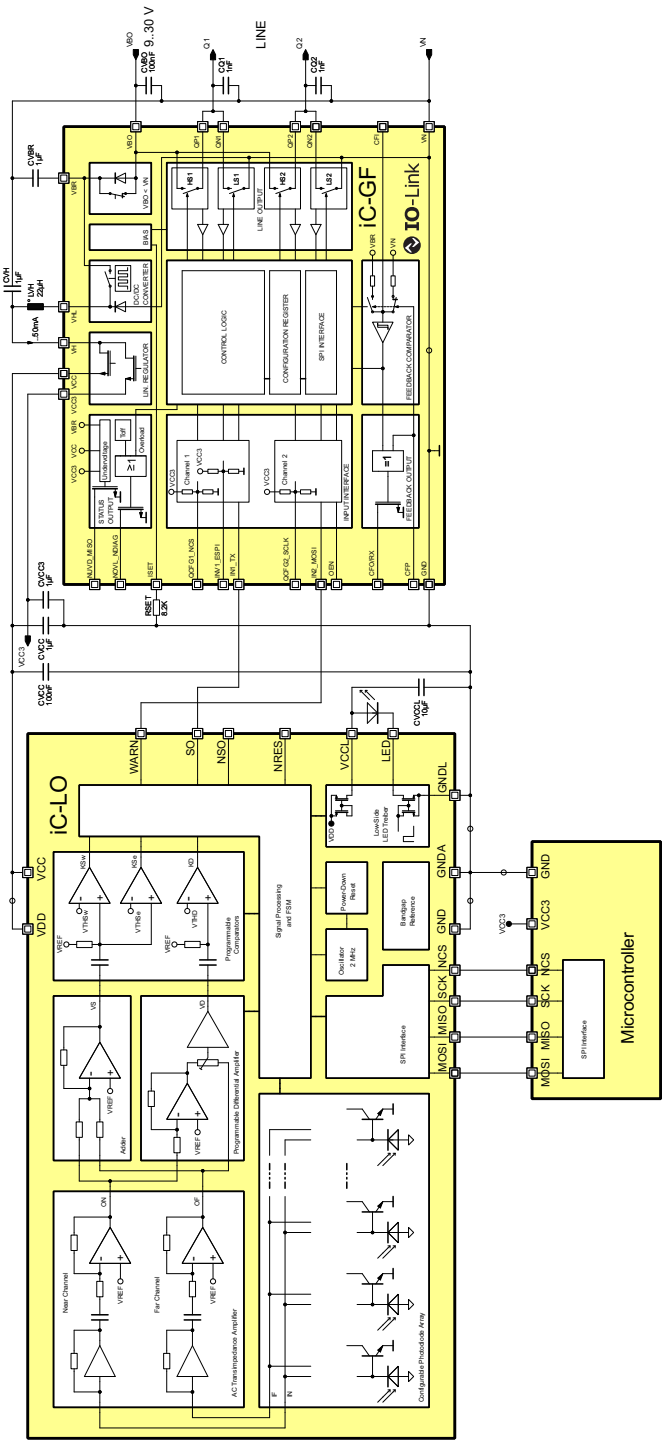


Figure 14: Application schematic

It would also be possible to combine iC-LO and iC-DN/DP/DX as switches and iC-WD as a voltage regulator. This would work for a supply voltage range of between 8 and 36 V.

DESIGN REVIEW

Prior to iC-LO revision Y and iC-LO specifications prior B2 the following applies:

Register Map

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LED DRIVER								
0x07				LCO	LCC(3:0)			
STATUS REGISTER (read only)								
0x0F	SOI	WARNI	TII(1:0)		KD(3:0)			

Table 33: Register layout

LED Driver

LCO	Addr. 0x07; bit 4	RW
Code	Description	
0x0	CMOS output at pin LED	
0x1	Low-side driver at pin LED	

Table 34: Configuration LED output type

LCC	Addr. 0x07; bit 3:0	RW
Code	Description	
0x0	94 mA	
0x1	110 mA	
...		
0x7	206 mA	
0x8	470 mA	
0x9	550 mA	
...		
0xF	1030 mA	

Table 35: Current in LED (low-side driver)

Status register

The status register is read out on a read access to register 0x0F. The switching state, warning, and transimpedance mode from the last measurement cycle are stored here, plus the last four individual differential comparator measurements. These can originate from one measurement cycle or from various individual measurement cycles with short measurement cycles. KD(0) is the most recent and KD(3) the oldest result. The switching state stored in the register is independent of SOCNO (see 16). Coding of TII is equivalent to that of TIM(1:0) (Table 11).

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	12-01-11		Initial Release	n.a.

Rel.	Rel. Date*	Chapter	Modification	Page
B1	14-05-26		iC-LO specification language only English	n.a.
		LED DRIVER	Item L03 prior iC-LO Y: I(LED)nom Nominal Current in LED V(LED) = Vs(LED)lo LCC = 0x0 86 mA LCC = 0x7 180 mA LCC = 0x8 420 mA LCC = 0xF 825 mA	12
		PACKAGING INFORMATION	oBGA replaced by optoBGA	1, 4
		ELECTRICAL CHARACTERISTICS	Item 502: typical values corrected	7
		ELECTRICAL CHARACTERISTICS	Item L01: min value changed Item L05: condition changed LCO = 0x1 Item L06 to L09: condition changed LCO = 0x0 Item 502: typical values corrected Item L12 added	8
		SPI INTERFACE	SPI interface description and timing and conditions added	20
		SPI INTERFACE	Differing to SPI specification mentioned above the MISO Pin of iC-LO is Tri State when NCS = 1.	20

Rel.	Rel. Date*	Chapter	Modification	Page
B2	14-10-30	NEAR/FAR CHANNEL PARTITION AND AMPLIFICATION	Table 11: Transimpedance Mode TIM additional column R_{ac} 112,5kΩ downto 101Ω	13
		STARTUP BEHAVIOR, OPERATING MODES, AND STATUS REGISTER	Parameter STATUS(3:0): changed from KD into LEDOK, NKDF, KSW, KSE for chip revision iC-LO Y	19
		DESIGN REVIEW	Chapter added	23

Rel.	Rel. Date*	Chapter	Modification	Page
B3	2016-08-05	ELECTRICAL CHARACTERISTICS	Item 203: typical values aligned	
		ORDERING INFORMATION	Order designation for package option added: iC-LO oBGA LO1C IR-Filter added	

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-LO	optoBGA LO1C	Default glas option, please use Order Designation with **clear option indication** below:	iC-LO oBGA LO1C
iC-LO	optoBGA LO1C	Default glas option	iC-LO oBGA LO1C Glas
iC-LO	optoBGA LO1C	IR-Filter glas option	iC-LO oBGA LO1C IR-Filter
Evaluation Board		Default glas option only	iC-LO EVAL LO1D

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