iC-MP 8-BIT HALL ANGLE ENCODER WITH RATIOMETRIC OUTPUT

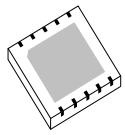
FEATURES

- Hall sensor array with automatic signal control
- Differential scanning for excellent magnetic stray field tolerance
- Real-time tracking interpolation of up to 256 angle steps, permitting up to 12,000 rpm
- Ratiometric output with 0.5 V to 4.5 V or 0 V to 5 V and selectable full-scale angle of 90, 180, 270 or 360 degrees
- Programmable zero position
- Fast, serial absolute angle data output
- Easy daisy chaining of multiple sensors: all analog/digital outputs can be used in buses
- Loss-of-magnet and excessive frequency indication via error output
- Non-volatile setup provided by 3x reconfigurable Zener zap ROM
- 5 V single-supply operation
- Power-saving standby function
- Operational temperature range of -40 to +125 °C
- Space-saving 10-pin DFN package measuring 4 mm x 4 mm

APPLICATIONS

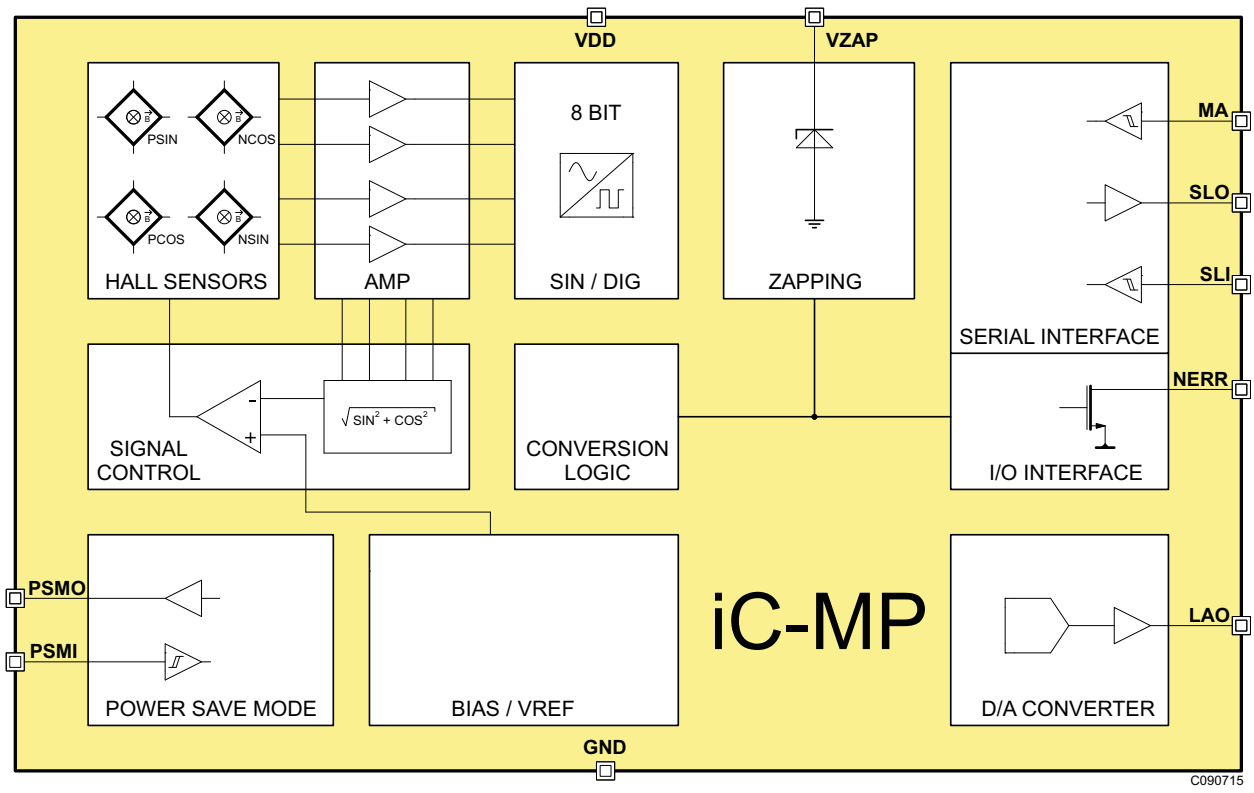
- Contactless potentiometer
- Absolute 360° angle sensor
- Magnetic rotary encoders

PACKAGES



DFN10 4 x 4 mm

BLOCK DIAGRAM



DESCRIPTION

iC-MP consists of a quadruple Hall sensor array which has been optimized for the magnetic measurement of an axis angle. The array permits error-tolerant adjustment of the magnet, reducing the time and effort required assembly. The integrated signal conditioning unit provides a differential sine/cosine signal at its outputs. The sensor generates one sine cycle per full rotation of the magnet, enabling the angle to be clearly determined. At the same time the internal amplitude control unit produces a regulated output amplitude of 2 Vpp, regardless of variations in the magnetic field strength, supply voltage and temperature. Furthermore, error signals are provided which report any magnet loss and an excessively high RPM speed.

With the aid of the integrated 8-bit sine-to-digital converter the axis angle is determined from the sine/cosine signals. The absolute position angle is output via the serial interface together with a bit indicating an error. The maximum resolution of 8 bits is maintained up to revolutions of 12,000 rpm.

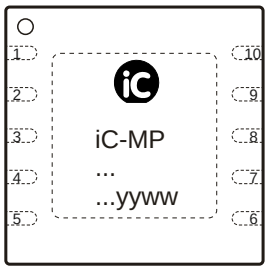
The absolute angle is converted back to a linear analog output voltage using the internal D/A converter. The analog output voltage range can be programmed to be either rail to rail or 10 % to 90 % of the supply voltage. The angular range of the analog signal is configurable to 90°, 180°, 270° or 360°.

iC-MP can be easily cascaded, enabling scanning of multiple axes. In Fast Scanning Mode all devices connected in a queue are read consecutively. In Slow Scanning Mode (Power Save Mode) each individual device is booted up before the serial data or analog output voltage is put on the common bus.

CONTENTS

PACKAGES

PIN CONFIGURATION DFN10



PIN FUNCTIONS

No.	Name	Function
1	PSMI	Power Save Mode Input
2	GND	Ground
3	PSMO	Power Save Mode Output
4	LAO	Linear Analog Output
5	MA	Serial Clock Input
6	SLO	Serial Data Output
7	SLI	Serial Data Input
8	VZAP	Zapping Voltage Input
9	VDD	+5 V Supply Voltage
10	NERR	Error Message Output (low active) / Serial ROM Data Output
	TP	Thermal Pad

The *thermal pad* must be connected to ground potential on the PCB.
Orientation of the logo (iC MP CODE ...) is subject to alteration.

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Supply Voltage at VDD		-0.3	6	V
G002	I()	Current in VDD		-20	20	mA
G003	V()	Voltage at pins PSMI, PSMO, LAO, MA, SLO, SLI, NERR		-0.3	VDD + 0.3	V
G004	V()	Voltage at pin VZAP		-0.3	8	V
G005	I()	Current in pins PSMI, PSMO, LAO, MA, SLO, SLI, NERR, VZAP		-10	10	mA
G006	I()	Current in pins PSMI, PSMO, LAO, MA, SLO, SLI, NERR, VZAP	Pulse width < 10µs	-100	100	mA
G007	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G008	Tj	Junction Temperature		-40	125	°C
G009	Ts	Storage Temperature Range		-40	125	°C

THERMAL DATA

Operating conditions: VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operation Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance, Chip to Ambient	Package mounted on PCB, thermal pad at approx. 2 cm² cooling area		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10 % , Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD	Supply Voltage		4.5	5	5.5	V
002	I(VDD)	Supply Current in VDD	PSMI = lo, other pins open		8	12	mA
003	I(VDD)sb	Standby Supply Current	PSMI = hi			200	µA
004	VDDon	Power-On Threshold	Increasing voltage VDD	3.0		4.1	V
005	VDDoff	Power-Down Threshold	Decreasing voltage VDD	2.6		3.9	V
006	VDDhys	Hysteresis	VDDhys = VDDon - VDDoff	200			mV
007	ton()1	Turn-On Delay Following Power-On	Time to data valid after enabling, VDD: VDDoff → VDDon			1	ms
008	ton()2	Turn-On Delay Following Standby	Time to data valid after standby, PSMI: hi → lo			900	µs
009	Vc()hi	Clamp Voltage hi at PSMI, MA, SLI, NERR	VDD = 0 V; I() = 1 mA	0.3		1.6	V
010	Vc()hi	Clamp Voltage hi at PSMO, LAO, SLO	VDD = 0 V; I() = 4 mA	0.3		1.6	V
011	Vc()lo	Clamp Voltage lo at PSMI, PSMO, LAO, MA, SLO, SLI, NERR, VDD, VZAP	I() = -4 mA	-1.5		-0.3	V
Hall Sensor Array							
101	Hext	Operating Magnetic Field Strength	At surface of chip	20	50	100	kA/m
102	RPM	Permissible RPM Speed				12 000	rpm
103	ferr()	Excessive Frequency Alarm	ENERR(1) = 1; NERR: hi → lo		1		kHz
104	fmag()	Magnetic Field Frequency				200	Hz
105	dsens	Diameter of Hall Sensor Array			2		mm
106	xpac	Chip Placement Tolerance	Versus DFN10 package outlines	-0.2		0.2	mm
107	ϕpac	Chip Tilt Angle	Versus DFN10 package outlines	-3		3	DEG
108	hpac	Distance Surface of Package to Surface of Chip	DFN10 package		400		µm
Sine-To-Digital Converter							
301	RES	Converter Resolution	Per 360 degree		8		bit
302	HYS	Converter Hysteresis			1.4		DEG
303	AAabs	Absolute Angle Accuracy	Magnet with 4 mm in diameter, axis centered to chip	-3		3	DEG
D/A Converter And Ratiometric Output LAO							
401	RES()	D/A Converter Resolution	MODE(1:0) = 00 (range 360°) MODE(1:0) = 01 (range 270°) MODE(1:0) = 10 (range 180°) MODE(1:0) = 11 (range 90°)		8 7.5 7 6		bit bit bit bit
402	Iload()	Permissible Output Current		-1		1	mA
403	dV0()hi	Output Voltage hi, Rail-To-Rail	dV0()hi = V(VDD) - V(LAO), MODE(3) = 0; I() = -1 mA I() = 0 mA			 170 85	 mV mV
404	dV0()lo	Output Voltage lo, Rail-To-Rail	MODE(3) = 0; I() = 1 mA I() = 0 mA			 170 85	 mV mV
405	dV1()hi	Output Voltage hi, 10/90% Range	MODE(3) = 1; I() = -1...+1 mA	85		95	%VDD
406	dV1()lo	Output Voltage lo, 10/90% Range	MODE(3) = 1; I() = -1...+1 mA	5		15	%VDD
407	Ilk()	Leakage Current	V(LAO) = 0...VDD, PSMI = hi	-5		5	µA
408	SR()hi	Slew Rate hi	V(LAO): 20% → 80% of range	2			V/µs
409	SR()lo	Slew Rate lo	V(LAO): 80% → 20% of range	2			V/µs
Zapping Input VZAP							
501	Vt1()hi	Voltage Threshold hi vs. GND				2	V
502	Vt1()lo	Voltage Threshold lo vs. GND		0.8			V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10 % , Tj = -40 ... 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
503	Vt1()hys	Threshold Hysteresis	Vt1()hys = Vt1()hi – Vt1()lo	230		400	mV
504	Vt2()hi	Voltage Threshold hi vs. VDD	Vt2()hi = V() - VDD, VDD = 5 V ±5%, Tj = 10 ... 40 °C			1.3	V
505	Vt2()lo	Voltage Threshold lo vs. VDD	Vt2()lo = V() - VDD; VDD = 5 V ±5%, Tj = 10 ... 40 °C	0.7			V
506	Vt2()hys	Threshold Hysteresis	Vt2()hys = Vt2()hi – Vt2()lo	20		150	mV
507	Vzap()	Permissible Zapping Voltage	VDD = 5 V ±5%, Tj = 10 ... 40 °C	7.3	7.4	7.5	V
508	Izap()	Required Zapping Current	VDD = 5 V ±5%, Tj = 10 ... 40 °C			90	mA
Serial Interface and Power Save Mode Inputs: MA, SLI, PSMI							
601	Vt()hi	Input Threshold Voltage hi				2	V
602	Vt()lo	Input Threshold Voltage lo		0.8			V
603	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	230			mV
604	Ipu()	Input Pull-up Current	V() = 0...VDD – 1 V	-240	-120	-10	µA
605	fclk(MA)	Permissible Clock Frequency at MA	Normal mode	0.080		10	MHz
606	tzap(MA)	Permissible Zapping Cycle at MA	Programming mode, VDD = 5 V ±5%, Tj = 10 ... 40 °C	4.5	5	5.5	µs
607	tout(MA)	Interface Timeout	Time from MA last edge to SLO lo → hi			15	µs
Serial Interface and Power Save Mode Outputs: SLO, PSMO							
701	Vs()hi	Saturation Voltage hi	Vs()hi = VDD – V(), I() = -4 mA			0.4	V
702	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
703	Isc()hi	Short-Circuit Current hi	V() = 0 V	-90		-10	mA
704	Isc()lo	Short-Circuit Current lo	V() = VDD	10		90	mA
705	tr()	Rise Time	CL() = 50 pF, V(): 20 → 80%			60	ns
706	tf()	Fall Time	CL() = 50 pF, V(): 80 → 20%			60	ns
I/O Interface NERR							
801	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
802	Ilk()	Leakage Current	V() = 0...VDD, PSMI = hi	-5		5	µA
803	Isc()lo	Short-Circuit Current lo	V() = VDD	4.5		90	mA
Test Signals at NERR, LAO, PSMO (iC-Haus device test only)							
902	VREF	Reference Voltage at LAO	Op. mode: Test 2	45	50	55	%VDD
904	Vpp(PSIN)	Pos. Sine Sensor AC Signal at NERR	Op. mode: Test 0		2		Vpp
905	Vdc(PSIN)	Pos. Sine Sensor DC Signal at NERR	Op. mode: Test 0		VREF		V
906	Vpp(PCOS)	Pos. Cosine Sensor AC Signal at LAO	Op. mode: Test 0		2		Vpp
907	Vdc(PCOS)	Pos. Cosine Sensor DC Signal at LAO	Op. mode: Test 0		VREF		V
908	Vpp(NSIN)	Neg. Sine Sensor AC Signal at NERR	Op. mode: Test 1		2		Vpp
909	Vdc(NSIN)	Neg. Sine Sensor DC Signal at NERR	Op. mode: Test 1		VREF		V
910	Vpp(NCOS)	Neg. Cosine Sensor AC Signal at LAO	Op. mode: Test 1		2		Vpp
911	Vdc(NCOS)	Neg. Cosine Sensor DC Signal at LAO	Op. mode: Test 1		VREF		V
912	dVoff()	Diff. Sine and Cosine Signal Offsets	dVoff() = V(PSIN) – V(NSIN), dVoff() = V(PCOS) – V(NCOS)	-50		50	mV
913	VR()	Sine/Cosine AC Signal Ratio	VR() = V(PSIN) / V(PCOS), VR() = V(NSIN) / V(NCOS)	0.95		1.05	

SENSOR PRINCIPLE

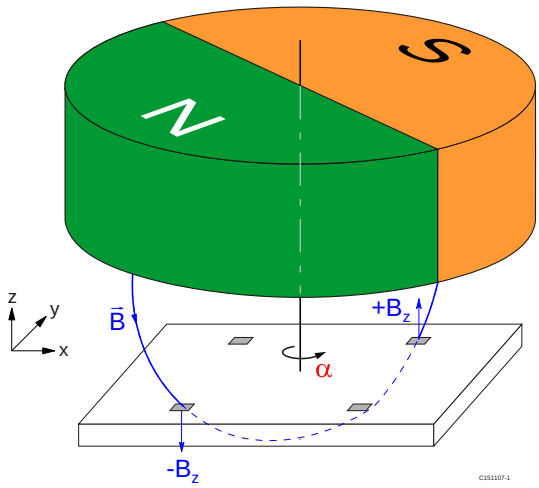


Figure 1: Sensor principle

In conjunction with a rotating permanent magnet, the iC-MP module can be used to create a complete encoder system or a contactless potentiometer. A diametrically magnetized, cylindrical permanent magnet made of neodymium iron boron (NdFeB) or samarium cobalt (SmCo) generates optimum sensor signals. The diameter of the magnet should be in the range of 3 mm to 6 mm.

The iC-MP has four Hall sensors adapted for angle determination and to convert the magnetic field into a measurable Hall voltage. Only the z-component of the magnetic field is evaluated, whereby the field lines pass through two opposing Hall sensors in the opposite direction. Figure 1 shows an example of field vectors.
The arrangement of the Hall sensors is selected so that the mounting of the magnets relative to iC-MP is extremely tolerant. Two Hall sensors combined provide a differential Hall signal. When the magnet is rotated around the longitudinal axis, sine and cosine output voltages are produced which can be used to determine angles.

HALL SENSOR POSITION AND INTERNAL ANALOG SIGNALS

The Hall sensors are placed in the center of the DFN10 package at 90° to one another and arranged in a circle with a diameter of 2 mm as shown in Figure 2.

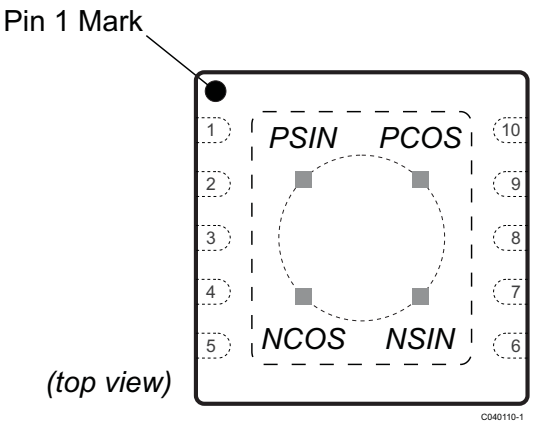


Figure 2: Position of the Hall sensors

In order to calculate the angle position of a diametrically polarized magnet placed above the device a difference in signal is formed between opposite pairs of Hall sensors, resulting in the sine being $V_{SIN} = V_{PSIN} - V_{NSIN}$ and the cosine $V_{COS} = V_{PCOS} - V_{NCOS}$. The zero angle position of the magnet is marked by the resulting cosine voltage value being at a maximum and the sine voltage value at zero.

This is the case when the south pole of the magnet is exactly above the PCOS sensor and the north pole is above sensor NCOS, as shown in Figure 3. Sensors PSIN and NSIN are placed along the pole boundary so that neither generate a Hall signal.

When a magnetic south pole comes close to the surface of the package the resulting magnetic field has a positive component in the +z direction (i.e. from the top of the package) and the individual Hall sensors each generate their own positive signal voltage.

When the magnet is rotated counterclockwise the poles then also cover the PSIN and NSIN sensors, resulting in the sine and cosine signals shown in Figure 4 being produced. The signals are internal but can be made externally available for test purposes (see chapter 'TEST MODES').

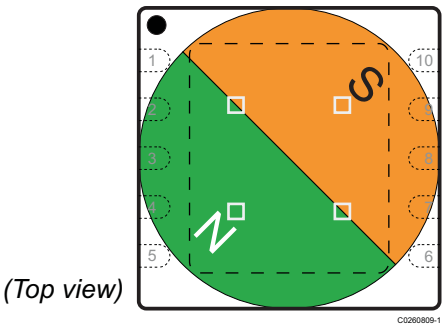


Figure 3: Zero position of the magnet

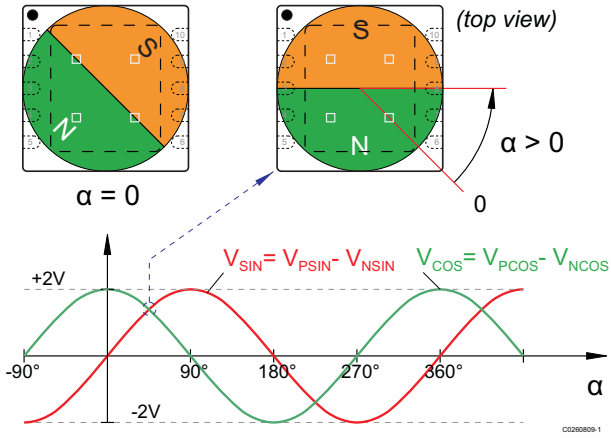


Figure 4: Pattern of the internal analog sensor signals with the angle of rotation

LINEAR ANALOG OUTPUT (LAO)

The LAO pin provides a linear analog output voltage representing the actual position. The output voltage can be either rail to rail or within a range of 10% to 90% of the supply voltage VDD, depending on the programmed configuration. In 10%-to-90% mode a short-circuit with VDD or GND is recognizable.

The zero position therefore begins at the minimum voltage (either GND or 10% of VDD) and reaches its maximum (either VDD or 90% of VDD) at the selected angular range limit (90°, 180°, 270° or 360°), depending on the chosen configuration.

LAO is tristate when the device is disabled.

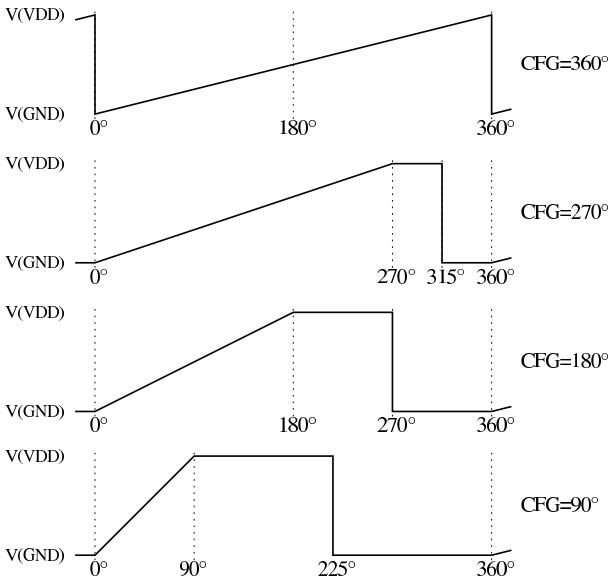


Figure 5: Linear analog output voltage

SERIAL OUTPUT (SLO)

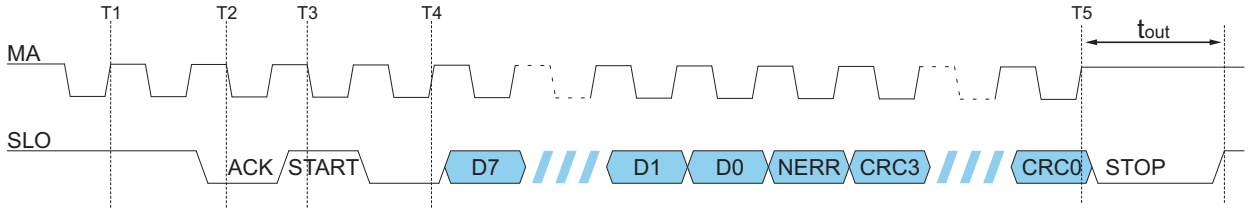


Figure 6: Serial data timing

D0 to D7 make up the absolute position data with respect to the programmed position offset (OFFSET1 xor OFFSET2 xor OFFSET3).

The absolute position is latched by a low to high transition at MA (see T1).

After an acknowledge (T2) at SLO iC-MP requests processing time until the start condition (T3) is sent. Processing time must be provided in Slow Scanning Mode during startup.

With rising edge T4 at the clock pin the most significant bit (D7) is placed on the serial data line SLO. After T5 has elapsed the controller can stop clocking at MA and the device is ready to latch a new position after a timeout (t_{out}). If the controller continues to clock in a daisy chain in Fast Scanning Mode after T5 has elapsed, the second device (slave 2) outputs the position latched at T1 at pin SLO.

The absolute position data (D0-D7) is binary coded. The position data and the error bit (NERR) are CRC protected. The CRC polynomial is X^4+X+1 = 0x13.

```
CRC_Value = CRCID;     //CRC start value,
                       //Parameter CRCID  D(45:42)
CRC_Poly = 0x13;       //CRC Polynoma
Sens_Data = D + NERR; //Protected Sensor Data 9bit

for (i=0; i<8; i++)
{
  if ((CRC_Value & 0x100) != (Sens_Data & 0x100))
    CRC_Value = (CRC_Value << 1) ^ CRC_Poly;
  else
    CRC_Value = (CRC_Value << 1);
  Sens_Data = Sens_Data << 1;
}
```

Figure 7: Example CRC calculation

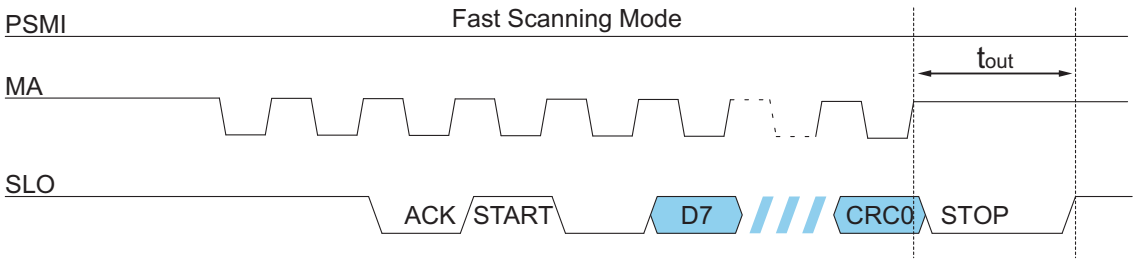


Figure 8: Timing in Fast Scanning Mode

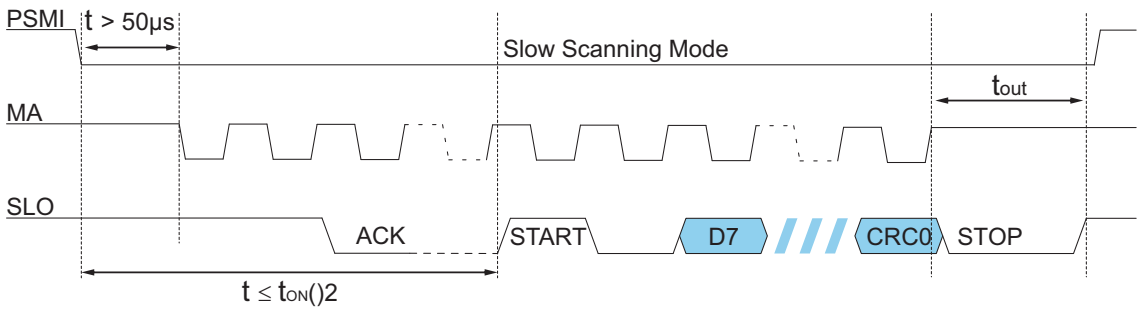


Figure 9: Timing in Slow Scanning Mode

OPERATING MODES

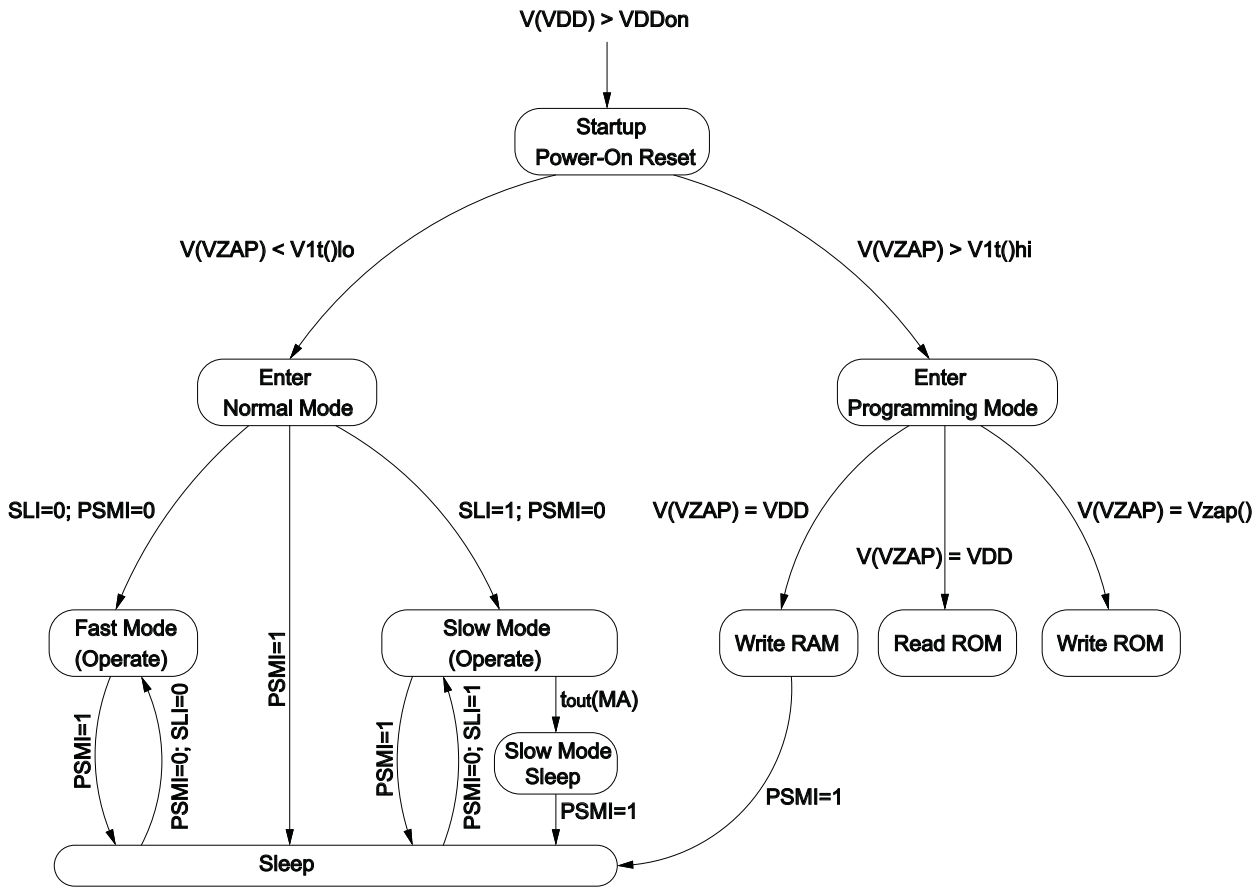


Figure 10: Operation Modes

Figure 10 shows the different modes of iC-MP. There are two major modes of operation:

- **Normal Mode:**
  Readout position data and error bit. Normal mode is subdivided into two minor modes of operation:
  - **Fast Scanning Mode:**
    iC-MP is always activated.
  - **Slow Scanning Mode (Power Save Mode):**
    iC-MP goes into Slow Mode Sleep following the first transmission of sensor data via the serial interface.
- **Programming Mode:**
  iC-MP can be configured in programming mode. See the chapter on 'PROGRAMMING MODE' for further details. There are three minor modes:
  - **Read ROM:**
    iC-MP's Zener zap ROM structure is read.
  - **Write RAM:**
    iC-MP's internal registers can be temporarily programmed for test purposes.
  - **Write ROM:**
    iC-MP's zapping structure is programmed.

A Power-On Reset is required after a Read ROM and Write ROM instruction. Each state is quit by a Power-On Reset.

PROGRAMMING MODE

When pulling the VZAP pin to high during startup, the programming mode is entered (see 'OPERATING MODES'). In this mode there are three different categories of operation:

- **Write ROM Mode** (V(VZAP) = V_{zap}(), according to ELEC.CHAR., no. 507):
  In Write ROM Mode each Zener zap diode is burned (= zapped) immediately on the rising edge of MA. See Figure 13 for details. For the conditions of operation of Write ROM Mode, see ELEC.CHAR., 'Zapping Input VZAP'.
- **Write RAM Mode** (V(VZAP) = VDD):
  In Write RAM Mode the iC-MP reacts as in Write ROM Mode but there is no zapping of the Zener zap diodes. This mode can be used to temporarily program iC-MP (non-permanent) for test purpose.
- **Read ROM** (V(VZAP) = VDD):
  In Read ROM Mode the content of the Zener zap diodes is read out. A Read ROM operation overwrites iC-MP's RAM content.

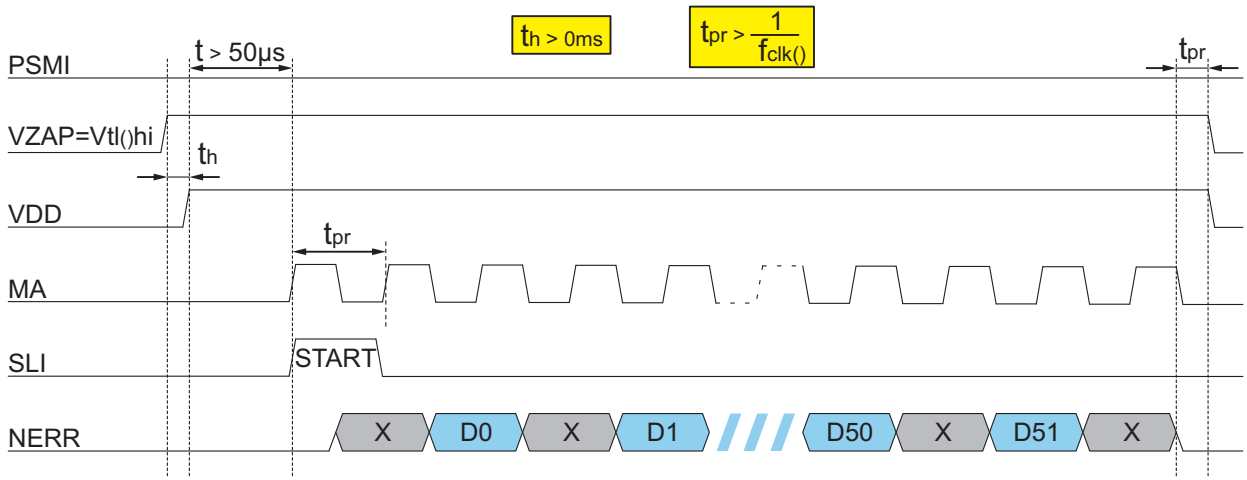


Figure 11: Serial timing of Read ROM Mode

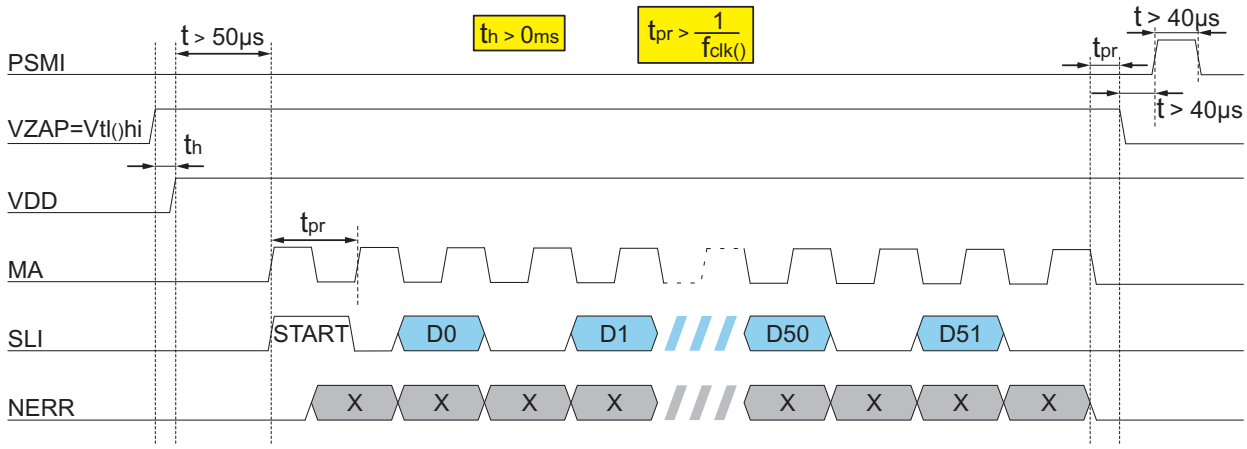


Figure 12: Serial timing of Write RAM Mode

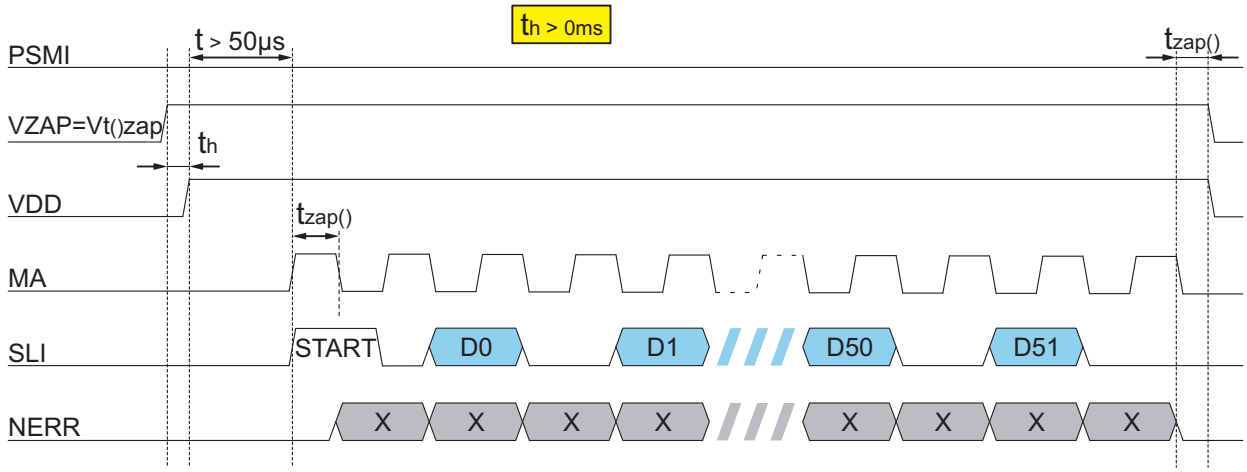


Figure 13: Serial timing of Write ROM Mode

Figure 13 shows the serial timing of a Write ROM operation (burning the Zener zap diodes). The bit stream is described in Table 4. Each Zener zap diode can be programmed once with a logic of '1'. The default value of the Zener zap diodes is a logic '0' (with the exception of ZTEST(1:0)). The resulting parameter (OFFSET, MODE and ENERR) are generated by an xor operation of the three sets of bits (see Figure 15).

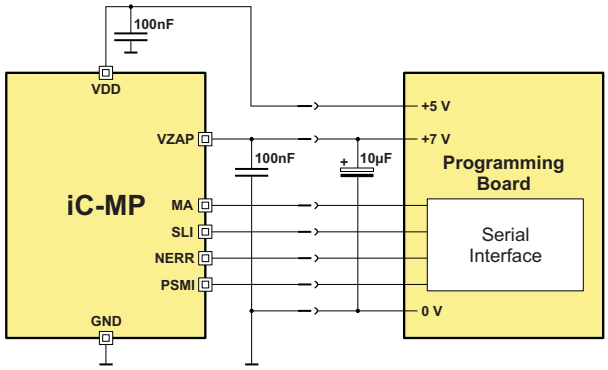


Figure 14: In-circuit programming

A 100 nF ceramic block capacitor must be placed on the board directly between iC-MP's VZAP and GND pins. A 10 µF capacitor must also be present at the end of the programming line as close to the connector as possible (see Figure 14). During programming, up to 90 mA flow from pin VZAP to pin GND, making it necessary to ensure proper PCB layout to minimize voltage drops.

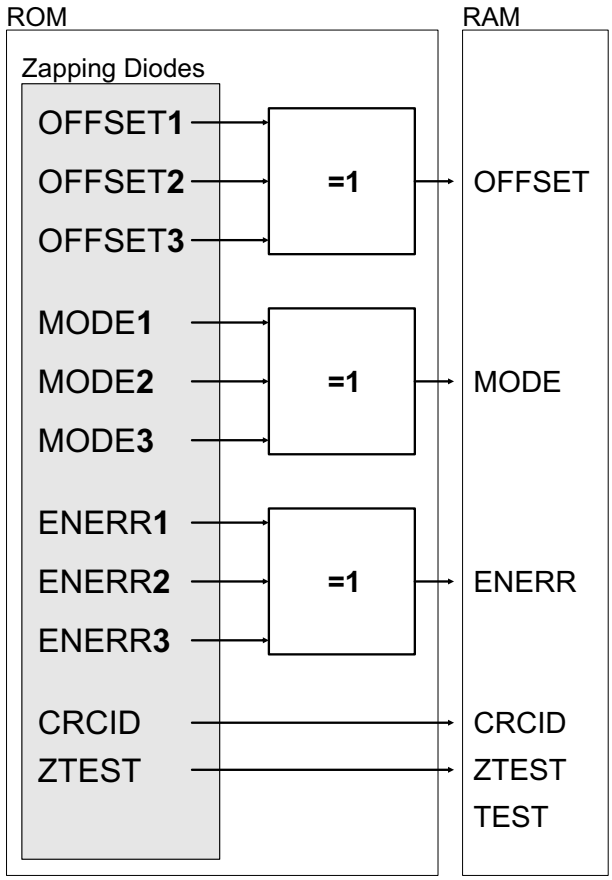


Figure 15: ROM construction

D(51:0)	Parameter	Description
7:0	OFFSET1(7:0)	Offset of the first set
11:8	MODE1(3:0)	Mode of the first set, see Table 5 and 6
13:12	ENERR1(1:0)	Error mask of the first set, see Table 8
21:14	OFFSET2(7:0)	Offset of the second set
25:22	MODE2(3:0)	Mode of the second set, see Table 5 and 6
27:26	ENERR2(1:0)	Error mask of the second set, see Table 8
35:28	OFFSET3(7:0)	Offset of the third set
39:36	MODE3(3:0)	Mode of the third set, see Table 5 and 6
41:40	ENERR3(1:0)	Error mask of the third set, see table 8
45:42	CRCID(3:0)	CRC ID
47:46	ZTEST(1:0)	Zener zap diodes, for iC-Haus test purposes only
51:48	TEST(3:0)	See 'TEST MODES'

Table 4: Programming Datastream

MODE1(1:0)	D(9:8)
MODE2(1:0)	D(23:22)
MODE3(1:0)	D(37:36)
Code	Full Scale Angle
00	360°
01	270°
10	180°
11	90°

Table 5: Linear Analog Output - Mode Bit 1:0

MODE1(2)	D(10)
MODE2(2)	D(24)
MODE3(2)	D(38)
Code	Rotation
0	CW*
1	CCW*
*) CW = clockwise, CCW = counter-clockwise	

Table 6: Mode Bit 2

MODE1(3)	D(11)
MODE2(3)	D(25)
MODE3(3)	D(39)
Code	Range
0	(0 % - 100 %) * VDD
1	(10 % - 90 %) * VDD

Table 7: Linear Analog Output - Mode Bit 3

ENERR

The parameter ENERR indicates two kind of errors. If the magnetic field strength is at low a 'Loss of Magnet' is generated. An 'Excessive Frequency Alarm' is generated when the revolution per minute is to high. Parameter ENERR handles the various error types.

ENERR1(1:0)	D(13:12)
ENERR2(1:0)	D(27:26)
ENERR3(1:0)	D(41:40)
Code	Error
00	No Error
01	Loss of Magnet*
10	Excessive Frequency Alarm
11	Excessive Frequency Alarm or Loss of Magnet*
*) see 'DESIGN REVIEW'	

Table 8: Error masks

Calculating the position offset

Before iC-MP outputs the actual position via the serial interface or the linear analog output (LAO), an offset is added internally. This offset consists of the following parameters:

OFFSET = OFFSET1 xor OFFSET2 xor OFFSET3

The offset is programmed in several stages (see Figure 16). It is important that the direction of rotation is programmed prior to this (MODE Bit 2). To determine the actual configured offset, all three offset parameters must be read out. After these parameters have been xored the actual offset is determined:

Actual Offset = OFFSET1 xor OFFSET2 xor OFFSET3

To calculate the new offset the actual position at the required offset is required. The formula used to calculate this new offset is as follows:

New Offset = 256 - Actual Position + Actual Offset

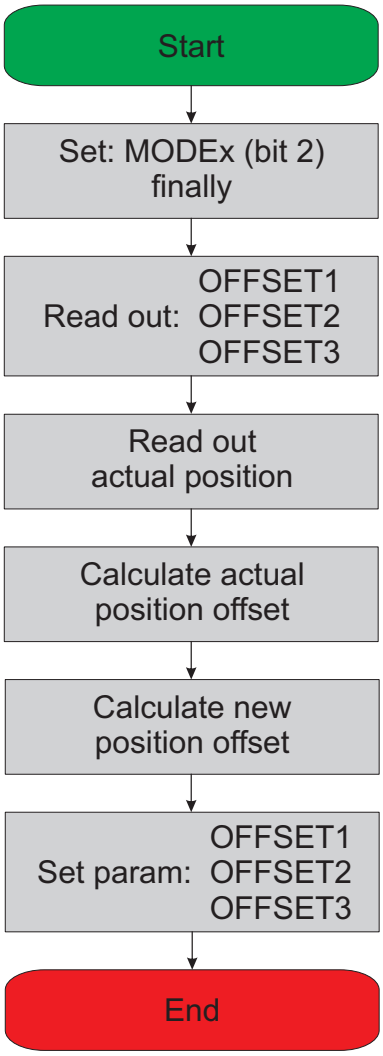


Figure 16: Principle of offset calculation

CRCID
The CRCID parameter contains the CRC start value. Configuring the CRC starting value enables a data value to be clearly assigned to a slave, as the CRC check fails with a faulty configuration of the master or an exchange sequence. For example, the controller assigns a start value for each slave and writes these to the CRCID slave parameter.
For CRC calculation, see 'SERIAL OUTPUT (SLO)'.

FAST SCANNING MODE

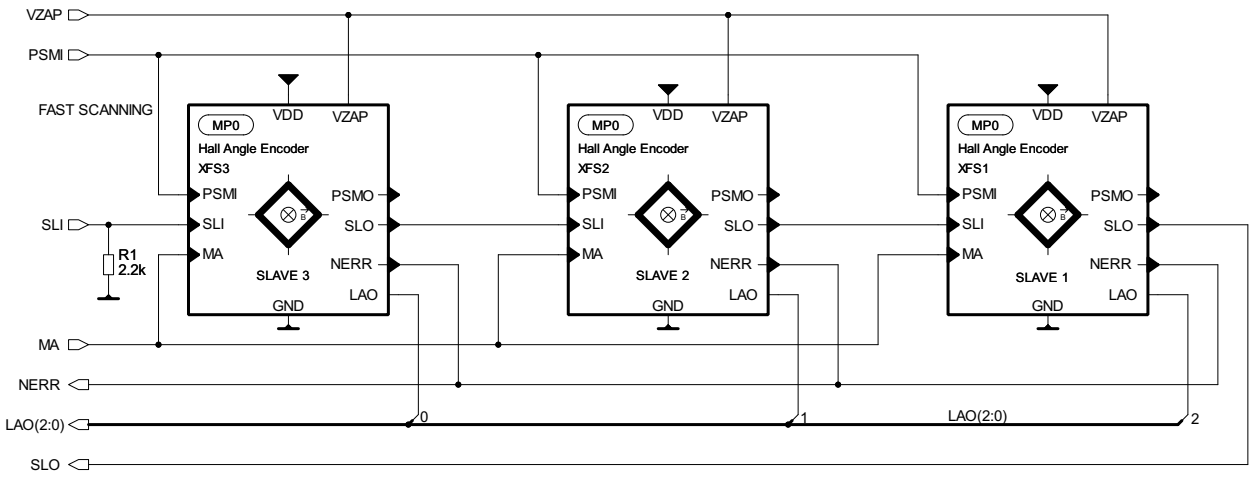
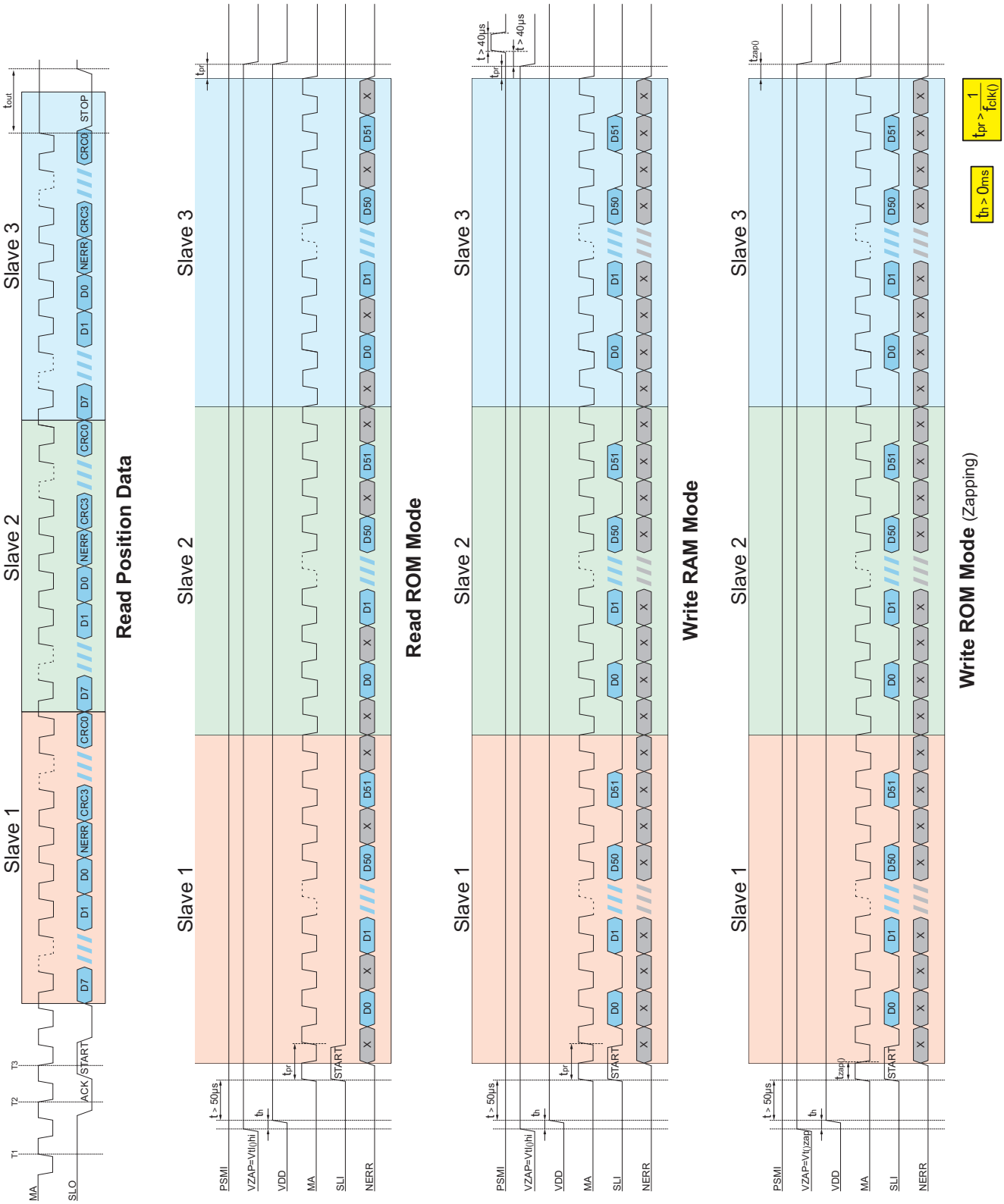


Figure 17: Fast Scanning Mode

In Fast Scanning Mode all devices are active at the same time. With a start condition at MA the absolute position of all devices is latched and all absolute positions are transferred as one long data word (see page 17). Parameter CRCID can be used for improved differentiation of the individual data words. See 'PROGRAMMING MODE'.


Read Position Data
Slave 1
Slave 2
Slave 3
MA
SLO
T1
T2
T3
ACK
START
D7
D1
D0
NERR
CRC3
CRC0
STOP
tout
Read ROM Mode
PSMI
VZAP=Vt(),hi
VDD
MA
SLI
NERR
tpr
th
t > 50µs
START
D51
D50
X
Write RAM Mode
t > 40µs
Write ROM Mode (Zapping)
tzap()
VZAP=Vt(),zap
tzap()
tpr > 1 / fclk()
th > 0ms

SLOW SCANNING MODE

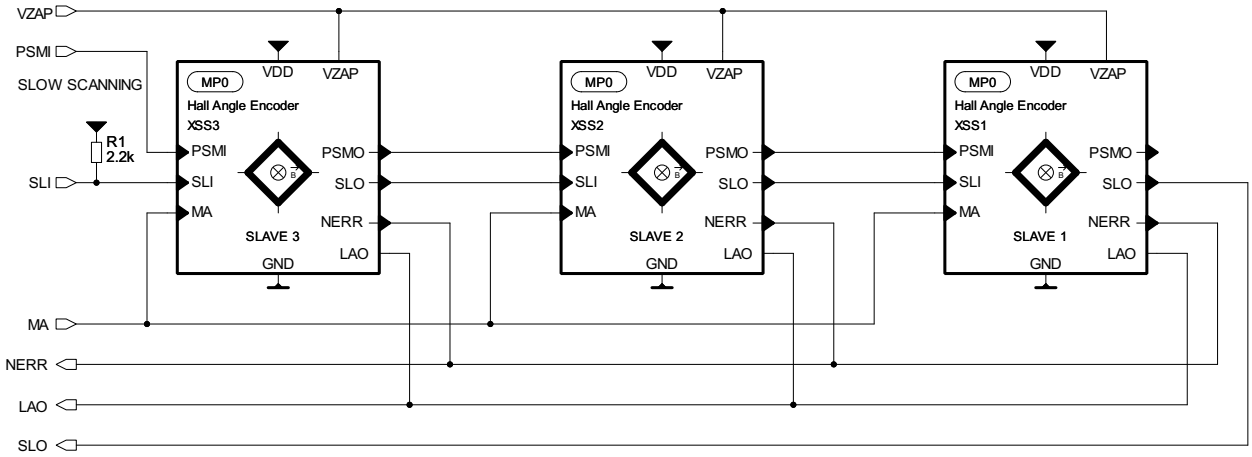
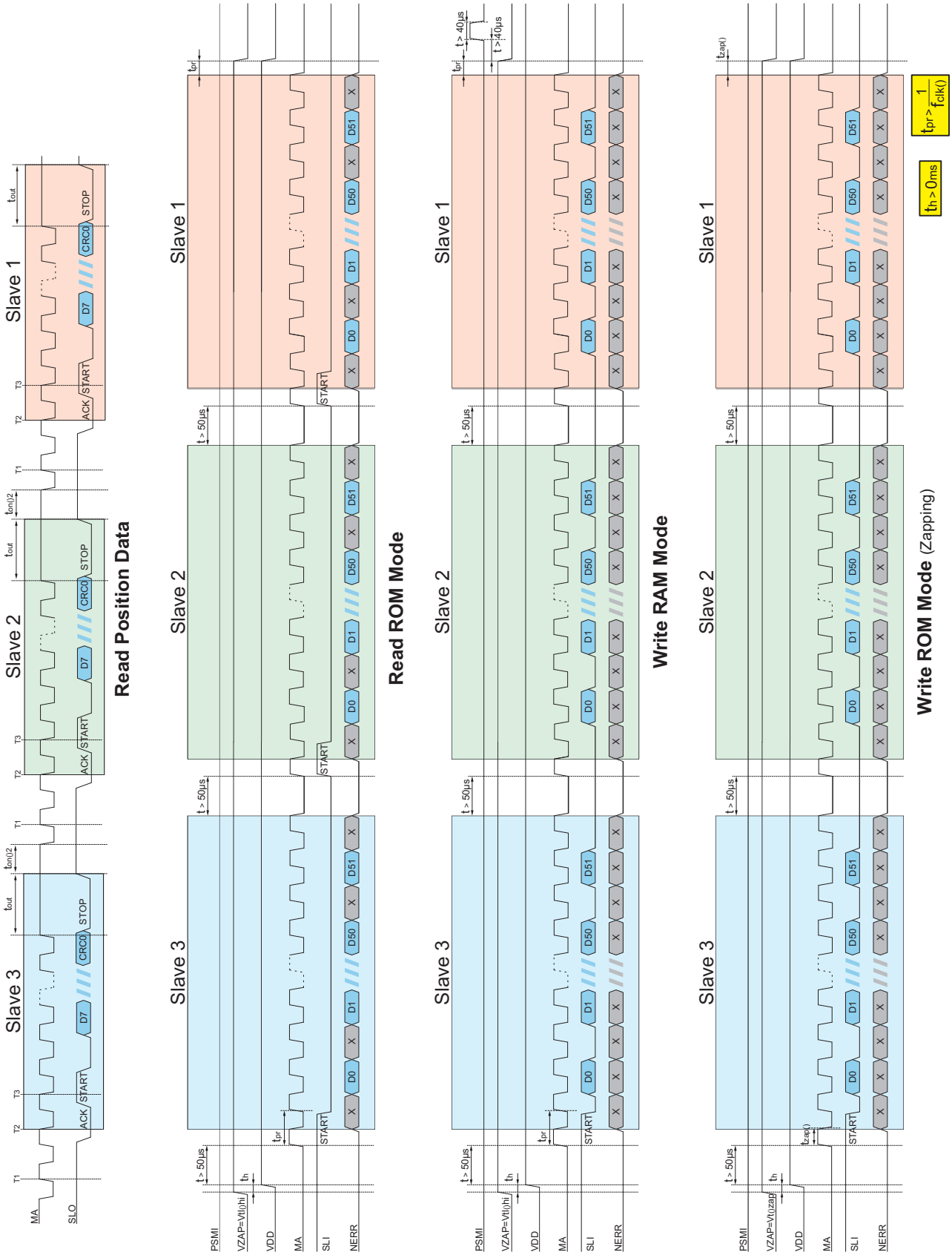


Figure 18: Slow Scanning Mode

In Slow Scanning Mode only one device is activated in a chain. This device transmits its absolute position on the SLO bus and the analog output voltage to the LAO bus. After an timeout at SLI, the next device is enabled (PSMO hi → lo). The devices needs some time after activation to find the actual position.
Parameter CRCID can be used for improved differentiation of the individual data words. See 'PROGRAMMING MODE'.
The chain is reset by a logic high at the PSMI pin (see page 19).

Application hints:
See 'DESIGN REWIEW'.


Slave 1
Slave 2
Slave 3
MA
SLO
START
ACK
D7
D0
D1
D50
D51
CRC0
STOP
Read Position Data
PSMI
VDD
SLI
NERR
Read ROM Mode
Write RAM Mode
Write ROM Mode (Zapping)
t > 50µs
t > 40µs
t > 0ms

APPLICATION CIRCUITS

Stand-alone example

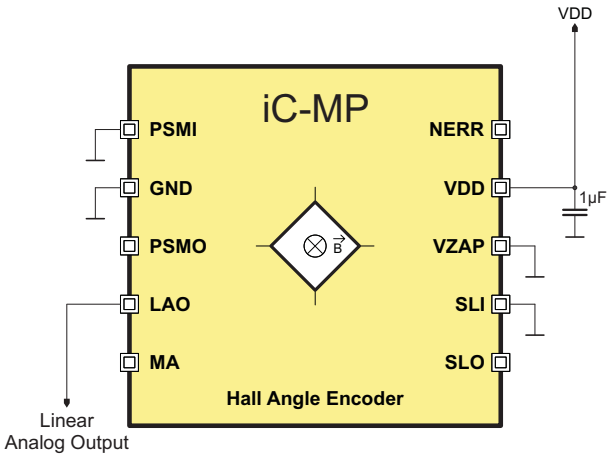


Figure 19: Circuit for stand-alone operation

Figure 19 shows an example circuit for stand-alone operation of iC-MP. The device is in Fast Scanning Mode. If the device is also to be programmed, pins PSMI, SLI and VZAP should be connected to GND by a pull-down resistor (e.g. 2.2 kΩ).

TEST MODES

iC-MP has several test settings which make internal reference quantities and the amplified, differential Hall voltages of the sensor pairs accessible at external pins for measurement purposes. This signals enables a chip/package to be adjusted in relation to the magnet.

Test modes can be triggered by programming the parameter TEST (D(51:48)). The individual test modes are listed in the following table.
See 'ELECTRICAL CHARACTERISTICS'.

Op. Mode	TEST(3:0)	Pin NERR		Pin LAO	Pin PSMO	Comments
		analog	digital			
Normal	0ddd	-	NERR	LAO	PSMO	
Test 0	1000	PSIN	-	PCOS	PSMO	
Test 1	1001	NSIN	-	NCOS	PSMO	
Test 2	1010	GAIN	-	VREF	PSMO	
Notes	d = don't care					

Table 9: Test modes

DESIGN REVIEW: Notes On Chip Functions

iC-MP Y		
No.	Function, Parameter/Code	Description and Application Notes
1	**Slow Scanning Mode** (without a magnet):	Serial Interface Mode is discontinued without a magnet - The start bit is not available - The daisy chain is stopped

Table 10: Notes on chip functions regarding iC-MP chip releas Y

ORDERING INFORMATION

Type	Package	Order Designation
iC-MP	DFN10	iC-MP DFN10
Evaluation Board		iC-MP EVAL MP1D

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Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.com/sales_partners