iC-PD 3948

PHASED ARRAY SINE ENCODER

preliminary

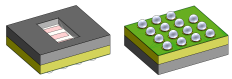
FEATURES

- Compact, 5-channel encoder sensor with differential scanning and analog sine/cosine outputs:
  2048 CPR with index, 1 CPR absolute, size ⌀ 39 mm
- Phased-array design for excellent signal matching
- Reduced cross talk due to moderate track pitch
- Ultra low dark currents for operation up to high temperature
- Low noise amplifiers with high transimpedance
- Short-circuit-proof, low impedance voltage outputs for enhanced EMI tolerance
- Space saving optoQFN and optoBGA packages (RoHS compliant)
- Low power consumption from single 4.5 to 5.5 V supply
- Operational temperature range of -40 to +110 °C
- Suitable code disc:
  PD2S 39-2048 (glass 1 mm)
  OD ⌀ 39 mm, ID ⌀ 18.0 mm, optical radius 17.5 mm

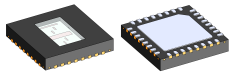
APPLICATIONS

- Incremental sine encoders with commutation information
- Motor feedback
- AC servo and BLDC motor systems

PACKAGES

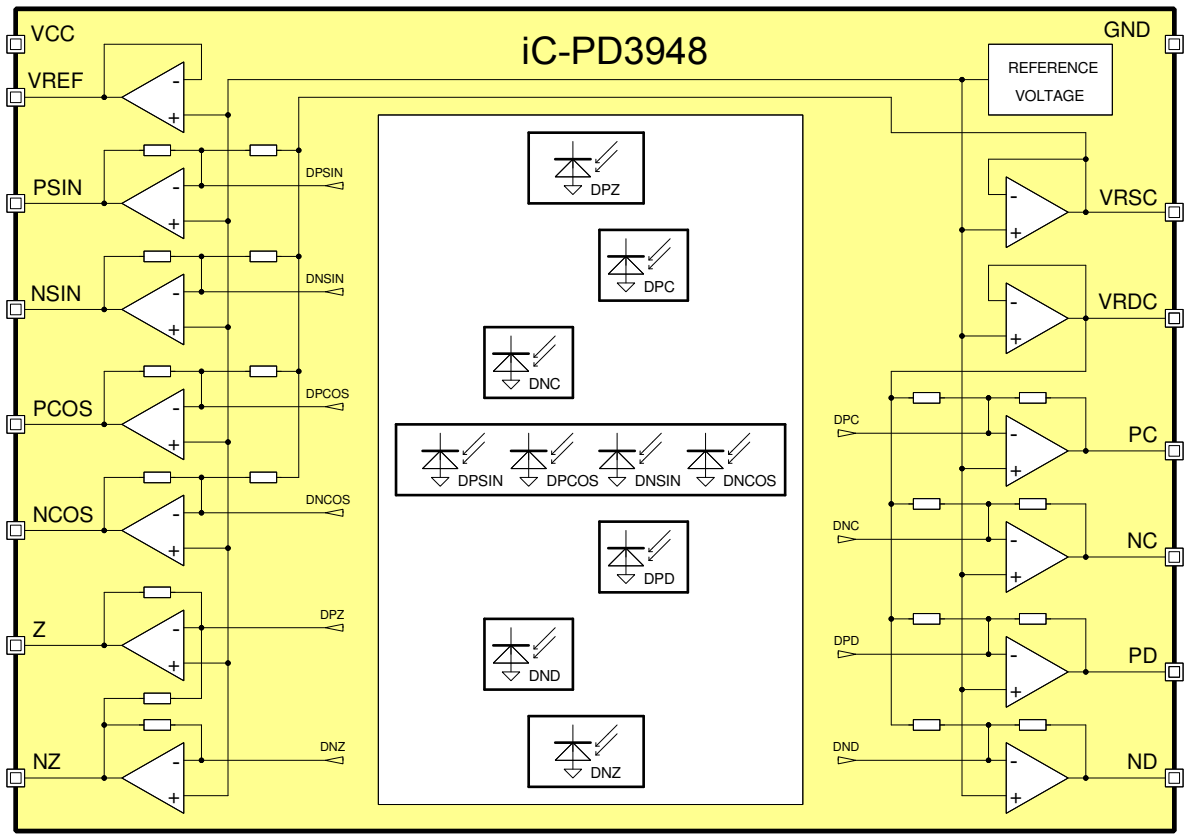


15-pin optoBGA
6.2 mm x 5.2 mm x 1.7 mm



32-pin optoQFN
5 mm x 5 mm x 0.9 mm

BLOCK DIAGRAM



DESCRIPTION

iC-PD3948 is an optical sensor IC with integrated photodiodes whose signal currents are converted into output voltages by low-noise transimpedance amplifiers.

Due to a high transimpedance gain of typically 4 MΩ (*1 MΩ/2 MΩ), output signal voltages of several hundred millivolts are obtained at illumination levels of just 1 to 3 mW/cm^2 (*6 to 18 mW/cm^2). In most cases complicated noise suppression measures are thus rendered unnecessary.

As the pin names would suggest, iC-PD3948 is typically applied as a sine encoder for motor feedback systems. To this end, iC-PD3948 provides sine and cosine signals with both a high resolution of 2048 CPR (plus an additional index signal) and a low resolution of 1 CPR (at C/D).

All code disc signal tracks are evaluated differential; the high resolution sine signals are read by photodiodes in a phased array. The layout of the signal amplifiers is such that there is good paired channel matching, reducing the time and effort required for calibration to an absolute minimum.

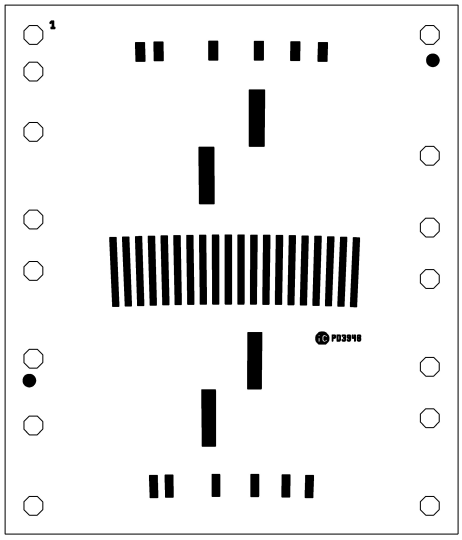
The spectral sensitivity ranges from visible to near infrared light, with the maximum sensitivity close to a wavelength of 680 nm. An output voltage of 1 V is typical in low light conditions, for instance when iC-PD is illuminated at only 2 mW/cm^2 (*12 mW/cm^2) by a 740 nm LED. A relatively low LED current is enough to operate the sensor, proving beneficial to the life expectancy of the LED at high operating temperatures.

HD Phased Arrays are designed for fidelity and robustness. Ultra-low signal distortion is obtained at increased tolerances for alignment and random code defects (e.g. due to dust).
For information on chip releases, refer to chapter Design Review.

*) Data refers to chip release iC-PD3948 Y.

PACKAGING INFORMATION

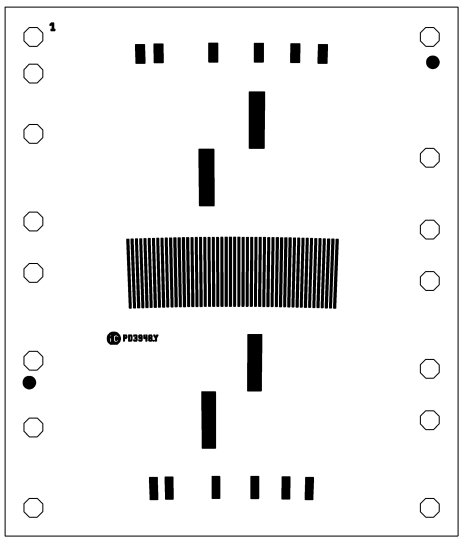
PAD LAYOUT
Chip release . (2.88 mm x 3.37 mm)



PAD FUNCTIONS

No.	Name	Function
		Refer to the description of pin functions.

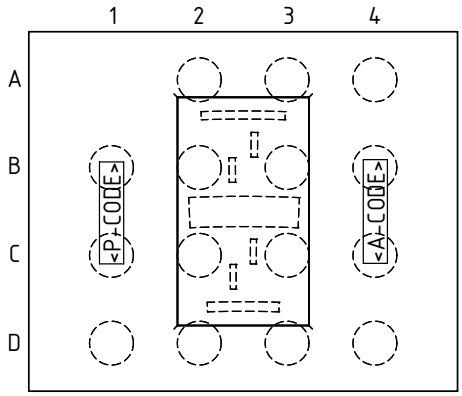
PAD LAYOUT
Chip release Y, Y1 (2.88 mm x 3.37 mm),
HD Phased Array



PAD FUNCTIONS

No.	Name	Function
		Refer to the description of pin functions.

PIN CONFIGURATION
oBGA LSH2C (6.2 mm x 5.2 mm)



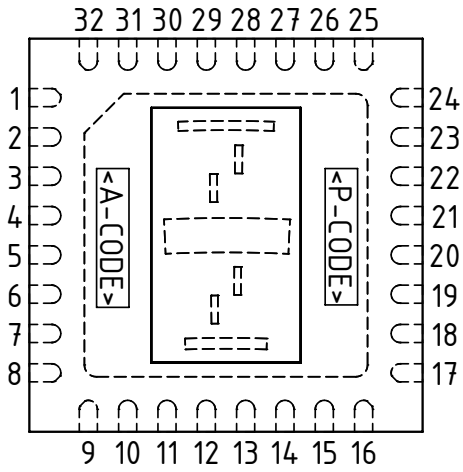
PIN FUNCTIONS

No.	Name	Function
A2	VCC	+4.5...5.5 V Supply Voltage
A3	VREF	Reference Voltage Output
A4	GND	Ground
B1	PSIN	Sine Track +
B2	NSIN	Sine Track -
B3	VRDC	D/C Track Reference
B4	VRSC	S/C Track Reference
C1	PCOS	Cosine Track +
C2	NCOS	Cosine Track -
C3	NC	C Track -
C4	PC	C Track +
D1	Z	Z Index Signal
D2	NZ	Z Index Track -
D3	ND	D Track -
D4	PD	D Track +

Note: All signal and reference outputs are analog voltage outputs.

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
For dimensional specifications refer to the relevant package data sheet, available separately.

PIN CONFIGURATION
oQFN32-5x5 (5 mm x 5 mm)



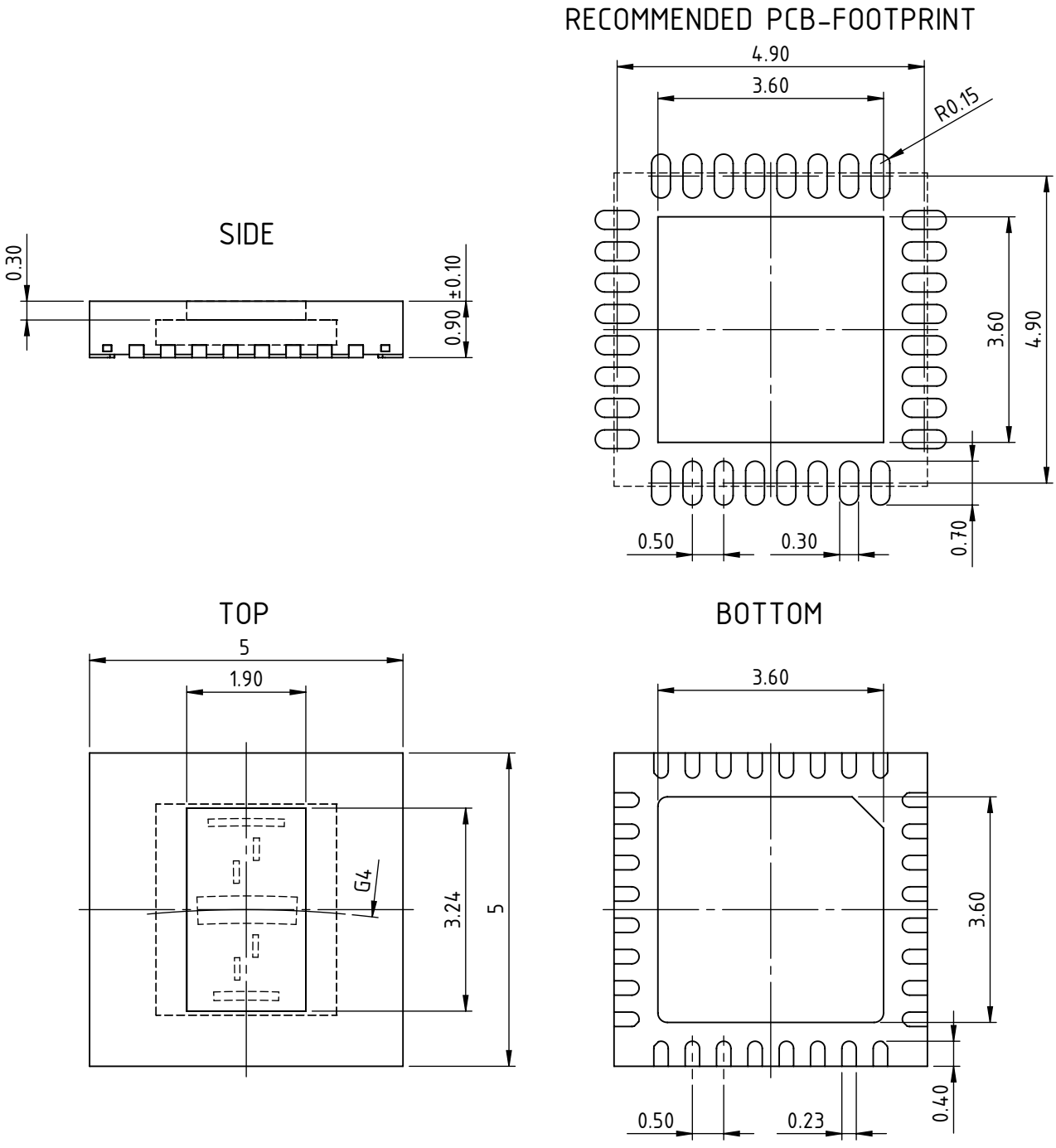
PIN FUNCTIONS

No.	Name	Function
1	VCC	+4.5...5.5 V Supply Voltage
2	VREF	Reference Voltage Output
3	PSIN	Sine Track +
4	NSIN	Sine Track -
5	PCOS	Cosine Track +
6	NCOS	Cosine Track -
7	Z	Z Index Signal
8	NZ	Z Index Track -
9..16	n.c.[1]	
17	ND	D Track -
18	PD	D Track +
19	NC	C Track -
20	PC	C Track +
21	VRDC	D/C Track Reference
22	VRSC	S/C Track Reference
23	n.c.[1]	
24	GND	Ground
25..32	n.c.[1]	
	BP	Backside paddle[2]

Note: All signal and reference outputs are analog voltage outputs.

IC top marking: <P-CODE> = product code, <A-CODE> = assembly (subject to changes);
1) Pin numbers marked n.c. are not connected.
2) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±70µm / ±1° (with respect to center of backside pad).
G4: radius of chip center (refer to the relevant encoder disc and code description).
Maximum molding excess +20µm / -75µm versus surface of glass/reticle.

drb_pdxx-oqfn32-2_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		-0.3	6	V
G002	I(VCC)	Current in VCC		-20	20	mA
G003	V()	Pin Voltage, all signal outputs		-0.3	VCC + 0.3	V
G004	I()	Pin Current, all signal outputs		-20	20	mA
G005	Vd()	ESD Susceptibility, all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G006	Tj	Junction Temperature		-40	150	°C
G007	Ts	Chip Storage Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VCC = 4.5...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package oBGA LSH2C package oQFN32-5x5 (extended temperature range of -40 to 125 °C available on request)	-40 -40		110 110	°C °C
T02	Ts	Storage Temperature Range	package oBGA LSH2C, package oQFN32-5x5	-40		110	°C
T03	Tpk	Soldering Peak Temperature	package oBGA LSH2C tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering TOL (time on label) 8 h; Please refer to customer information file No. 7 for details.			 245 230	 °C °C
T04	Tpk	Soldering Peak Temperature	package oQFN32-5x5 tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering MSL 5 A (max. floor live 24 h at 30 °C and 60 % RH); Please refer to customer information file No. 7 for details.			 245 230	 °C °C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.5...5.5 V, Tj = -40..125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VCC	Permissible Supply Voltage		4.5		5.5	V
002	I(VCC)	Supply Current	no load, photocurrents within op. range		12	16	mA
003	Vc()hi	Clamp-Voltage hi at all pins	I() = 4 mA			11	V
004	Vc()lo	Clamp-Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
Photosensors							
101	λar	Spectral Application Range	Se(λar) = 0.25 x S(λpk)	400		950	nm
102	λpk	Peak Sensitivity Wavelength			680		nm
103	Aph()	Radiant Sensitive Area	chip release iC-PD3948. S/C track (DPSIN, DNSIN, DPCOS, DNCOS) C/D track (DPC, DNC, DPD, DND) Z track (DPZ, DNZ) chip release iC-PD3948 Y S/C track (DPSIN, DNSIN, DPCOS, DNCOS) C/D track (DPC, DNC, DPD, DND) Z track (DPZ, DNZ)		 0.075 0.033 0.042 0.076 0.031 0.039		 mm^2 mm^2 mm^2 mm^2 mm^2 mm^2
104	S(λ)	Spectral Sensitivity	λ_{LED} = 740 nm λ_{LED} = 850 nm		0.5 0.3		A/W A/W
106	E()mx	Irradiance For Maximum Signal Level	λ_{LED} = 740 nm, Vout() not saturated; chip release iC-PD3948. S/C track C/D track Z track chip release iC-PD3948 Y S/C track C/D track Z track	 1.2 2.4 1.9 6.0 8.0 12	 2.0 4.0 3.0 12 15 21	 3.2 6.4 4.8 18 24 36	 mW/cm^2 mW/cm^2 mW/cm^2 mW/cm^2 mW/cm^2 mW/cm^2
Photocurrent Amplifiers							
201	Iph()	Permissible Photocurrent Operating Range	chip release iC-PD3948., all tracks chip release iC-PD3948 Y S/C track and Z track C/D track	0 0 0		280 1120 560	nA nA nA
202	η()r	Photo Sensitivity (light-to-voltage conversion ratio)	λ_{LED} = 740 nm; chip release iC-PD3948., all tracks chip release iC-PD3948 Y S/C track, Z track C/D track	0.8 0.1 0.2	1.2 0.16 0.32	2.0 0.3 0.6	V/µW V/µW V/µW
203	Z()	Equivalent Transimpedance Gain	Z = Vout() / Iph(); chip release iC-PD3948., all tracks chip release iC-PD3948 Y S/C track, Z track C/D track	2.69 0.67 1.34	4.0 1.0 2.0	5.46 1.36 2.72	MΩ MΩ MΩ
204	TCz	Temperature Coefficient of Transimpedance Gain			-0.12		%/°C
209	ΔZ()pn	Transimpedance Gain Matching Of Paired Amplifiers	P.. channel vs. corresponding N.. channel	-0.2		0.2	%
210	ΔVout()pn	Signal Matching	no illumination, any output to any output	-35		35	mV
211	ΔVout()pn	Signal Matching	no illumination, P vs. N path per diff. channel	-2.5		2.5	mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.5...5.5 V, Tj = -40..125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
212	fc()hi	Cut-off Frequency (-3 dB)	chip release iC-PD3948. chip release iC-PD3948 Y	120 240	180 360	280 560	kHz kHz
213	VNoise()	RMS Output Noise	illuminated to 500 mV signal level above dark level, 500 kHz band width		0.5		mV
Signal Outputs							
301	Vout()mx	Permissible Maximum Output Voltage	illumination to E()mxr, linear gain	2.45	2.72	3.02	V
302	Vout()d	Dark Signal Level	no illumination, load 20 kΩ vs. +2 V;	560	770	1000	mV
303	Vout()acmx	Maximum Signal Level	Vout()acmx = Vout()mx - Vout()d	1.48	1.96	2.35	V
304	Isc()hi	Short-Circuit Current hi	load current to ground	100	420	800	µA
305	Isc()lo	Short-Circuit Current lo	load current to IC	250	480	700	µA
306	Ri()	Internal Output Resistance	f = 1 kHz	70	110	180	Ω
Signal References VRSC, VRDC							
401	Vout()	Reference Voltage		560	770	1000	mV
402	Isc()hi	Short-Circuit Current hi	current to ground	100	420	800	µA
403	Isc()lo	Short-Circuit Current lo	current to IC	250	480	700	µA
404	Ri()	Internal Output Resistance		70	110	180	Ω
Reference Voltages VREF							
501	Vout()	Reference Voltage	I(VREF) = -100 µA...+300 µA	560	770	1000	mV
502	dVout()	Load Balancing	I(VREF) = -100 µA...+300 µA	-10		+10	mV
503	Isc()hi	Short-Circuit Current hi	current to ground; chip release iC-PD3948. chip release iC-PD3948 Y	 200 600	 420 1100	 800 1600	 µA µA
504	Isc()lo	Short-Circuit Current lo	current to IC	0.5	4.5	10	mA

APPLICATION CIRCUITS

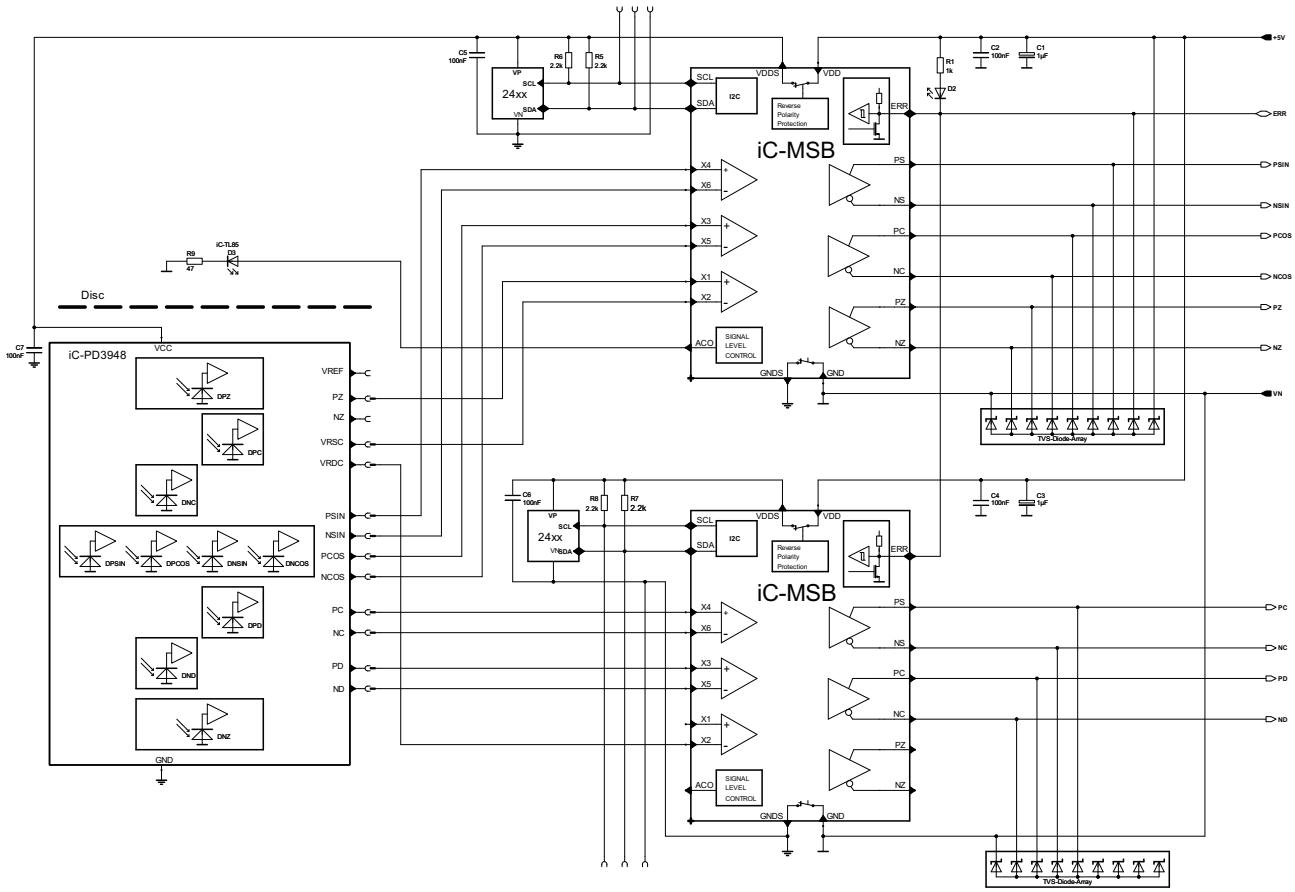


Figure 1: Application example of a motor feedback encoder utilizing two iC-MSB devices.
Sine square plus cosine square LED power controlling by iC-MSB maintains the differential 1 Vpp signal of the S/C channel featuring 2048 CPR. The C/D channel with 1 CPR is initially also calibrated to 1 Vpp differential, but experiences variation due to LED power controlling. This variation can be neglected at speeds below 1,500 rpm, as iC-PD3948 does not run into cut-off frequency.

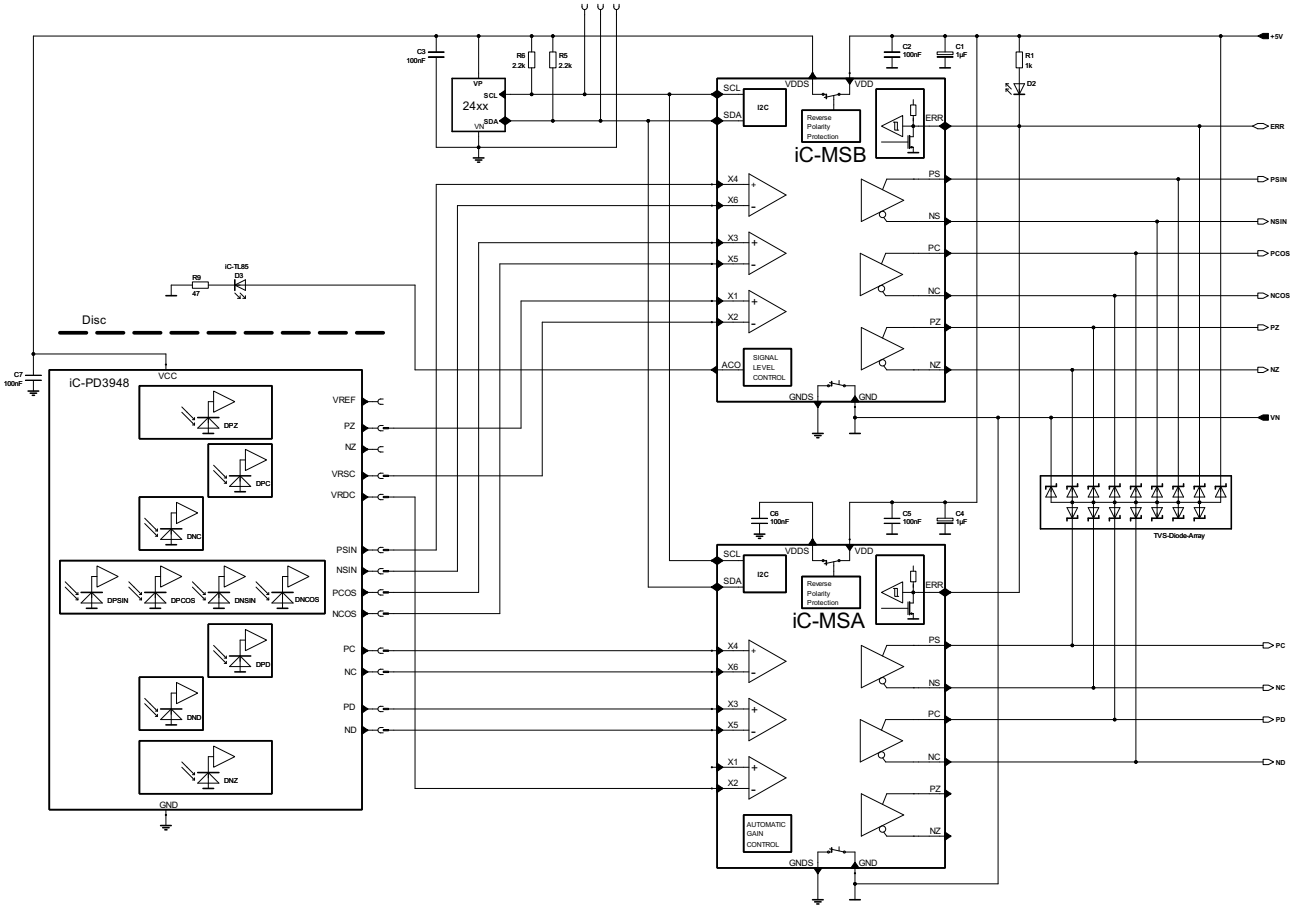


Figure 2: Application example motor feedback encoder utilizing iC-MSB and iC-MSA.
Sine square plus cosine square LED power controlling by iC-MSB maintains the differential 1 Vpp signal of the S/C channel featuring 2048 CPR. The C/D channel with 1 CPR ensures its 1 Vpp differential signal by automatic gain control. In this setup, operation at high rpm speed and beyond iC-MSB's cut-off frequency is possible.

DESIGN REVIEW: Notes On Chip Functions

iC-PD3948.		
No.	Function, Parameter/Code	Description and Application Hints
1		None at time of printing (datasheet release B5, 2011). The current datasheet (C1) introduces minor changes to Elec. Char. which are applicable to iC-PD3948. as well, but not functional relevant to applications. Refer to Revision History for details.
2	IC top marking	Change of optoBGA package marking during 2014: <A-CODE> (assembly code) replaced by <P-CODE> (product code), <D-CODE> (date code) replaced by <A-CODE> (assembly code)

Table 4: Notes on chip functions regarding iC-PD3948 chip release 0.

iC-PD3948 Y, Y1		
No.	Function, Parameter/Code	Description and Application Hints
1	*HD Phased Array*	Chip release utilizes a high density phased array layout.
2	Transimpedance Gain	Improvement of disturbance immunity by lower gain: for S/C and index channel from 4 MΩ to 1 MΩ, for C/D channel from 4 MΩ to 2 MΩ.

Table 5: Notes on chip functions regarding iC-PD3948 chip release Y and Y1.

REVISION HISTORY

Rel	Rel.Date	Chapter	Modification	Page
B5	11-03-14	...		

Rel	Rel.Date	Chapter	Modification	Page
C1	14-07-31	FEATURES	Explanation of CPR and size Change of transimpedance (for chip release iC-PD3948 Y)	2
		DESCRIPTION	Description of *HD Phased Array* supplemented (for chip release iC-PD3948 Y)	2
		PACKAGING INFORMATION	Pad layout supplemented (for chip release iC-PD3948 Y) oQFN and oBGA package drawings updated for top marking oQFN package drawing updated for tolerances	3...5
		THERMAL DATA	Missing operating conditions and extended temperature added	6
		ELECTRICAL CHARACTERISTICS	Item 101, conditions: reference is λpk Item 104: wavelength 850 nm supplemented, item 105 excluded Item 106: adaption of limits (for chip release iC-PD3948.) Items 103, 106, 201, 202, 203, 212: supplements (for chip release iC-PD3948 Y) Items 302, 401, 501, 503: min. limit Items 501, 502: conditions	7, 8
		APPLICATION CIRCUITS	Fig. 1 corrected, description supplemented Fig. 2 replaced, description supplemented (iC-MSA in place of iC-TW3)	9,10
		DESIGN REVIEW	Chapter added	10
		REVISION HISTORY	Chapter added	11

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-PD3948	32-pin optoQFN, 5 mm x 5 mm, thickness 0.9 mm RoHS compliant		iC-PD3948 oQFN32-5x5
	15-pin optoBGA, 6.2 mm x 5.2 mm thickness 1.7 mm RoHS compliant		iC-PD3948 oBGA LSH2C
Evaluation Kit	PCB (60 mm x 40 mm), assembled with optoBGA	with LED and code disc	iC-PD3948 EVAL LSH2M
Code Disc		2048 CPR (S/C) with index, 1 CPR (C/D) absolute, OD ∅ 39 mm, ID ∅ 18.0 mm, optical radius 17.5 mm (glass 1 mm)	PD2S 39-2048

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (0) 61 35 - 92 92 - 0
Fax: +49 (0) 61 35 - 92 92 - 192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

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