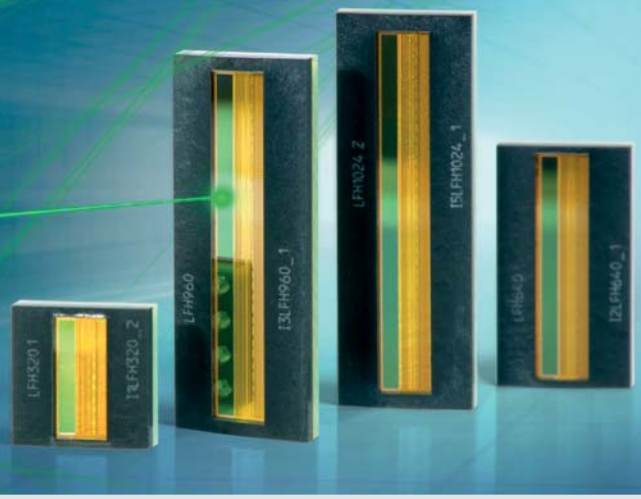
iC-LFH Series
High Resolution Linear Image Sensors



Description

iC-LFH Series are integrating light-to-voltage converters with 1024 / 960 / 640 / 320 pixels pitched at 12.7 µm with high fill factor. Each active pixel consists of a 12.7 µm x 600 µm photodiode, an integration capacitor, and a sample-and-hold circuit.

The on-chip control logic facilitates operation with only a start and clock signal necessary. A third input (ESH) optionally controls the asynchronous, global shutter and allows flexible exposure times.

The new integration and read-out control also keeps the results of aborted integration cycles.
Thus integration can be aborted any time without data loss.
Also a lossless re-read is available.

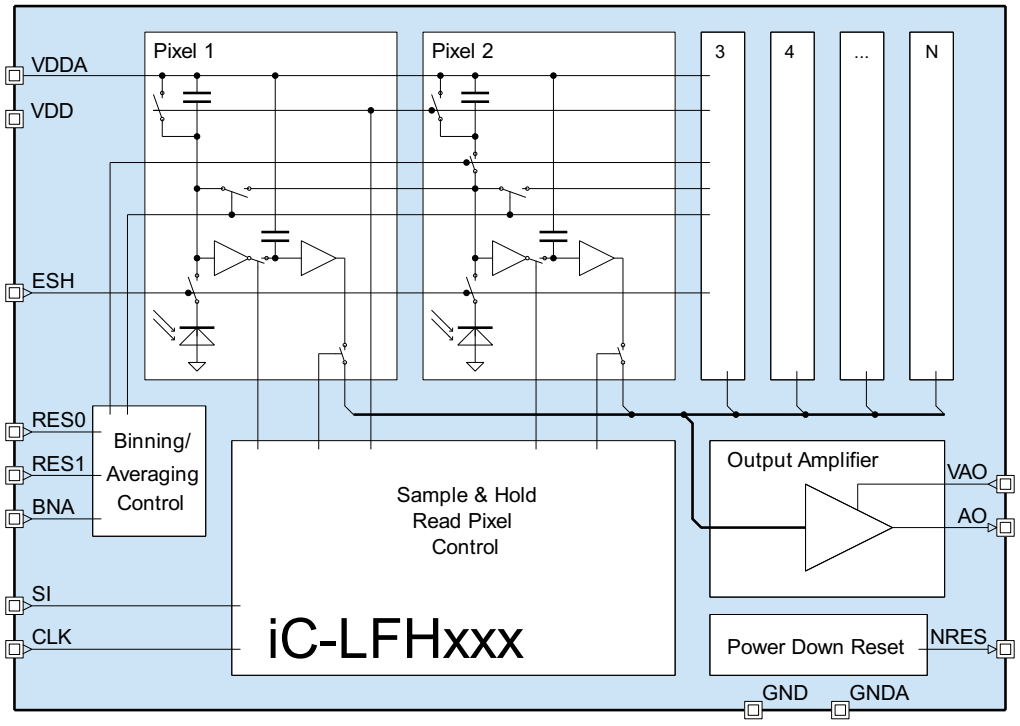
Features

- 1024 / 960 / 640 / 320 active photo pixels with 12.7 µm x 600 µm (2000 DPI)
- Pin-selectable resolution of 2000, 1000, 500 and 250 DPI (binning or averaging selectable)
- High sensitivity and uniformity over wavelength
- High pixel clock rate of up to 5 MHz
- Continuous sample and read mode
- Asynchronous, global shutter enables flexible integration times
- 3 V capable analog output with separate supply pin
- Glitch-free push-pull analog output

Applications

- Triangulation sensors
- Contact image sensors
- Spectroscopy sensors
- CCD replacement

Block Diagram



iC-LFH Series
High Resolution CMOS Linear Image Sensors

Key Specifications

General		
Supply Voltage	VDD, VDDA: 4.5 V ... 5.5 V	
Supply Current in VDD	300 µA @ f(CLK) = 1 MHz	
Supply Current in VDDA	N = 320:	11 ... 15 mA
	N = 640:	20 ... 25 mA
	N = 960:	26 ... 30 mA
	N = 1024:	28 ... 32 mA

Photodiode Array		
Radiant Sensitive Area	600 µm x 12.70 µm, per Pixel	
Spectral Sensitivity	S(λ)max = 0.35 A/W @ λ= 775 nm	
Spectral Application Range	S(λar) = 0.25 x S(λ)max:	420 ... 980 nm

Analog Output AO, VAO		
Sensitivity	RES1/0 = 00, λ = 775 nm	
	V(VAO) = 3.3 V:	1.7 V / pWs
	V(VAO) = 5.0 V:	2.8 V / pWs
Sensitivity Ratio	K (Binning x 2) / K:	1.87
	K (Binning x 4) / K:	3.27
	K (Binning x 8) / K:	5.14
Settling Time	CLK lo to hi until	
	V(AO) = 0.95 x V(AO)max:	200 ns
Pixel Response Nonuniformity	V(AO) = 2.5 V:	±15 % max
Integral Nonlinearity		±1.5 %
Output Noise Voltage	1.5 mV_{RMS} @ V(AO) = 2.5 V	
Dynamic Range	V(VAO) = 5.0 V:	70 dB
	V(VAO) = 3.3 V:	66 dB
Permissible Clock Frequency	Reset integration and digital control:	10 MHz
	Read Pixel and S&H;	
	N = 320:	0.03 ... 5 MHz
	N = 640:	0.06 ... 5 MHz
	N = 960, 1024:	0.1 ... 5 MHz

Package Overview

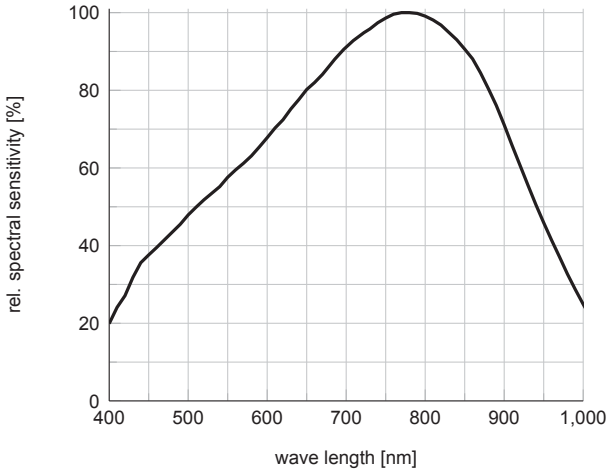
oBGA LFH1C

oBGA LFH2C

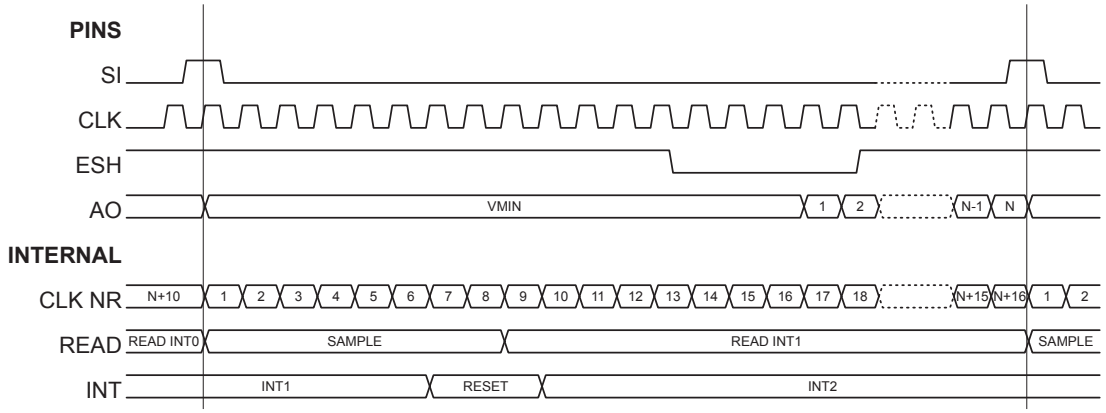
oBGA LFH3C

oBGA LFH5C

Optical Characteristics



Integration and Readout Cycle



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