iC-MFL / iC-MFLT

8-/12-FOLD FAIL-SAFE LOGIC N-FET DRIVER

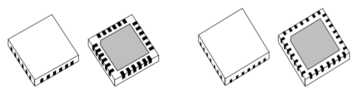
FEATURES

- 8-/12-fold level shift to 5 V output voltage
- Safe low output state with single errors
- Schmitt trigger inputs with two-stage pull-down current for enhanced noise immunity with limited power dissipation
- Inputs compatible with TTL and CMOS levels (1.8 V to 3.3 V to 5 V)
- Current-limited and short-circuit-proof push-pull output stages
- Push-pull current sources for driving FETs
- Surge voltage-proof outputs up to 18 V
- Ground and supply voltage monitor
- Protective ESD circuitry
- Temperature range from -40 to 125 °C

APPLICATIONS

- Operation of 5 V logic level N-FETs from 3.3 V systems

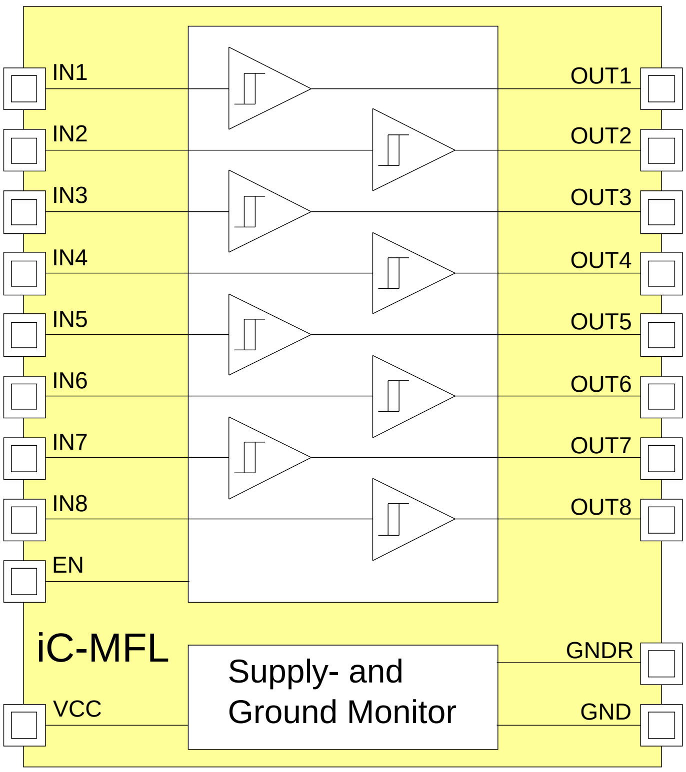
PACKAGES



QFN24 (iC-MFL)

QFN28 (iC-MFLT)

BLOCK DIAGRAM



DESCRIPTION

iC-MFL / iC-MFLT is a monolithically integrated, 8/12-channel level adjustment device which drives N-channel FETs. The internal circuit blocks have been designed in such a way that with single errors, such as open pins (VCC, GND, GNDR) or the short-circuiting of two outputs, iC-MFL's output stages switch to a predefined, safe low state. Externally connected N-channel FET are thus shut down safely in the event of a single error.

The inputs of the eight/twelve channels consist of a Schmitt trigger with a pull-down current source and are compatible with TTL and CMOS levels (1.8 to 5 V). The eight/twelve channels have a current-limited push-pull output stage and a pull-down resistor at the output. The output stages supply an output signal of 5 V and are enabled by a high signal at pin EN. Furthermore, all stages can handle surge voltage pulses (max. 18 V, pulse width < 100 ms, max. 2 % duty cycle) at the output.

iC-MFL monitors the supply voltage at VCC pin and the voltages at the two ground pins GND and GNDR. The pins GND and GNDR must be connected together externally in order to guarantee the safe low state of the output stages in the event of error.

Should the supply voltage at VCC undershoot a predefined threshold, the voltage monitor causes the outputs to be actively tied to GND via the lowside transistors. If the supply voltage ceases to be applied to VCC, the outputs are tied to GNDR by pull-down resistors.

If the connection between the ground potential and the GND pin is disrupted, the highside and lowside transistors of the output stages are shut down and the outputs tied to GNDR via the pull-down resistors. If on the other hand the connection between ground potential and the GNDR pin is disrupted, only the output stage highside transistors are shut down; the outputs are then actively tied to GND via the lowside transistors.

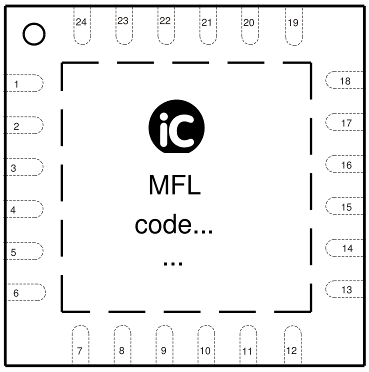
Open inputs IN1...8/12 and EN are actively tied to GND by pull-down currents. The pull-down currents have two stages in order to limit power dissipation with enhanced noise immunity.

When two outputs of different logic states are short circuited, the driving capability of the lowside driver predominates, keeping the connected N-channel FETs in a safe shutdown state.

The device is protected against destruction by ESD.

PACKAGES

PIN CONFIGURATION QFN24
4 mm x 4 mm to JEDEC MO220

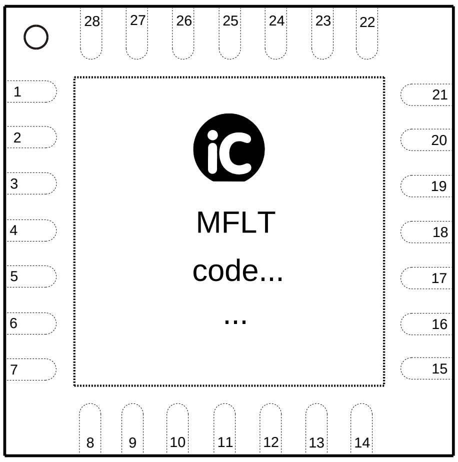


PIN FUNCTIONS

No.	Name	Function
1	OUT1	5 V Output channel 1
2	-	(n.c.)
3	-	(n.c.)
4	GNDR	Ground (Resistor)
5	VCC	5 V Supply Voltage
6	IN1	Input channel 1
7	IN2	Input channel 2
8	IN3	Input channel 3
9	IN4	Input channel 4
10	IN5	Input channel 5
11	IN6	Input channel 6
12	IN7	Input channel 7
13	IN8	Input channel 8
14	-	(n.c.)
15	EN	Enable Input
16	-	(n.c.)
17	GND	Ground
18	OUT8	5 V Output channel 8
19	OUT7	5 V Output channel 7
20	OUT6	5 V Output channel 6
21	OUT5	5 V Output channel 5
22	OUT4	5 V Output channel 4
23	OUT3	5 V Output channel 3
24	OUT2	5 V Output channel 2
	TP	Thermal-Pad

The *Thermal Pad* is to be connected to a ground plane on the PCB. Connections between GND, GNDR and the ground plane should be conciled to system FMEA aspects.

PIN CONFIGURATION QFN28
5 mm x 5 mm to JEDEC MO220



PIN FUNCTIONS

No.	Name	Function
1	OUT2	5 V Output channel 2
2	OUT1	5 V Output channel 1
3	GNDR	Ground (Resistor)
4	VCC	5 V Supply Voltage
5	IN1	Input channel 1
6	IN2	Input channel 2
7	IN3	Input channel 3
8	IN4	Input channel 4
9	IN5	Input channel 5
10	IN6	Input channel 6
11	IN7	Input channel 7
12	IN8	Input channel 8
13	IN9	Input channel 9
14	IN10	Input channel 10
15	IN11	Input channel 11
16	IN12	Input channel 12
17	EN	Enable Input
18	GND	Ground
19	OUT12	5 V Output channel 12
20	OUT11	5 V Output channel 11
21	OUT10	5 V Output channel 10
22	OUT9	5 V Output channel 9
23	OUT8	5 V Output channel 8
24	OUT7	5 V Output channel 7
25	OUT6	5 V Output channel 6
26	OUT5	5 V Output channel 5
27	OUT4	5 V Output channel 4
28	OUT3	5 V Output channel 3
	TP	Thermal-Pad

The *Thermal Pad* is to be connected to a ground plane on the PCB. Connections between GND, GNDR and the ground plane should be conciled to system FMEA aspects.

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Supply Voltage		-0.3	6	V
G002	V()	Voltage at OUT1...8/12		-0.3	6	V
G003	Vp()	Peak Voltage at OUT1...8/12	t < 100 ms, duty cycle < 2 %	-0.3	18	V
G004	V()	Voltage at IN1...8/12, EN		-0.3	6	V
G005	V(GNDR)	Voltage at GNDR referenced to GND		-0.3	0.3	V
G006	V(GND)	Voltage at GND referenced to GNDR		-0.3	0.3	V
G007	Imx()	Current in OUT1...8/12, IN1...8/12, EN		-10	10	mA
G008	Imx()	Current in OUT1...8/12	t < 100 ms, duty cycle < 2 %	-10	120	mA
G009	Imx()	Current in VCC, GND		-50	50	mA
G010	Imx()	Current in GND, GNDR	t < 100 ms, duty cycle < 2 %	-100	10	mA
G011	Vd()	ESD susceptibility	HBM 100 pF discharged through 1.5 kΩ		2	kV
G012	Tj	Operating Junction Temperature		-40	150	°C
G013	Ts	Storage Temperature Range		-55	125	°C

THERMAL DATA

Operating Conditions: VCC = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip/Ambient	SMD assembly, no additional cooling areas.			75	K/W

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 5 V ±10 %, Tj = -40...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VCC	Permissible Supply Voltage				4.5	5	5.5	V
002	I(VCC)	Supply Current in VCC	(No load) iC-MFL iC-MFLT			 1.5		 7 10	 mA mA
003	I(VCC)	Error Current in VCC	VCC = 5 V, one output at 18 V			-50			mA
004	I(GND)	Current in GND	(No load) iC-MFL iC-MFLT			 -6 -9			 mA mA
005	I(GNDR)	Current in GNDR	(No load, all OUTx = hi) iC-MFL iC-MFLT			 -4 -6		 -0.3	 mA mA
Current Driver OUT1...8/12									
101	I(OUTx)	Current in I(OUTx)	V() = 18 V VCC = 5 V			20		100	mA
102	U(OUTx)	permitted voltage	T < 100 ms, duty cycle < 2 %					18	V
103	Vc()lo	Clamp Voltage lo referenced to the lower voltage of GND, GNDR	I() = -10 mA			-3		-0.4	V
104	Vs()hi	Saturation Voltage hi referenced to VCC	Vs()hi = VCC – V(); I() = -0.5 mA I() = -2 mA					 0.2 0.8	 V V
105	Vs()lo	Saturation Voltage lo referenced to GND	I() = 0.5 mA I() = 2 mA					0.2 0.8	V V
106	Rpd()	Pull-Down Resistor at OUTx referenced to GNDR	V(GND) > Vtr(GND)			12	30	70	kΩ
107	Isc()lo	Short circuit current lo	V() = 0.8 V...VCC			2	3.6	6	mA
108	Isc()hi	Short circuit current hi	V() = 0...VCC – 0.8 V			-6	-3	-2	mA
109	Vsh()	Output Voltage at short circuit of two outputs	At two different input signals hi and lo					1.1	V
Input IN1...8/12, EN									
201	Vc()hi	Clamp Voltage hi	I() = 10 mA			6			V
202	Vc()lo	Clamp Voltage lo referenced to the lower voltage of GND, GNDR	I() = -10 mA			-3		-0.4	V
203	Vt()hi	Threshold Voltage hi				1.1		1.4	V
204	Vt()lo	Threshold Voltage lo				0.8		1.1	V
205	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo			200		400	mV
206	Ipd1()	Pull-Down Current 1	0.4 V < V() < Vt()hi		4	150	225	350	µA
207	Ipd2()	Pull-Down Current 2	V() > 1.4 V		4	20	45	70	µA
208	Cin()	Input Capacitance						20	pF
209	Ileak()	Input Leakage Current	VCC = 0 V, V() = 0...5.5 V			-10		10	µA
Supply Monitor									
301	VCCon	Turn-On Threshold VCC				3.7		4.4	V
302	VCCoff	Turn-Off Threshold VCC	Decreasing voltage VCC			3.2		4.1	V
303	VCChys	Hysteresis	VCChys = VCCon – VCCoff			100	200	600	mV
Ground Monitor GND, GNDR									
401	Vtg()hi	Threshold Voltage hi GND Monitor	Referenced to GNDR					270	mV
402	Vtg()lo	Threshold Voltage lo GND Monitor	Referenced to GNDR			50			mV
403	Vtg()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo			5		80	mV
404	Vtr()hi	Threshold Voltage hi GNDR Monitor	Referenced to GND					270	mv
405	Vtr()lo	Threshold Voltage lo GNDR Monitor	Referenced to GND			50			mV

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 5 V ±10 %, Tj = -40...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
406	Vtr()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo			5		80	mV
Timing									
501	tp(OUTx)	Propagation Delay, INx, EN → OUTx	({INx, EN}lo → hi) → 90 % OUTx, ({INx, EN}hi → lo) → 10 % OUTx, no Cl()		1	40		200	ns

ELECTRICAL CHARACTERISTICS: Diagrams

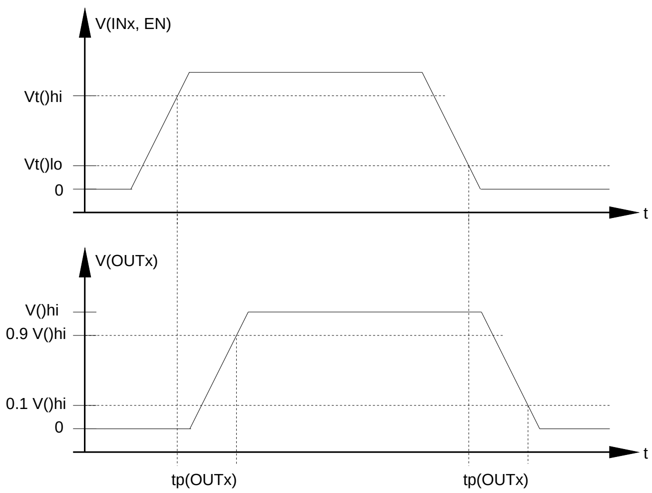


Figure 1: Propagation delays

DESCRIPTION OF FUNCTIONS

Output characteristic of the lowside transistor
The lowside output transistors at the eight/twelve channels demonstrate a resistive behavior with low voltage V(OUTx) and behave as a current sink with finite output resistance with higher voltages.

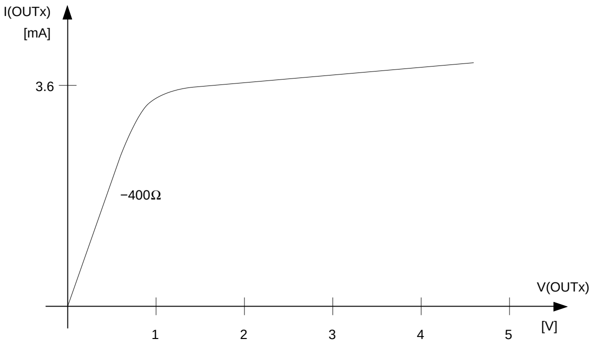


Figure 2: Output characteristic of the lowside transistor at OUTx

Output characteristic for the highside transistor
The highside output transistors at the eight/twelve channels demonstrate a resistive behavior with low voltage (VCC – V(OUTx)) and behave as a current source with finite output resistance with higher voltages.

Pull-down currents
In order to enhance noise immunity with limited power dissipation at inputs INx and EN the pull-down currents at these pins have two stages. With a rise in voltage at input pins INx and EN the pull-down current remains high until Vt()hi (Electrical Characteristics No. 203); above this threshold the device switches to a lower pull-down current. If the voltage falls below Vt()lo (Electrical Characteristics No. 204), the device switches back to a higher pull-down current.

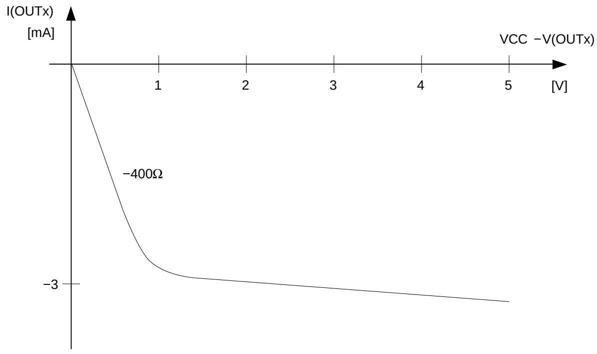


Figure 3: Output characteristic of the highside transistor at OUTx

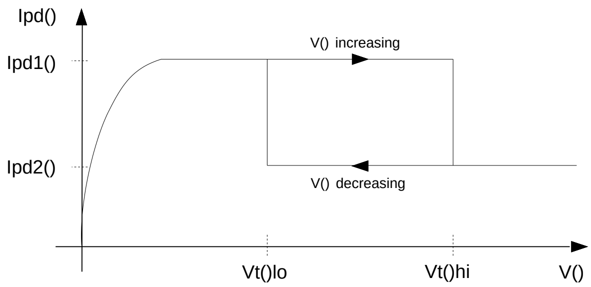


Figure 4: Pull-down currents at INx and EN

DETECTING SINGLE ERRORS

If single errors are detected, safety-relevant applications require externally connected switching transistors to be specifically shut down. Single errors can occur when a pin is open (due to a disconnected bonding wire or a bad solder connection, for example) or when two pins are short-circuited.

When two output of different logic levels are short-circuited, the driving capability of the lowside driver will predominate, keeping the connected N-channel FETs in a safe shutdown state.

With open pins VCC, GND or GNDR iC-MFL switches the output stages to a safe, predefined low state via pull-down resistors or pull-down current sources at the inputs, subsequently shutting down any externally connected N-channel FETs.

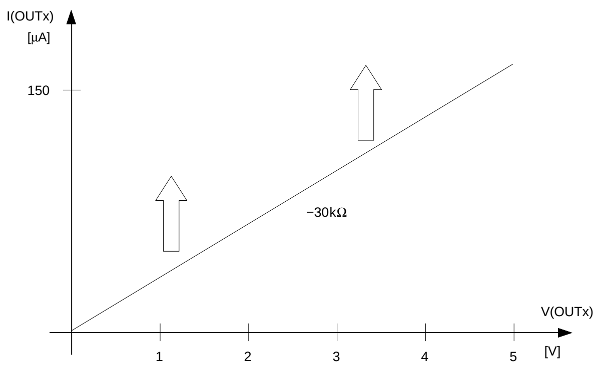


Figure 5: Output characteristic at OUTx with disconnected VCC supply

Loss of VCC potential

If the supply voltage is disconnected from VCC pin, the outputs are tied to GNDR via internal pull-down resistors of typically 30 kΩ which form a passive path from the gate of an external switching transistor to ground. A further increase of output current may occur due to self-supply effects via the output of the iC, as indicated by the arrows in Figure 5.

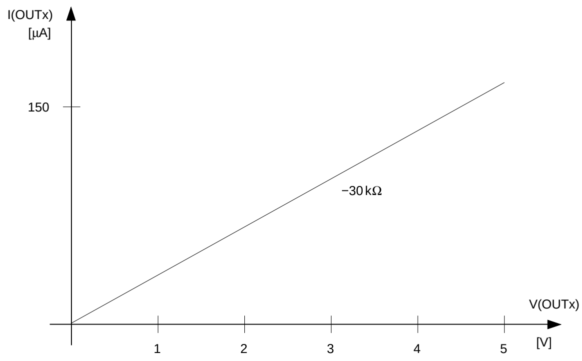


Figure 6: Output characteristic at OUTx with open GND pin

Loss of GND potential

If ground potential is not longer applied to GND, the output stages are shut down and the outputs tied to GNDR via internal pull-down resistors with a typical value of 30 kΩ.

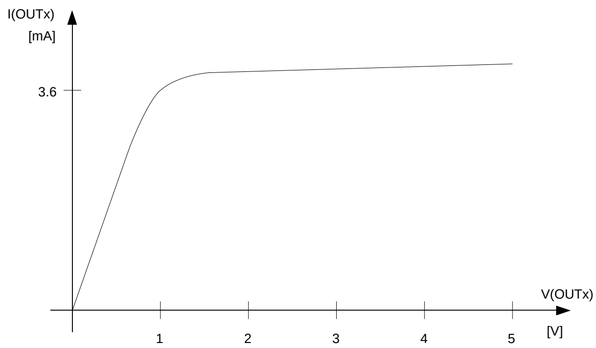


Figure 7: Output characteristic at OUTx with open GNDR pin

Loss of GNDR potential

If ground potential is no longer applied to the GNDR-pin, the output stage highside drivers are shut down and the outputs actively tied to GND via the lowside drivers.

OUTPUT VOLTAGE SURGE PROTECTION

An internal protective circuitry allows for short overvoltage pulses of up to 18 V at the output stages. Puls duration and duty cycle must be less than 100 ms and 2 % respectively for absolute maximum ratings.

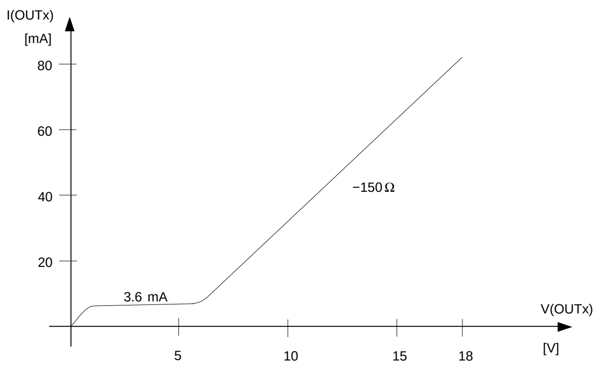


Figure 8: Surge output characteristic at OUTx with Vin = low

The output characteristic in Figure 8 corresponds to that of the lowside driver as shown in Figure 2 for an output voltage V(OUTx) of up to VCC potential. At higher output voltage, the excess current is diverted to ground via the output resistor which has a typical value of 150 Ω.

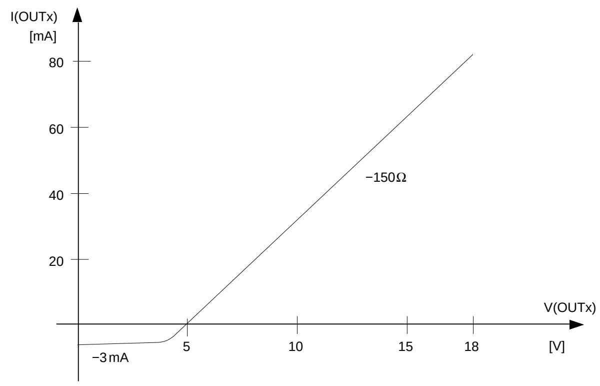


Figure 9: Surge output characteristic at OUTx with Vin = high

The output characteristic in Figure 9 corresponds to that of the highside driver as shown in Figure 3 for an output voltage V(OUTx) of up to VCC potential. At higher output voltage, the excess current is diverted to ground via the output resistor which has a typical value of 150 Ω.

APPLICATION NOTES

Driving an N-channel MOSFET

One typical field of application for iC-MFL is in the operation of 5 V logic level N-FETs with microprocessor output signals of 1.8 to 5 V, as shown in Figure 10.

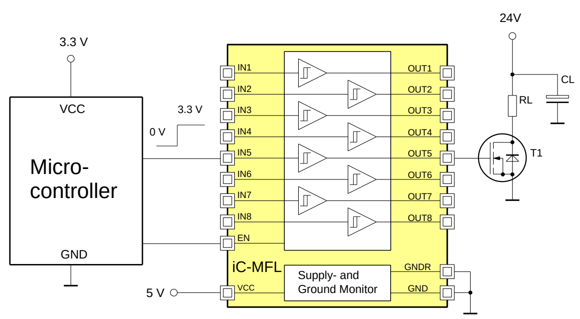


Figure 10: Driving an N-channel MOSFET

ORDERING INFORMATION

Type	Package	Order Designation
iC-MFL	QFN24 QFN24	iC-MFL QFN24 iC-MFLT QFN28

For technical support, information about prices and terms of delivery please contact:

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