iC-OC
INTEGRATING LIGHT-VOLTAGE CONVERTER

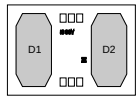
FEATURES

- Two photosensors with integrating amplifiers
- Integration time can be set externally
- Internal shift register for chain connection
- Detection of low supply voltage
- TTL/CMOS-compatible logic inputs and outputs
- 5 V supply voltage
- Low power consumption
- Photosensors with 1 mm pitch;
  active area ca. 0.97 mm x 0.47 mm (0.44 mm²)

APPLICATIONS

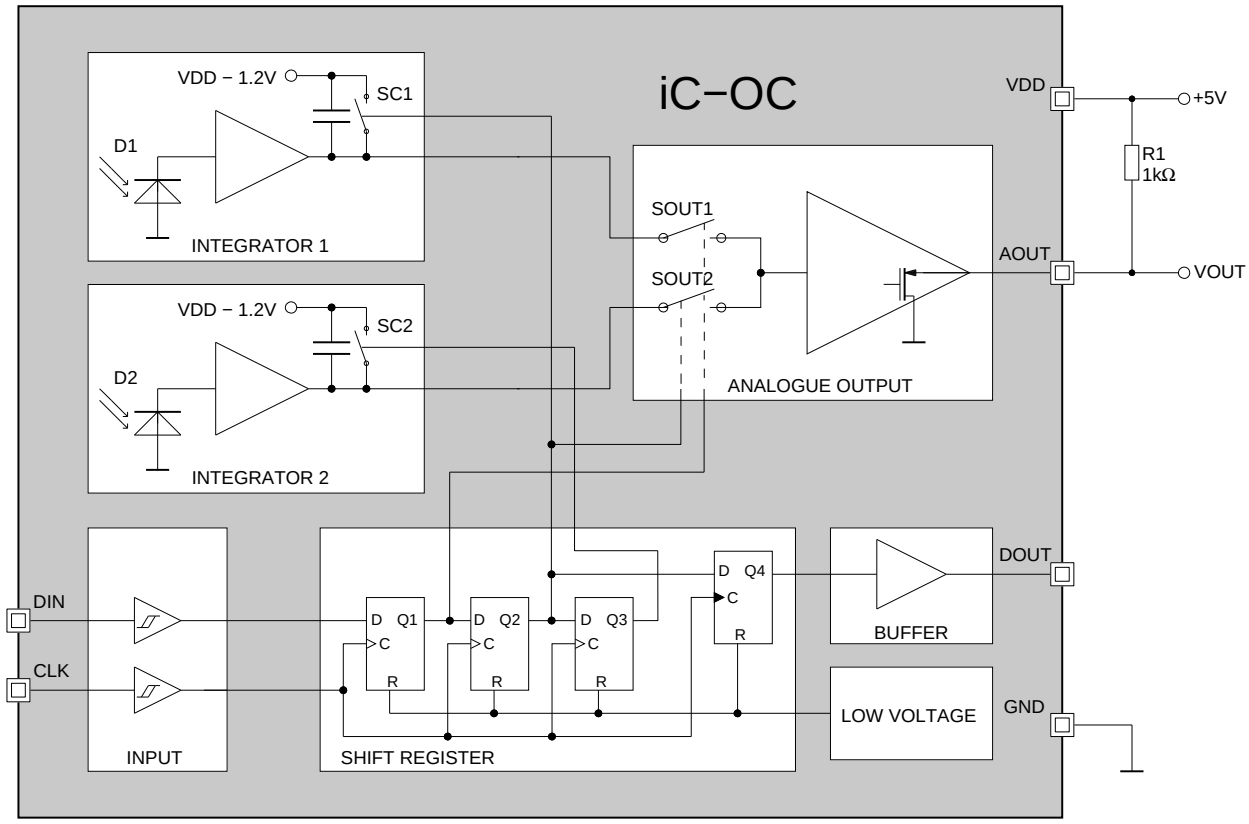
- Optical line sensors
- CCD substitute

CHIP



1.7 mm x 1.2 mm

BLOCK DIAGRAM



DESCRIPTION

iC-OC is an optical sensor with two photodiodes, two integrating amplifiers and a control logic which enables several iC-OCs to be connected in a chain.

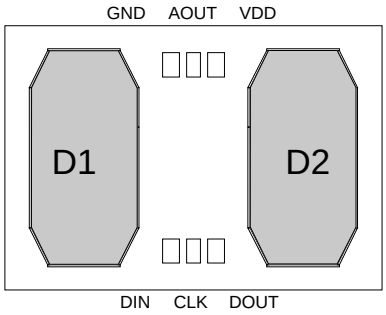
Furthermore, the control logic, consisting of a two-stage shift register, determines when the integration time starts and ends and switches the integrators in sequence to the analogue output. The analogue output is a source follower and in its deactivated state has a high impedance and can thus be used in buses.

The control logic output supplies a CMOS compatible signal and in chain connection it can be directly linked to the digital input of the next device. Logic inputs are configured as Schmitt triggers and are TTL/CMOS-compatible.

All the registers in the device are reset with low voltage (power-down reset). All pins are protected against ESD.

CHIP LAYOUT

PIN CONFIGURATION Chip



PIN FUNCTIONS

No.	Name	Function
	DIN	Input
	CLK	Clock Input
	DOUT	Data Output
	VDD	+5 V Supply Voltage
	AOUT	Analogue Output
	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Supply Voltage		-0.3	6.5	V
G002	Ic()	Clamping Current in DIN, CLK, DOUT, AOUT		-20	20	mA
G003	I()	Current in DOUT		-10	10	mA
G004	Ilu()	Pulse Current in all Pins (Latch-up strength)	Pulse width $\leq$ 10 µs	-100	100	mA
G005	Vd()	ESD Susceptibility, at all Pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G006	Tj	Junction Temperature		-40	150	°C
G007	Ts	Storage Temperature	See package specification			

THERMAL DATA

Operating Conditions: VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	See package specification				

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 5 V ±10 %, RL(VDD/AOUT) = 1 kΩ, Tj = 0...85 °C unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage Range		4.5		5.5	V
002	I(VDD)	Supply Current in VDD		100		700	µA
003	Vc()hi	Clamp Voltage hi at DIN, CLK, DOUT, AOUT	Vc()hi = V() − VDD, I() = 10 mA, other pins open	0.3		1.5	V
004	Vc()lo	Clamp Voltage lo at DIN, CLK, DOUT, AOUT	I() = -10 mA, other pins open	-1.5		-0.3	V
005	Aph()	Radiant Sensitive Area		ca. 0.97 x 0.47			mm²
006	λar	Spectral Application Range	S(λar) = 0.25 x S(λ)max	300		950	nm
Analogue Output AOUT							
201	V0()	Output Voltage at no illuminance	V0() = VDD − V(AOUT)max, AOUT active (* see below)	0.7		1.4	V
202	ΔVd()	Variation of Output Voltage at no illuminance	ΔVd() = V(AOUT)t1 − V(AOUT)t2, Δt = t2 − t1 = 1 ms	-10		10	mV
203	Vs()	Saturation Voltage	Tenfold illuminance VDD = 4.5 V VDD = 5 V VDD = 5.5 V			 1.4 1.45 1.5	 V V V
204	ΔV()	Repeatability (standard deviation at repeated measurement)	20 measurements at constant LED illuminance, Vav(AOUT) ≈ 2.91 V, Δt = 25 µs			15	mV
205	Vlin()	Output Voltage Linearity Range	Vlin() = VDD − V0() − V(AOUT)	1.7			V
206	K	Transfer Factor output voltage vs. light power	BMST assembly incl. sealing; λ_{LED} = 628 nm, Δλ = ±23 nm λ_{LED} = 880 nm, Δλ = ±40 nm	 0.22 0.13	 0.27 0.16	 0.32 0.19	 V/pWS V/pWS
207	Δklin	Transfer Factor Deviation within linearity range		-5		5	%
208	I()	Leakage Current	V(AOUT) = 0...VDD, AOUT high impedance (* see below)	-2		2	µA
Shift-Register DIN, CLK, DOUT							
301	Vt()hi	Threshold Voltage hi at DIN, CLK				2.2	V
302	Vt()lo	Threshold Voltage lo at DIN, CLK		0.8			V
303	Vt()hys	Hysteresis at DIN, CLK	Vt()hys = Vt()hi − Vt()lo	250		1300	mV
304	Ii()	Input Current in DIN, CLK	V() = 0...VDD	-1		1	µA
305	f()	Permissible Frequency at CLK				10	MHz
306	tw()hi	Permis. Pulse Width hi at CLK		20			ns
307	tw()lo	Permis. Pulse Width lo at CLK		20			ns
308	tplh	Propagation Delay: CLK hi → lo until DOUT lo → hi	CL(DOUT) = 50 pF (see Fig. 2)			40	ns
309	tphl	Propagation Delay: CLK hi → lo until DOUT hi → lo	CL(DOUT) = 50 pF (see Fig. 2)			40	ns
310	tpon	Propagation Delay: CLK lo → hi until AOUT active	CL(VDD/AOUT) = 1 nF (see Fig. 2)			800	ns
311	tpoff	Propagation Delay: CLK lo → hi until AOUT high impedance	CL(VDD/AOUT) = 1 nF (see Fig. 2)			100	ns
312	Vs()hi	Saturation Voltage hi at DOUT	Vs()hi = VDD − V(), I() = -1 mA			0.4	V
313	Vs()lo	Saturation Voltage lo at DOUT	I() = 1 mA			0.4	V
Low Voltage Detection							
401	VDDon	Turn-on Threshold VDD	Increasing voltage at VDD	2.1		3.8	V
402	VDDoff	Undervoltage Threshold VDD	Decreasing voltage at VDD	1.0		2.1	V
403	VDDhys	Hysteresis	VDDhys = VDDon − VDDoff	0.5		2	V

(*) AOUT active: SOUT1 or SOUT2 closed; AOUT high impedance: SOUT1 and SOUT2 open.

ELECTRICAL CHARACTERISTICS: Diagrams

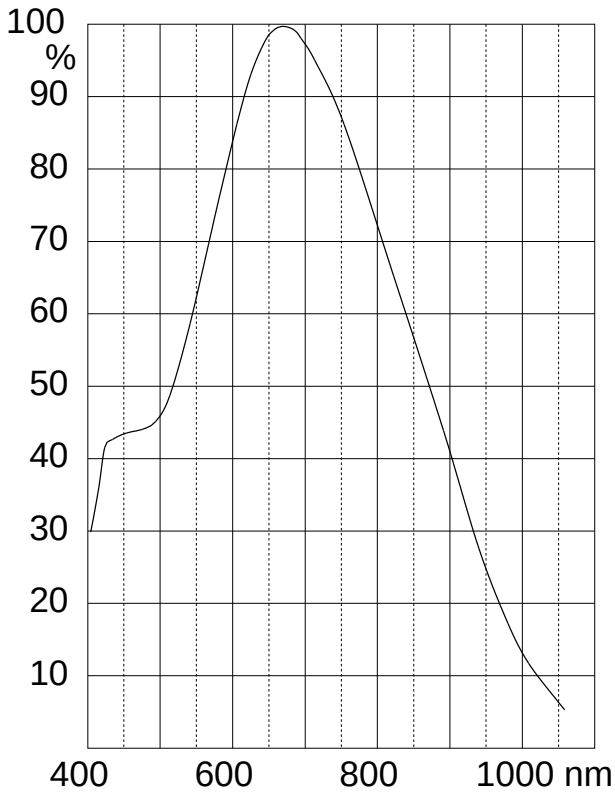


Figure 1: Relative Spectral Sensitivity

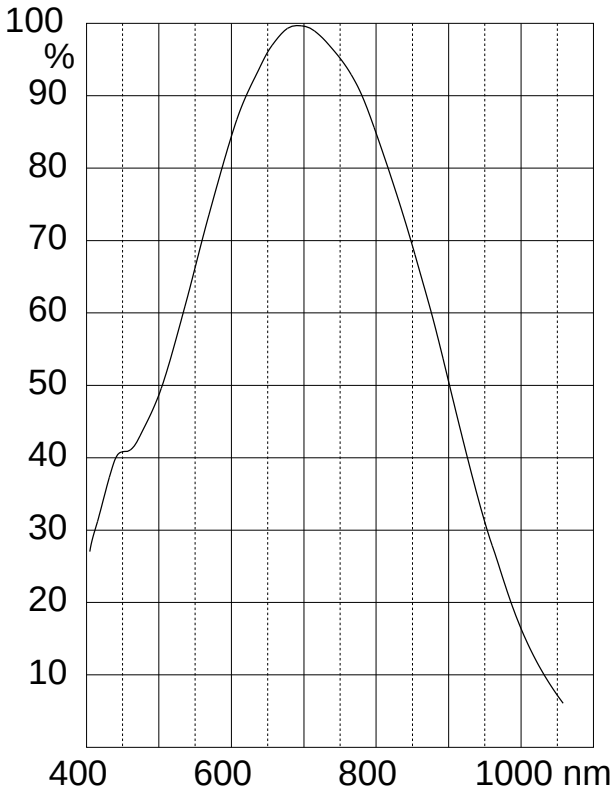


Figure 2: Relative Spectral Sensitivity with BMST assembly

OPERATING REQUIREMENTS: Logic

Operating Conditions: VDD = 5 V ±10 %, Ta = 0...85 °C,
input levels lo = 0...0.45 V, hi = 2.4 V...VDD, see Fig. 3 for reference levels

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I001	tset	Setup time: DIN stable before CLK lo → hi		3	10		ns
I002	thold	Hold time: DIN stable after CLK lo → hi		3	5		ns

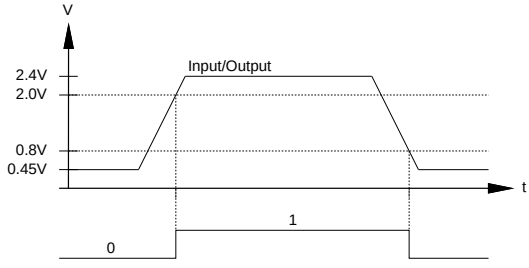


Figure 3: Reference levels

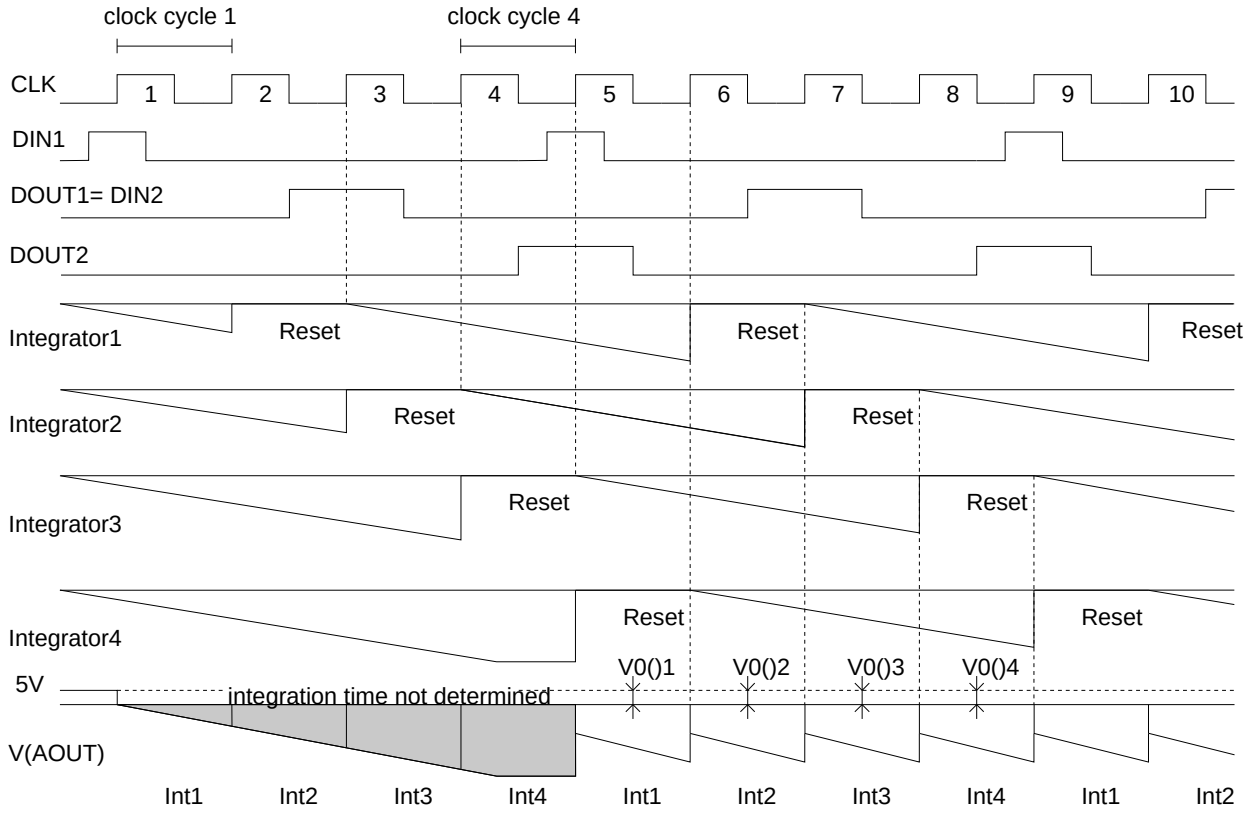


Figure 4: Timing characteristics after power on (assumption: V0()1 = V0()2 = V0(), VDD = 5 V)

DESCRIPTION OF FUNCTIONS

iC-OC is an integrating light-voltage converter with two separate photodiodes and two integrators. The integration time starts when the supply voltage is applied. To obtain a specified integration time a hi pulse must first be available at the digital input DIN and clocked by the device. This process sequentially resets the integrators to their initial value and restarts the integration time with the next clock pulse.

Flip-flops Q1 to Q3 sequentially accept the signal at DIN with the positive CLK edge. Flip-flop Q4, which controls the DOUT output signal, reacts to the negative CLK edge. The switching states in the IC always remain for the duration of a clock cycle. The process depicted in Fig. 2 is initiated when a hi pulse is applied to DIN.

During the first clock cycle integrator 1 is switched to the analogue output AOUT (switch SOUT1 closes). AOUT initially supplies a voltage value which cannot be reproduced as the integration time is unknown. The second clock cycle switches the analogue output from integrator 1 to integrator 2 (SOUT1 opens, SOUT2 closes). A non-reproducible voltage value is again present at AOUT (see above). At the same time the integration capacity of integrator 1 is short-circuited by switch SC1 (reset).

Flip-flop Q4 is set in the second clock cycle with the negative clock edge (DOUT1) and thus the DIN signal for the next device in the chain is produced.

During the third clock cycle integrator 2 is disconnected from AOUT (SOUT2 opens) and reset (SC2 closes). Simultaneously, the integration time for integrator 1 starts anew (SC1 opens). If several iC-OCs are connected in a chain, then the hi signal from DOUT is shifted into the first flip-flop of the next device with the third clock cycle. During the fourth clock cycle switch SC2 opens and starts the integration time for integrator 2.

APPLICATIONS INFORMATION

Only when the DOUT2 output has a hi level can the next hi signal be applied to DIN1. The first hi signal clocked by the device implements a sequential reset of the integrators, followed by the integration time starting in sequence. The second hi signal shifted through the register determines the end of the integration time and restarts the integration time after a reset. The integrators can be read out with the aid of a sample and hold circuit, as the device itself has no hold mode. Besides the clock a periodic signal at DIN is also necessary for the continuous operation of the device.

With operation of the device at low level illumination the output voltage V(AOUT) decreases by V0(AOUT). When calibrating, this drop in voltage must be determined for each of the photosensors.

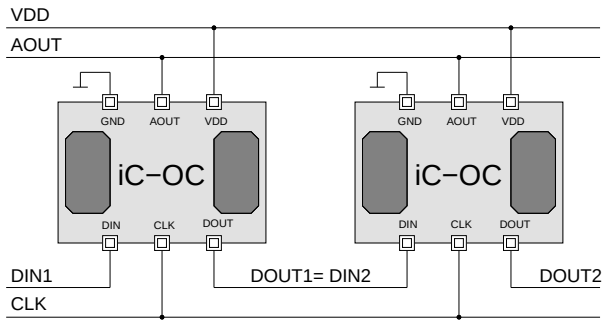


Figure 5: Example of a chain connection for two devices

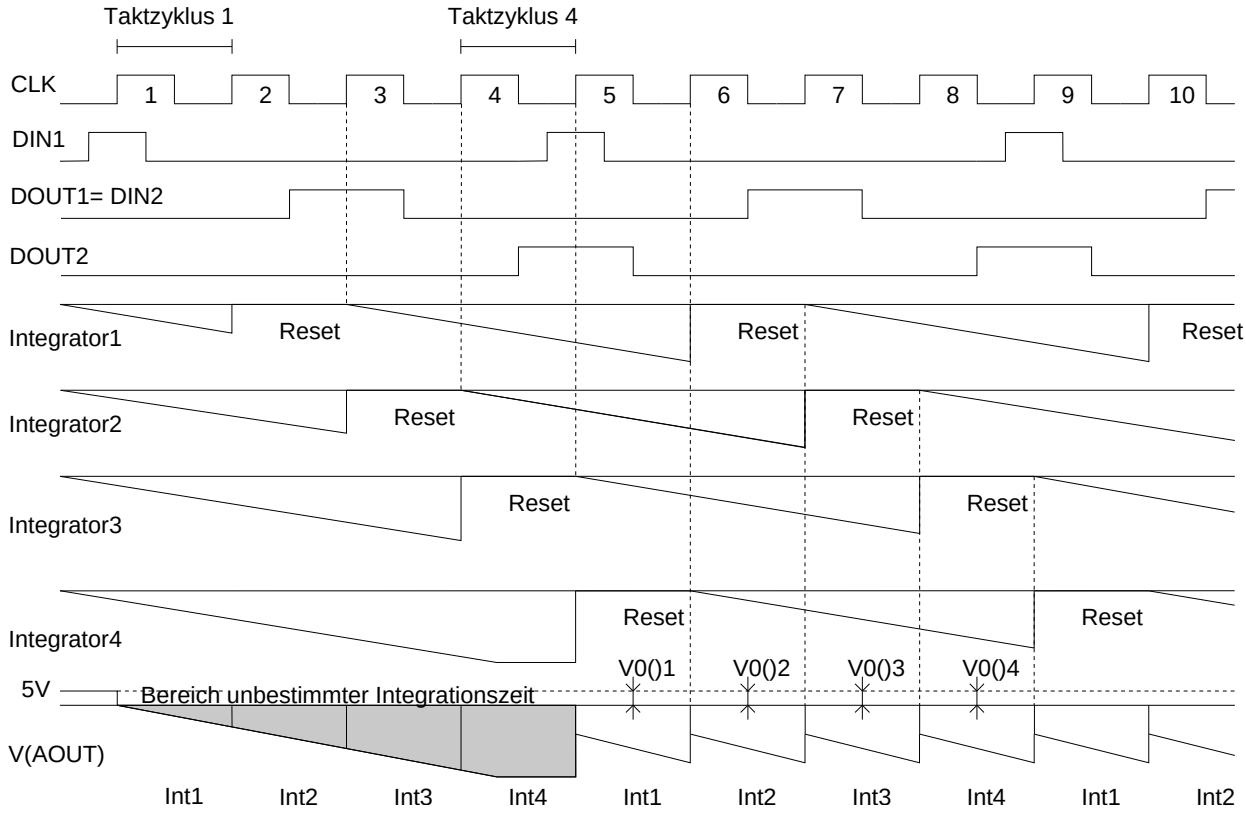


Figure 6: Time sequence for the chain connection in Fig. 5 after the device has been switched on

ORDERING INFORMATION

Type	Package	Order Designation
iC-OC samples	CDIP16	iC-OC CDIP16
iC-OC	-	iC-OC chip

For technical support, information about prices and terms of delivery please contact:

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