iC-JRX

µP INTERFACE WITH 2×4 24V HIGH-SIDE DRIVERS

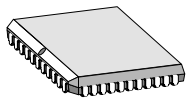
FEATURES

- 2 × 4 bidirectional input/output stages at 24 V
- Input/output mode programmable in 4-bit blocks
- Guaranteed high-side driving capability of 100 mA_{dc} and 500 mA_{peak} for pulse load
- Short-circuit-proof drivers with high dielectric strength
- Low saturation voltage of 0.6 V at 100 mA and 2 V at 500 mA
- Integrated flyback circuits
- PWM function with programmable duty cycle
- Flash mode for the outputs
- Power outputs can be disabled together
- Programmable current sources define logic levels and allow load monitoring
- Digital input filters with externally adjustable filtering times
- Can be bus operated due to the high-speed µP interface
- Programmable interrupt output
- Voltage and two-stage temperature monitoring

APPLICATIONS

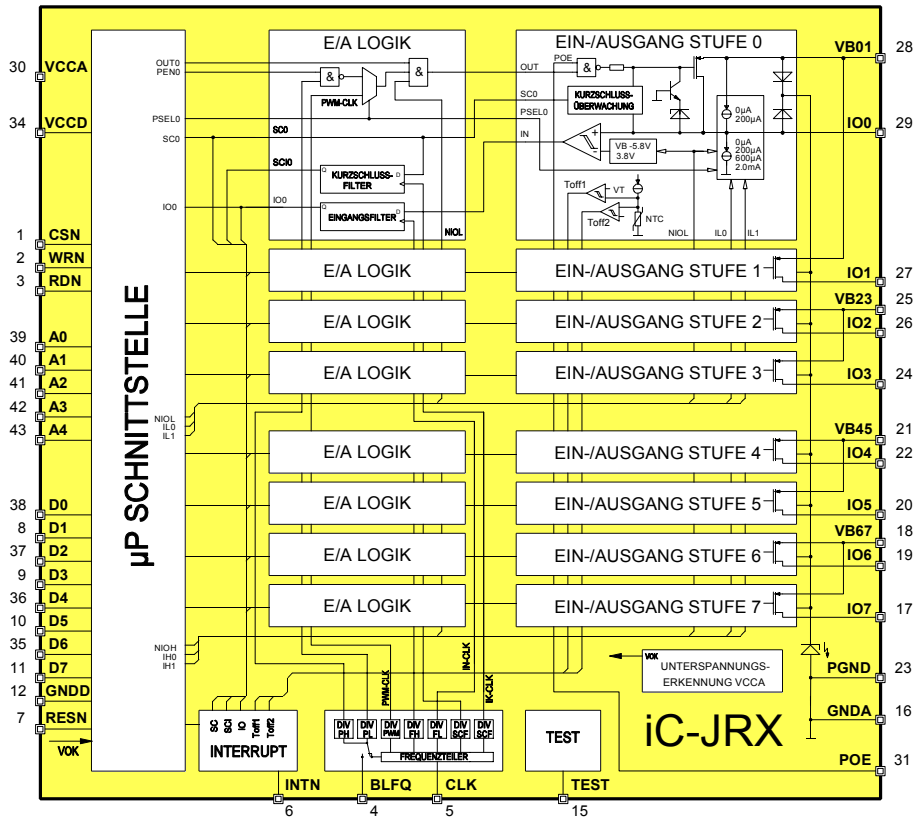
- Dual quad high-side driver as a bidirectional µP interface with digital filtering in industrial 24 V applications

PACKAGES



PLCC44

BLOCK DIAGRAM



DESCRIPTION

iC-JRX is an 8-fold high-side driver with integrated control logic, internally divided into two independent blocks (nibbles). Both blocks can be individually set to input or output. The µP interface is made up of eight data, five address and three control pins. Two further clock inputs control internal sequences (input filter, pulse operation of the outputs). Starting with reset state, various register partitionings dependent on the selected operating mode are possible.

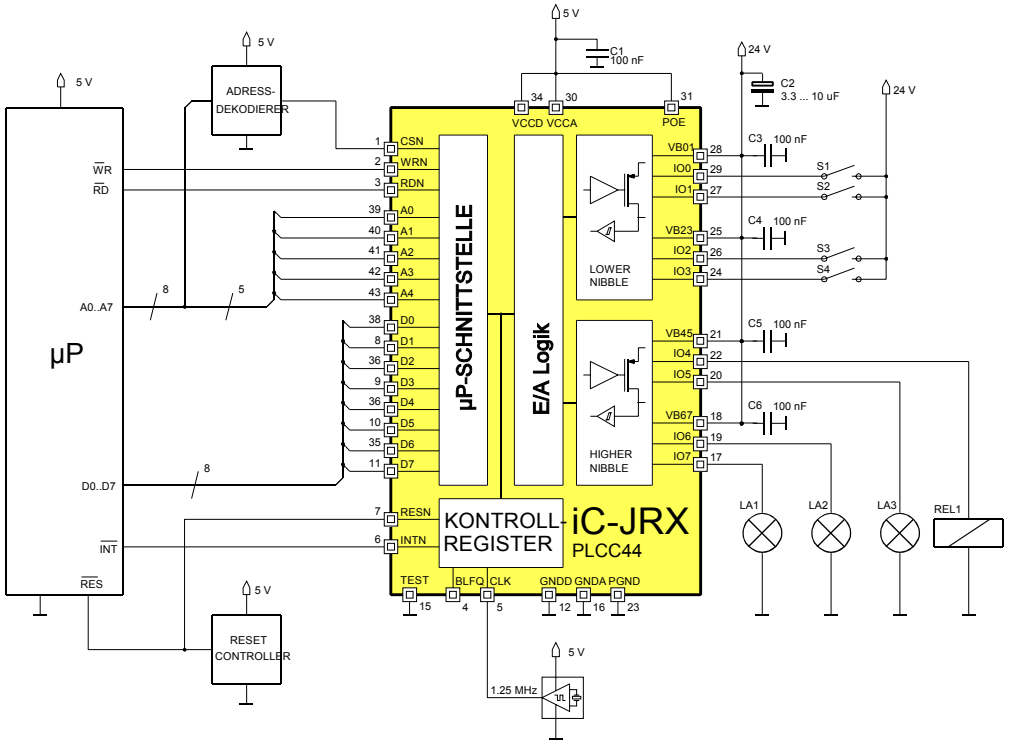
Input mode is used to log logic levels at 24 V. An interrupt message can be generated when a signal at the inputs changes. Spurious signals are rejected by the device's adjustable digital filters. When the inputs are open the programmable pull-down current sets defined levels and acts as the bias current for switching contacts.

In output mode the power output stages can drive any desired load to GND (e.g. lamps, long cables or relays) at a continuous current of 100 mA or 500 mA in pulse operation. Spikes and flyback currents are discharged through the integrated flyback circuits. All output stages are short-circuit-proof and two-stage temperature monitoring (with interrupt messages) protects against thermal damage caused by large power dissipation. A short circuit at one of the outputs can cause an interrupt; the current short circuit status can be scanned via the µP interface. Pulse mode can be selected for each output, such as for indicator lamps in plugboards, in order to offload the control software used. The actual switching level of the output can be read out via the µP interface and be used to check for cable fractures with the pull-up currents. A PWM signal can also be switched to any selected output. All outputs can be switched off via a mutual disable input e.g. by a processor-independent watchdog circuit.

An interrupt pipeline which prevents the loss of interrupts allows reliable processing of interrupts using the applied control software.

With low voltage the voltage monitor resets all registers and in doing so switches off the power output stages.

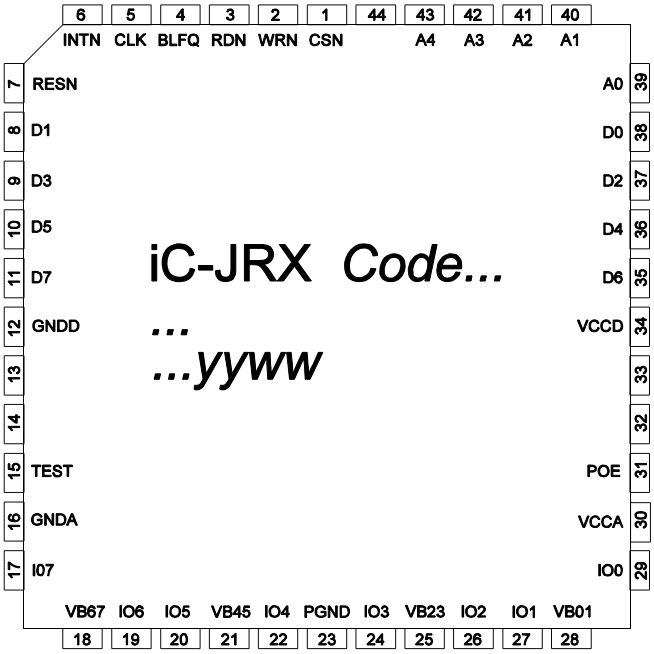
Diodes protect all inputs and outputs against ESD. The device is also immune to burst transients according to IEC 1000-4-4 (4 kV; previously IEC 801-4).



Typical application circuit

PACKAGES PLCC44 to JEDEC Standard

PIN CONFIGURATION PLCC44
(top view)



PIN FUNCTIONS PLCC44

No.	Name	Fct.	Description
1	CSN	I	Chip Select, active low
2	WRN	I	Write Enable, active low
3	RDN	I	Read Enable, active low
4	BLFQ	I	Clock Flash Mode
5	CLK	I	Clock Filter and PWM Function
6	INTN	O	Interrupt Message, active low
7	RESN	I	Reset, active low
8	D1	B	Data Bus Bit 1
9	D3	B	Data Bus Bit 3
10	D5	B	Data Bus Bit 5
11	D7	B	Data Bus Bit 7
12	GNDD		Ground (digital section)
13	n.c.		
14	n.c.		
15	TEST	B	Test Pin
16	GNDA		Ground (analog section)
17	IO7	B	I/O Stage 7
18	VB67		Power Supply Driver Stage 6+7
19	IO6	B	I/O Stage 6
20	IO5	B	I/O Stage 5
21	VB45		Power Supply Driver Stage 4+5
22	IO4	B	I/O Stage 4

No.	Name	Fct.	Description
23	PGND		Ground (ESD protection circuitry)
24	IO3	B	I/O Stage 3
25	VB23		Power Supply Driver Stage 2+3
26	IO2	B	I/O Stage 2
27	IO1	B	I/O Stage 1
28	VB01		Power Supply Driver Stage 0+1
29	IO0	B	I/O Stage 0
30	VCCA		+5 V Supply Voltage (analog section)
31	POE	I	Power Output Enable
32	n.c.		
33	n.c.		
34	VCCD		+5 V Supply Voltage (digital section)
35	D6	B	Data Bus Bit 6
36	D4	B	Data Bus Bit 4
37	D2	B	Data Bus Bit 2
38	D0	B	Data Bus Bit 0
39	A0	I	Address Bus Bit 0
40	A1	I	Address Bus Bit 1
41	A2	I	Address Bus Bit 2
42	A3	I	Address Bus Bit 3
43	A4	I	Address Bus Bit 4
44	n.c.		

Functions: I = Input, O = Output, B = bidirectional
External wiring VCCA, VCCD to +5 V and GNDA, GNDD, PGND to 0 V required.

PROGRAMMING

Register Overview

	Address						
A(4..0)d	A4	A3	A2	A1	A0	**Write**	**Read**
0	0	0	0	0	0	-	Input Register [1]
1	0	0	0	0	1	-	Change-of-input Message [2]
2	0	0	0	1	0	-	Interrupt Status Register
3	0	0	0	1	1	-	Overcurrent Message [3]
4	0	0	1	0	0	-	Overcurrent Status
5	0	0	1	0	1	-	Device ID
6	0	0	1	1	0	Output Register	
7	0	0	1	1	1	Flash Pulse Enable	
8	0	1	0	0	0	Change-of-input Interrupt Enable [4]	
9	0	1	0	0	1	Overcurrent Interrupt Enable	
10	0	1	0	1	0	Control Word 1 (I/O filters)	
11	0	1	0	1	1	Control Word 2 (I/O pin functions)	
12	0	1	1	0	0	Control Word 3 (flash pulse settings)	
13	0	1	1	0	1	Control World 4 (filter settings for overcurrent message)	
14	0	1	1	1	0	Control Word 5 (PWM enable and pin selection)	
15	0	1	1	1	1	PWM Register	
16	1	0	0	0	0	-	
...	...	...	...	...	...	-	
26	1	1	0	1	0	-	
27	1	1	0	1	1	-	A/D Interface
28	1	1	1	0	0	Test Register 1	
29	1	1	1	0	1	Test Register 2	
30	1	1	1	1	0	Test Register 3	
31	1	1	1	1	1	Test Control Register	

[1]) Reads the inputs or reads back the outputs, depending on I/O pin mode
[2]) For I/O pins in input mode (register is '0' in output mode)
[3]) For I/O pins in output mode (register is '0' in input mode)
[4]) Only writable in input mode

Control Word 1 (I/O filters)								**Add.: 10**
								reset entry: 00h
	higher nibble				lower nibble			
Bit Name	7 BYPH	6 -	5 FH1	4 FH0	3 BYPL	2 -	1 FL1	0 FL0

higher nibble

Bit 7 BYPH	0 1	I/O filters active Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.			(r)
Bit 5..4 FH1..0		FH1	FH0	Filter times	
		0 0 1 1	0 1 0 1	14.5 × tc(CLK) ± 1 × tc(CLK) 896.5 × tc(CLK) ± 64 × tc(CLK) 3584.5 × tc(CLK) ± 256 × tc(CLK) 7168.5 × tc(CLK) ± 512 × tc(CLK)	

lower nibble

Bit 3 BYPL	0 1	I/O filters active Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.			(r)
Bit 1..0 FL1..0		FL1	FL0	Filter times	
		0 0 1 1	0 1 0 1	14.5 × tc(CLK) ± 1 × tc(CLK) 896.5 × tc(CLK) ± 64 × tc(CLK) 3584.5 × tc(CLK) ± 256 × tc(CLK) 7168.5 × tc(CLK) ± 512 × tc(CLK)	(r)

'-' Free memory location without a function. Status after a reset is ‘0’
'xx'h Indicates hexadecimal data for logic states. ‘x’ indicates binary data
(r) Status after a reset

Control Word 2 (I/O pin functions)								**Add.: 11**
								reset entry: 00h
	higher nibble				lower nibble			
Bit Name	7 NIOH	6 -	5 IH1	4 IH0	3 NIOL	2 -	1 IL1	0 IL0

higher nibble

Bit 7 NIOH	0 1	Input mode Output mode			
Bit 5..4 IH1..0		Current sources at I/O pins 4..7			
		IH1	IH0	in input mode (sources low-side)	in output mode (sources high-side)
		0 0 1 1	0 1 0 1	0 µA 200 µA 600 µA 2 mA	0 µA 200 µA 0 µA 200 µA (r)

lower nibble

Bit 3 NIOL	0 1	Input mode Output mode			
Bit 1..0 IL1..0		Current sources at I/O pins 0..3			
		IL1	IL0	in input mode (sources low-side)	in output mode (sources high-side)
		0 0 1 1	0 1 0 1	0 µA 200 µA 600 µA 2 mA	0 µA 200 µA 0 µA 200 µA (r)

Control Word 3 (flash pulse settings)								**Add.: 12**
								reset entry: 00h
	higher nibble				lower nibble			
Bit Name	7 NOBLFQ	6 NOCLK	5 PH1	4 PH0	3 -	2 -	1 PL1	0 PL0

higher nibble

Bit 7 NOBLFQ	0 1	Flash pulse is generated from the external clock signal at BLFQ Flash Pulse is generated from clock signal CLK	(r)
Bit 6 NOCLK	0 1	Operation with the clock signal at CLK (all clock controlled actions are possible) Operation without the clock signal at CLK (filtering etc. deactivated)	(r)
Bit 5..4 PH1..0		Flash frequency for I/O pins 4..7	

PH1	PH0	NOBLFQ = 0		NOBLFQ = 1
0	0	f(BLFQ)		f(CLK) / 2^{19}
0	1	f(BLFQ) / 2		f(CLK) / 2^{20}
1	0	f(BLFQ) / 4		f(CLK) / 2^{21}
1	1	f(BLFQ) / 16	(r)	f(CLK) / 2^{23}

lower nibble

Bit 1..0 PL1..0	Flash frequency for I/O pins 0..3

PL1	PL0	NOBLFQ = 0		NOBLFQ = 1
0	0	f(BLFQ)		f(CLK) / 2^{19}
0	1	f(BLFQ) / 2		f(CLK) / 2^{20}
1	0	f(BLFQ) / 4		f(CLK) / 2^{21}
1	1	f(BLFQ) / 16	(r)	f(CLK) / 2^{23}

Control Word 4 (filter settings for overcurrent message)								**Add.: 13**
								reset entry: 00h
Bit Name	7 EOI	6 -	5 -	4 SCFH	3 BYPSCF	2 -	1 -	0 SCFL

Bit 7 EOI	0 1	No effect "DELETE"s the interrupt message (change-of-input message; interrupt status register, overcurrent message), accepts successive interrupts from the pipeline, deletes the message at INTN when the pipeline is empty; Bit automatically resets to '0'.	(r)
Bit 4 SCFH	0 1	Overcurrent message with 2.3ms filtering (higher nibble) Overcurrent message with 4.6ms Filtering (higher nibble) Gives the filter times with the maximum clock frequency permitted at CLK, i.e. 1.25 MHz: 2.3ms from (2689.5 ± 192)× t(CLK) and 4.6ms from (5378.5 ± 384) × t(CLK) respectively	(r)
Bit 3 BYPSCF	0 1	Filters for the overcurrent message are active Bypass for the filters: overcurrent messages are reprocessed in their unfiltered state	(r)
Bit 0 SCFL	0 1	Overcurrent message with 2.3 ms filtering (lower nibble) Overcurrent message with 4.6 ms filtering (lower nibble)	(r)

Control Word 5 (PWM enable and pin selection)								**Add.: 14**
								reset entry: 00h
Bit Name	7 -	6 -	5 -	4 PWMEN	3 PWMPN	2 PWM ADR(2)	1 PWM ADR(1)	0 PWM ADR(0)

Bit 4 PWMEN	0 1	PWM "DISABLED" PWM "ENABLED": the output selected with PWMADR receives the PWM signal. The relevant current sources are switched off.	(r)
Bit 3 PWMPN	0 1	PWM signal active low PWM signal active high	(r)

Bit 2..0
PWMADR 2..0

PWMADR2	PWMADR1	PWMADR0	Selected I/O pin
0	0	0	IO0 (control line PSEL0= 1)
0	0	1	IO1
0	1	0	IO2
0	1	1	IO3
1	0	0	IO4
1	0	1	IO5
1	1	0	IO6
1	1	1	IO7

PWM Register								**Add.: 15**
								reset entry: 00h
Bit Name	7 PWM7	6 PWM6	5 PWM5	4 PWM4	3 PWM3	2 PWM2	1 PWM1	0 PWM0

Bit 7..0 PWM7..0	'00'h '...'h 'FF'h	Output stage "OFF" (continously) Duration of the PWM signal in steps of 16× t(CLK) Output stage "ON" (continously) The PWM register determines the pulse length of the PWM signal. Output selection and enable are set via Control Word 5.	(r)

Input Register (read only) reading of inputs / output feedback								**Add.: 0**
								reset entry: 00h
Bit Name	7 IN7	6 IN6	5 IN5	4 IN4	3 IN3	2 IN2	1 IN1	0 IN0

Bit 7..0 IN7..0	0 1	Input/Output IOx reads '0' Input/Output IOx reads '1' INx indicates the state for IOx (via I/O filter or bypass).	(r)

Change-of-input Message (read only) for I/O stages in input mode								**Add.: 1**
								reset entry: 00h
Bit Name	7 DCH7	6 DCH6	5 DCH5	4 DCH4	3 DCH3	2 DCH2	1 DCH1	0 DCH0

Bit 7..0 DCH7..0	0 1	No change of state at the input IOx or no interrupt enable Input IOx has had a change of state enabled for interrupt messages Read access gates off changes to the register; the register is reenabled only when reset via EOI. Any successive interrupts which occur during the read-out phase and before a reset with EOI are trapped by an interrupt pipeline. If this happens, the message at INTN cannot be deleted by EOI, i.e. INTN constantly remains on low. In this instance, EOI fills the change-of-input message from the pipeline. Status bits can also be selectively deleted by disabling and reenabling IENx. ‘0’ is output for IOx pins in output mode.	(r)

Interrupt Status Register (read only)								**Add.: 2**
								reset entry: 00h
	higher nibble				lower nibble			
Bit Name	7 DCHI	6 IET2	5 IET1	4 ISCI	3 -	2 ET2	1 ET1	0 SCS

higher nibble

overcurrent, excessive temperature, change-of-input data (interrupts stored)		
		Read access gates off changes to the register; the register is reenabled only when reset via EOI. Any successive interrupts for IET1 and IET2 which occur during the read-out phase and before a reset with EOI are trapped (pipeline). If this happens, the message at INTN cannot be deleted by EOI, i.e. INTN constantly remains on low. In this instance, EOI fills the excessive temperatue message from the pipeline.
Bit 7 DCHI	0 1	No message Interrupt through change-of-input message (r)
Bit 6 IET2	0 1	No message Interrupt through excessive temperature level 2 (r)
Bit 5 IET1	0 1	No message Interrupt through excessive temperature level 1 (r)
Bit 4 ISCI	0 1	No message Interrupt through overcurrent message (r)

lower nibble

overcurrent status, excessive temperature status (real time signals, at the time of readout)		
Bit 2 ET2	0 1	No error message Excessive temperature level 2 (shutdown) (r)
Bit 1 ET1	0 1	No error message Excessive temperature level 1 (warning) (r)
Bit 0 SCS	0 1	No error message Overcurrent status (e.g. caused by low-side short circuit) (r)

Overcurrent Message (read only)								**Add.: 3**
								reset entry: 00h
Bit Name	7 SCI7	6 SCI6	5 SCI5	4 SCI4	3 SCI3	2 SCI2	1 SCI1	0 SCI0

Bit 7..0 SCI7..0	0 1	No message (r) Output IOx has had an overcurrent state enabled for interrupt messages (short circuit) Read access gates off changes to the register; the register is reenabled only when reset via EOI. Any successive interrupts which occur during the read-out phase and before a reset with EOI are trapped by an interrupt pipeline. If this happens, the message at INTN cannot be deleted by EOI, i.e. INTN constantly remains on low. In this instance, EOI fills the overcurrent message from the pipeline. '0' is output for IOx pins in input mode. SCIx reports for IOx.

Overcurrent Status (read only)								**Add.: 4**
								reset entry: 00h
Bit	7	6	5	4	3	2	1	0
Name	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Bit 7..0 SC7..0	0 1	No overcurrent Overcurrent in output IOx, e.g. through a low-side short circuit This signal acts as error analysis and does not generate any interrupts (real time, no register). '0' is output for IOx pins in input mode. SCx reports for IOx.

Device Identification (read only)								**Add.: 5**
								reset entry: 00h
Bit	7	6	5	4	3	2	1	0
Name	-	-	DID5	DID4	DID3	DID2	DID1	DID0

Bit 5..0 DID5..0		ID code for iC-JRX: '00 0000' (binary) (r) DID0= '1' with RESN= '0' and with undervoltage

Output-Register for I/O stages with output function								**Add.: 6**
								reset entry: 00h
Bit	7	6	5	4	3	2	1	0
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bit 7..0 OUT7..0	0 1	H High-side driver "OFF" (r) High-side driver "ON", i.e. normally, IOx = '1' OUTx switches the high-side driver for IOx.

Flash Pulse Enable for I/O stages with output function								**Add.: 7**
								reset entry: 00h
Bit	7	6	5	4	3	2	1	0
Name	PEN7	PEN6	PEN5	PEN4	PEN3	PEN2	PEN1	PEN0

Bit 7..0 PEN7..0	0 1	Flash pulse "DISABLED" (r) Flash pulse "ENABLED" PENx enables the flash pulse for IOx.

Change-of-input Interrupt Enable for I/O stages with input function								**Add.: 8**
								reset entry: 00h
Bit Name	7 IEN7	6 IEN6	5 IEN5	4 IEN4	3 IEN3	2 IEN2	1 IEN1	0 IEN0

Bit 7..0 IEN7..0	0 1	"DISABLED" for interrupt "ENABLED" for interrupt: a hi→lo or lo→hi change of state at the input IOx triggers an interrupt. Outputs IOx cannot be enabled for messaging. IENx enables the input IOx for interrupt.	(r)

Overcurrent Interrupt Enable								**Add.: 9**
								reset entry: 00h
Bit Name	7 SCEN7	6 SCEN6	5 SCEN5	4 SCEN4	3 SCEN3	2 SCEN2	1 SCEN1	0 SCEN0

Bit 7..0 SCEN7..0	0 1	"DISABLED" for interrupt "ENABLED" for interrupt: a short-circuit at IOx triggers an interrupt. SCENx enables the output IOx for interrupt.	(r)

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VCCD VCCA	Supply Voltage VCCD, VCCA			-0.3	7	V
G002	VB	Supply Voltage VB			-0.3	30	V
G003	V(IO)	Voltage at IO0..7	IOx= off		-10	30	V
G004	Idc(IO)	Current in IO0..7		1	-500	100	mA
G005	Ipk(IO)	Pulse Current in IOx	IOx= hi (*), τ= 2ms, T≥ 2s	2	-1		A
G006	Imax()	Current in VCCD, VCCA			-50	50	mA
G007	Imax(VB)	Current in VB01, VB23, VB45, VB67			-4	4	A
G008	Ic()	Current in Clamping Diodes CSN, WRN, RDN, A0..4, D0..7, RESN, CLK, BLFQ, POE	D0..7 with input function		-20	20	mA
G009	I()	Current in D0..7, INTN	D0..7 with output function		-25	25	mA
G010	Ilu()	Pulse Current in CSN, WRN, RDN, A0..4, D0..7, RESN, CLK, BLFQ, INTN, POE, IO0..7 (Latch-Up Strength)	pulse duration < 10µs, all in-/outputs open		-100	100	mA
E001	Vd()	ESD Susceptibility at all Pins	MIL-STD-883.D, Method 3015.7; HBM 100pF discharged through 1.5kΩ			2	kV
E002	Vb()	Permissible Burst-Transients at IO0..7	according to IEC 1000-4-4			4	kV
TG1	Tj	Junction Temperature			-40	150	°C
TG2	Ts	Storage Temperature			-40	150	°C

(*) IOx= hi: pin set to output, active high, x= 0..7

THERMAL DATA

Operating Conditions: VCCD= VCCA= 5V ±10%, VB= 19.2..25.2V
GNDA= GNDD= PGND= 0V, alle inputs wired (to hi respectively to lo)

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range			0		70	°C
T2	Rthja	Thermal Resistance Chip to Ambient	surface mounted on PCB, no additional cooling areas			55		K/W

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCD= VCCA= 5V ±10%, VB= 19.2..25.2V,
GNDA= GNDD= PGND= 0V, all inputs wired (to hi respectively to lo), Tj= 0..125°C unless otherwise noted.

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VCCA	Permissible Supply Voltage VCCA				4.5		5.5	V
002	I(VCCA)	Supply Current in VCCA					7.5	13	mA
003	I(VCCA)	Supply Current in VCCA	no supply voltage VB					25	mA
004	VCCD	Permissible Supply Voltage VCCD				4.5		5.5	V
005	I(VCCD)	Supply Current in VCCD (static)	all logic inputs lo= 0V or hi= VCCD				0.3	3	mA
006	I(VCCD)	Supply Current in VCCD (dynamic)	continously repeated read access: tlo(RDN)= thi(RDN)= 200ns; data word changes every other cycle between "00" and "FF", CL(D0..7)= 200pF					35	mA
007	I(VCCD)	Supply Current in VCCD	all logic inputs lo= 0.8V				80		mA
008	I(VCCD)	Supply Current in VCCD	all logik inputs hi= 2.0V				100		mA
009	VB	Permissible Supply Voltage VB (operating range)				19.2		25.2	V
010	I(VB)	Supply Current in VB	POE= hi, IOx= hi, no load				8.5	14	mA
011	I(VB)	Supply Current in VB	IOx= off				2	4	mA
012	Vc()lo	ESD Clamp Voltage lo at VCCA, VCCD, VB	I()= -20mA			-1.4		-0.3	V
013	Vc()hi	ESD Clamp Voltage hi at VCCA	I()= 20mA					11	V
014	Vc()hi	ESD Clamp Voltage hi at VB	I()= 20mA			30	47	60	V
015	Vc()lo	ESD Clamp Voltage lo at IOx	I()= -20mA			-30		-10	V
016	Vc()hi	ESD Clamp Voltage hi at IOx	I()= 20mA			30	47	60	V
I/O Stages: High-Side Driver IO0..7									
101	Vs()hi	Saturation Voltage hi	Vs()hi= VB -V(IOx); I(IOx)= -10mA	1				0.2	V
102	Vs()hi	Saturation Voltage hi	Vs()hi= VB -V(IOx); I(IOx)= -100mA	1				0.6	V
103	Vs()hi	Saturation Voltage hi for pulse load	Vs()hi= VB -V(IOx); I(IOx)= -500mA, τ= 2ms, T≥ 2s	2				2	V
104	Isc()hi	Overcurrent Cut-off	IOx= hi, V(IOx)= 0..VB-3V			-1.8		-0.55	A
105	It()scs	Threshold Current for Overcurrent Message				-1.2		-0.55	A
106	Vc()lo	Free-wheeling Clamp Voltage	I(IOx)= -100mA			-15		-12	V
107	SRhi()	Slew Rate hi	CL= 0..100pF, RL= 240Ω..1kΩ			15		40	V/µs
108	SRlo()	Slew Rate lo	CL= 0..100pF, RL= 240Ω..1kΩ			15		40	V/µs
109	tplh()	Propagation Delay until IOx: lo→hi	write cycle, WRN: lo→hi until V(IOx) > V0(IOx)+1V					5	µs
110	tphl()	Propagation Delay until IOx= off	write cycle, WRN= lo→hi until V(IOx) < 80% (VB-Vs(IOx)hi)					5	µs

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCD= VCCA= 5V ±10%, VB= 19.2..25.2V,
GNDA= GNDD= PGND= 0V, all inputs wired (to hi respectively to lo), Tj= 0..125°C unless otherwise noted.

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
I/O Stages: Current Sources at IO0..7									
201	Ipd()	Pull-down Current Source (200µA)	IOx with input function, IL1= IH1= 0, IL0= IH0= 1, V(IOx)= 3V..VB			120	200	280	µA
202	Ipd()	Pull-down Current Source (600µA)	IOx with input function, IL1= IH1= 1, IL0= IH0= 0, V(IOx)= 3V..VB			400	600	800	µA
203	Ipd()	Pull-down Current Source (2mA)	IOx with input function, IL1= IH1= 1, IL0= IH0= 1, V(IOx)= 3V..VB			1.4	2	2.7	mA
204	Ipu()	Pull-up Current Source (200µA)	IOx with output function and IOx= off, IL0, IH0= 1; V(IOx)= -7V..VB-2V			120	200	280	µA
205	tp()Ion	Current Source Enable Time (pull-down and pull-up sources)	write cycle, WRN: lo→hi til I(IOx) > 90% Ipd(IOx) or I(IOx) > 90% Ipu(IOx)					5	µs
206	tp()Ioff	Current Source Disable Time (pull-down and pull-up sources)	write cycle, WRN: lo→hi til I(IOx) < 10% Ipd(IOx) or I(IOx) < 10% Ipu(IOx)					5	µs
207	Ilk()	Leakage Current	IOx with input function or output function with IOx= off and IL1, IH1, IL0, IH0= 0; V(IOx)= -7V..VB			-20		20	µA
208	Ilk()	Leakage Current	logic see item 207; V(IOx)= -10V..-7V			-100		20	µA
209	Ilk()	Leakage Current	logic see item 207; V(IOx)= VB..VB+0.4V			-20		100	µA
210	Ilk()	Leakage Current	logic see item 207; V(IOx)= VB..30V				200	500	µA
211	Ilk()	Leakage Current	no supply voltage VB					5	mA
I/O Stages: Comparator IO0..7									
301	Vin()	Permissible Input Voltage referenced to VB	V(VB)= 0..25.2V, (see also max. rating G003)					25.2	V
302	Vt()hi	Threshold Voltage hi	IOx with input function					82	%VCC
303	Vt()lo	Threshold Voltage lo	IOx with input function			66			%VCC
304	Vt()hys	Hysteresis	IOx with input function, Vt()hys= Vt()hi -Vt()lo			100			mV
305	Vt()hi	Threshold Voltage hi referenced to VB	IOx with output function, Vt()hi= VB -V(IOx)			5			V
306	Vt()lo	Threshold Voltage lo referenced to VB	IOx with output function, Vt()lo= VB -V(IOx)					6.7	V
307	Vt()hys	Hysteresis	IOx with output function, Vt()hys= Vt()lo -Vt()hi			100			mV
308	tp(IOx -Dx)	Propagation Delay Input IOx to Data Output Dx	I/O filter inactive, CSN= lo, RDN= lo, A0..4= lo					10	µs

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCD= VCCA= 5V ±10%, VB= 19.2..25.2V,
GNDA= GNDD= PGND= 0V, all inputs wired (to hi respectively to lo), Tj= 0..125°C unless otherwise noted.

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Thermal Shutdown									
401	Toff1	Over-Temperature Threshold Level 1: warning				105		130	°C
402	Toff1	Level 1 Release				100		125	°C
403	Thys1	Level 1 Hysteresis	Thys1= Ton1 -Toff1			2		7	°C
404	Toff2	Over-Temperature Threshold Level 2: shutdown				130		155	°C
405	Ton2	Level 2 Release				100		125	°C
406	Thys2	Level 2 Hysteresis	Thys2= Toff2 -Ton2			22		37	°C
407	ΔT	Temperatur Difference Level 2 to Level 1	ΔT= Toff2 -Toff1			20		30	°C
Bias and Low Voltage Detection									
501	VCCAon	Turn-on Threshold VCCA (Power-on release)				3.9	4.1	4.4	V
502	VCCAoff	Undervoltage Threshold VCCA (Power-down reset)				3.8	4	4.3	V
503	VCCAhys	Hysteresis	VCCAhys= VCCAon -VCCAoff			80	100	130	mV
504	toff	Power Down Time required for low voltage detection	VCCA= 2.5V..VCCAoff			1			µs
505	tdoff	Propagation Delay until Reset after Low Voltage at VCCA						12	µs
µP Interface, I/O Logic, Frequency Divider, Interrupt									
701	Ilk(Dx)	Leakage Current in Dx	D0..7 with input function			-5		5	µA
702	Ii()	Input Current in Schmitt-Trigger Input CSN, WRN ,RDN, A0..4, RESN, CLK, BLFQ, D0..7	V()= 0V..VCCD, D0..7 with input function			-1		1	µA
703	Vt()hi	Threshold Voltage hi at Schmitt-Trigger Input CSN, WRN, RDN, A0..4, RESN, CLK, BLFQ, D0..7	D0..7 with input function					2.2	V
704	Vt()lo	Threshold Voltage lo at Schmitt-Trigger Input CSN, WRN, RDN, A0..4, RESN, CLK, BLFQ, D0..7	D0..7 with input function			0.8			V
705	Vt()hys	Schmitt-Trigger Input Hysteresis CSN, WRN, RDN, A0..4, RESN, CLK, BLFQ, D0..7	Vt()hys= Vt()hi-Vt()lo; D0..7 with input function			300			mV
706	Vs()hi	Saturation Voltage hi at INTN	Vs()hi= VCCD -V(INTN); I(INTN)= -2mA					0.8	V
707	Vs()lo	Saturation Voltage lo at INTN	I(INTN)= 100µA I(INTN)= 2mA					0.2 0.49	V V
708	Vs()hi	Saturation Voltage hi at Dx	Vs()hi= VCCD -V(Dx); I(Dx)= -4mA					0.8	V
709	Vs()lo	Saturation Voltage lo at Dx	I(Dx)= 4mA					0.49	V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCD= VCCA= 5V ±10%, VB= 19.2..25.2V,
GNDA= GNDD= PGND= 0V, all inputs wired (to hi respectively to lo), Tj= 0..125°C unless otherwise noted.

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
µP Interface, I/O Logic, Frequency Divider, Interrupt (cont'd)									
710	Vc()hi	ESD Clamp Voltage hi at CSN, WRN, RDN, A0..4, RESN, CLK, BLFQ, D0..7, INTN	Vc()hi= V() -VCCD; D0..7 with input function, I()= 20mA			0.4		1.5	V
711	Vc()lo	ESD Clamp Voltage lo at CSN, WRN, RDN, A0..4, RESN, CLK, BLFQ, D0..7, INTN	D0..7 with input function, I()= -20mA			-1.5		-0.4	V
Input POE									
F01	Vt()hi	Threshold Voltage hi						2.2	V
F02	Vt()lo	Threshold Voltage lo				0.8			V
F03	Vt()hys	Hysteresis	Vt()hys= Vt()hi -t()lo			300			mV
F04	Rpd()	Pull-Down Resistor				24		72	kΩ
F05	tw()lo	Disable/Enable Pulse Width				1000			ns
F06	tsup()	Permissible Interference Pulse Width						100	ns
F07	td(POE-IOx)	Power Output Switch-off Delay	POE: hi→lo until IOx disabled, ie. V(IOx)< 80% (VB -Vs(IOx)hi), RL= 240Ω..1kΩ					5	µs
F08	Vc()hi	ESD Clamp Voltage hi	Vc()hi= V(POE) -VCCA; I(POE)= 20mA			0.8		2	V
F09	Vc()lo	ESD Clamp Spannung lo	I(POE)= -20mA			-1.5		-0.4	V
Switching Characteristics									
801	td()	Permissible Cycle Duration at CLK				800			ns
802	tw()	Permis. Pulse Width lo at CLK				400			ns
803	td()	Permissible Cycle Duration at BLFQ				100			ms
804	tw()	Permis. Pulse Width lo at BLFQ				50			ms

ELECTRICAL CHARACTERISTICS: WAVEFORMS

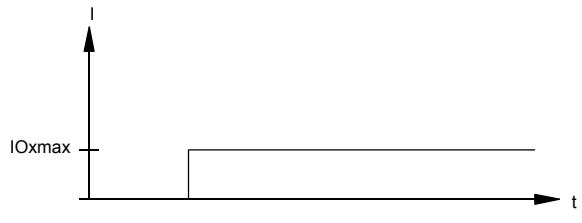


Fig. 1: DC load

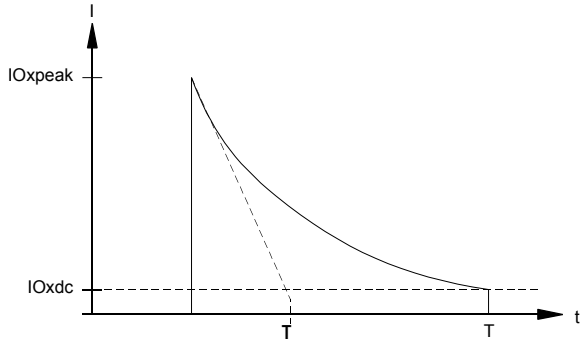


Fig. 2: Pulse load, pulse duration 2 ms

OPERATING REQUIREMENTS: µP INTERFACE

Operating Cconditions: VCCD, VCCA= 5V ±10%, VB= 19.2..25.2V, GNDA= GNDD= PGND= 0V,
Ta= 0..70°C, CL()= 150pF, input levels lo= 0.45V, hi= 2.4V, see Fig. 3 for reference levels

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
Data Word Read Timing							
I1	t_{AR1} t_{AR2}	Setup Time: CSN, A0..4 set before RDN hi→lo		4	30		ns
I2	t_{RA}	Hold Time: CSN, A0..4 stable after RDN lo→hi		4	10		ns
I3	t_{RD}	Read Data Access Time: data valid after RDN hi→lo		4		120	ns
I4	t_{DF}	Read Data Hold Time: ports high impedance after RDN lo→hi		4		65	ns
I5	t_{RL}	Required Read Signal Duration at RDN			50		ns
Data Word Write Timing							
I6	t_{AW1} t_{AW2}	Setup Time: CSN, A0..4 set before WRN hi→lo		4	30		ns
I7	t_{DW}	Write Data Setup Time: data valid before WRN lo→hi		4	100		ns
I8	t_{WA}	Hold Time: CSN, A0..4 stable after WRN lo→hi		4	10		ns
I9	t_{WD}	Write Data Hold Time: data valid after WRN lo→hi		4	10		ns
I10	t_{WL}	Required Write Signal Duration at WRN		4	50		ns
Read/Write Timing							
I11	t_{cyc}	Recovery Time between cycles: RDN lo→hi to RDN hi→lo, RDN lo→hi to WRN hi→lo, WRN lo→hi to WDN hi→lo, WRN lo→hi to RDN hi→lo		4	165		ns

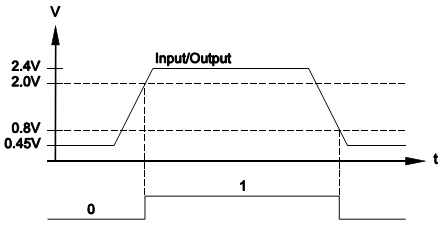


Fig. 3: Reference levels

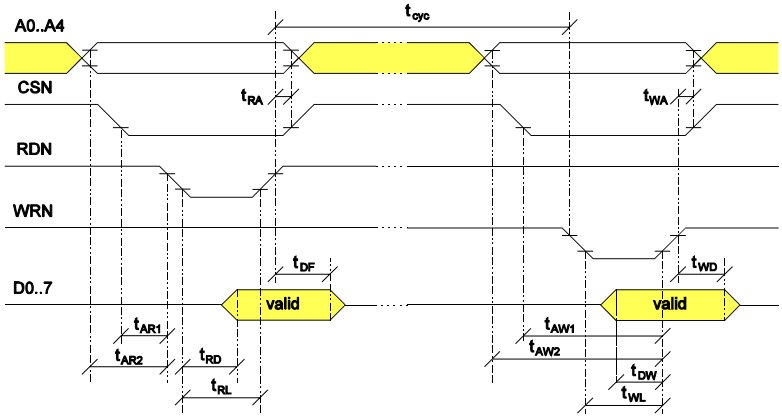


Fig. 4: Data word read/write timing

DESCRIPTION OF FUNCTIONS

iC-JRX is a bidirectional device which can analyze signals at the I/O pins and drive loads connected to ground. The input and output modes can be set in blocks of 4 bits (using nibbles).

I/O stages in input mode pass on the external signal via digital filtering which can be switched off as required by way of a bypass. Changes of level at any one input can generate an interrupt at the INTN port – providing that messaging is enabled. Individually programmable low-side current sources are available for each pin, enabling logic levels for the inputs to be defined (ranges 200 µA, 600 µA and 2 mA).

I/O stages in output mode can switch currents of up to 500 mA. A 200 µA high-side current source can be activated to check the load for any interruptions. A PWM function and a flash mode for indicator lamps are integrated in the device, both of which can be selected for any chosen output pin. If overcurrent is determined at any of the outputs, caused for example by a short-circuit, this can be reported as an interrupt if suitably enabled. If the device exceeds normal operating temperature, an interrupt gives a temperature warning; if, following this, the device continues to overheat, the outputs are shutdown.

I/O stages in input mode
Input register (add. 0): reads the inputs
A hi level at IOx generates a hi signal at Dx. Any change to an input signal is accepted via digital filtering only after the chosen filter time has ended. Doing this, the input comparator of each I/O stage switches the count direction of a 3-bit counter. The counter output changes only when the final status is reached. The counters are reset to a value of 3 by a lo signal at the RESN reset input. The counter is clocked externally via the CLK pin.

The scaling factor for the clock frequency and the input filter bypass can be programmed separately for both nibbles (the bypass with BYPH or BYPL in control word 1). Switching the bypass permits operation without an external clock signal (see below).
After the change-of-input message has been enabled (add. 8) a change of level at one of the I/O pins is signaled via an interrupt to the microcontroller.

I/O stages in output mode
Input register (add. 0): reads the output feedback
A hi level at IOx generates a hi signal at Dx. Through this, the microcontroller can make a direct check of the switching state and, in conjunction with the 200 µA high-side current source, can monitor the channel for any cable fractures. As with the input read, the read-back signals can be reprocessed in their filtered or unfiltered state.

Output register (add. 6): switches the various output stages on and off (for POE= 1)
Flash pulse enable (add. 7): enables flash mode
With this, each of the various output stages can be set to flash mode, providing the value of the corresponding output register is ‘1’. The flash frequency is derived from BLFQ or, alternatively, can be generated from CLK (via NOBLFQ in control word 3). Different flash frequencies can be set for both nibbles (ports 0..3 and 4..7).

PWM enable (add. 14)
A PWM signal for any chosen output stage can be activated with the aid of PWMEN in control word 5. The I/O stage is selected using PWMADR2..0. PWMPN determines the direction of the PWM signal (active hi or active lo). The shape of the PWM signal is given by the value of the PWM register (add. 15), multiplied by 16xtd(CLK).

Interrupts
Interrupt outputs at INTN can be triggered by a change of (filtered) input signal, by overcurrent, signaled at an I/O pin (e.g. due to a short circuit), or by exceeding maximum temperature levels (2 stages).

For each individual I/O stage, interrupt outputs can be caused by a change of input, or, with stages in output mode, also by a short circuit. The relevant interrupt enables determine which messages are stored and displayed. The display of interrupt messages caused by excessive temperature is not maskable; it is permanently enabled.

When an event occurs which is enabled to produce an interrupt output, pin INTN is set to '0'. An interrupt status register read-out (add. 2) enables the nature of the message to be determined and the I/O stage causing the interrupt to be located. Thus with a change-of-input message the initiating I/O stage is shown in the corresponding register (add. 1); with an overcurrent interrupt, the overcurrent message register (add. 3) pinpoints the I/O stage with a short circuit.

Interrupts are deleted by simply setting EOI in control word 4. This bit then automatically resets to '0'. If during operation the I/O mode is switched, i.e. from input to output mode, all interrupt messages are deleted via EOI.

To avoid interrupt messages caused by other sources in the time between the read-out of an interrupt register and the deletion of the current interrupt being overlooked, successive interrupts are stored in a pipeline. In the event of there being any successive interrupts, output INTN remains at '0' after the current interrupt has been deleted using EOI. The new interrupt source is shown in the interrupt status register and in the type-specific status registers.

Overcurrent messages
With an overload at one of the outputs the current in IOx is limited. In this instance an interrupt message is displayed, providing relevant interrupt enables have been set for overcurrent messages (add. 9) and the filter time set with control word 4 has elapsed. If this happens, ISCI is set in the interrupt status register (add. 2) and the relevant bit is set for the initiating I/O stage in the overcurrent message register (add. 3).

Under address 4 the current, unfiltered overcurrent status of each I/O stage can be read; an overall scan of all the I/O stages is also possible via bit SCS of the interrupt status register. This shows whether any of the I/O stages have overcurrent at the time of the readout. This short-circuit messaging allows permanent monitoring of the output transistors and clear allocation of the error message to the I/O stage affected.
Filtering of the overcurrent message can be shutdown via a bypass; this bypass can be activated for all I/O stages together using BYPSCF in control word 4 (add. 13).

Temperature monitoring
iC-JRX has a two-stage temperature monitor circuit.

Stage 1: A warning interrupt (INTN= 0) is generated if the first temperature level (Toff 1 at ca. 125 °C) is exceeded. Suitable measures to decrease the power dissipation of the driver can be implemented via the microcontroller.

Stage 2: If the second temperature level is exceeded (Toff 2 at ca. 150 °C), a second interrupt is generated (INTN= 0). At the same time the output transistors and the I/O stage current sources are shutdown, the output register and flash mode enable deleted.
Once the temperature level has returned to below that of Toff1 the current sources are reactivated. The output register and flash pulse enable have to be respecified to activate the output stages.

The interrupt status register (add. 2) gives information as to the stage of temperature interrupt but also on the current status of the temperature monitor. ET2 and ET1 statically indicate when Toff2 and Toff1 are exceeded, whereby the stored interrupt messages IET2 and IET1 and the display at INTN via EOI= 1 can be deleted (control word 4).

Low voltage detection
When the supply voltage at VCC is switched on, the output transistors are only released by the low voltage detector after the power-on enable VCCon has been reached. Should the supply voltage drop to VCCoff during operation, the I/O stages are disabled, i.e. the output transistors are turned off and the device reset (signal VOK). If the supply voltage should then rise to VCCon, iC-JRX is in its reset state.

Identification of the device
An identification code has been introduced to enable identification of device iC-JRX. Bit pattern ‘000000’b can be read out under address 5.

Reset
A reset (RESN= 0) sets the register entries to the reset values given in the tables. The output transistors and the current sources in the I/O stages are shutdown and all stages switched to input mode.

Operation without the BLFQ signal
Should no clock signal be available at pin BLFQ, iC-JRX can generate the flash pulse internally from the clock signal at pin CLK. To this end, NOBLFQ in control word 3 must be set to ‘1’. The flash period is then calculated from the clocking pulse at CLK by division by 2^{19}.

Operation without the CLK signal
iC-JRX is operable without a clocking pulse at the CLK pin. With NOCLK in control word 3 the clocked filtering for the I/O signals and overcurrent messaging is deactivated. The device remains fully functional with one exception; the PWM cannot be activated, as this is dependent on CLK.

The same behavior can be obtained by setting BYPH and BYPL in control word 1 together with BYPSCF in control word 4; all filters are avoided by way of a bypass circuit. This has one disadvantage, namely that interferences in the load lines, for example, can lead to the unwanted display of interrupts.

Forced shutdown of output stages
The output stages can be forcibly shutdown at input POE. A ‘1’ enables logic access to the drivers; an ‘0’ disables this. With this, a processor-independent watchdog can lock the outputs in the event of error, for example. An integrated pull-down resistor increases safety.

Pulse-width modulation

This function can be activated for any chosen I/O stage in output mode.

First the duty cycle is determined via the PWM register in 256 steps within one PWM period. Pulse direction and the address for the desired driver stage is selected via control word 5 (PWMPN, PWMADR2..0).

The PWM enable bit can now also be set via control word 5. With this enable, the current source and any active flash mode for the selected output are automatically switched off.

The set duty cycle is activated when a new PWM period is started.

A PWM signal is set at the selected output, whose frequency is determined by the clock signal at CLK and whose duty cycle follows the PWM register.

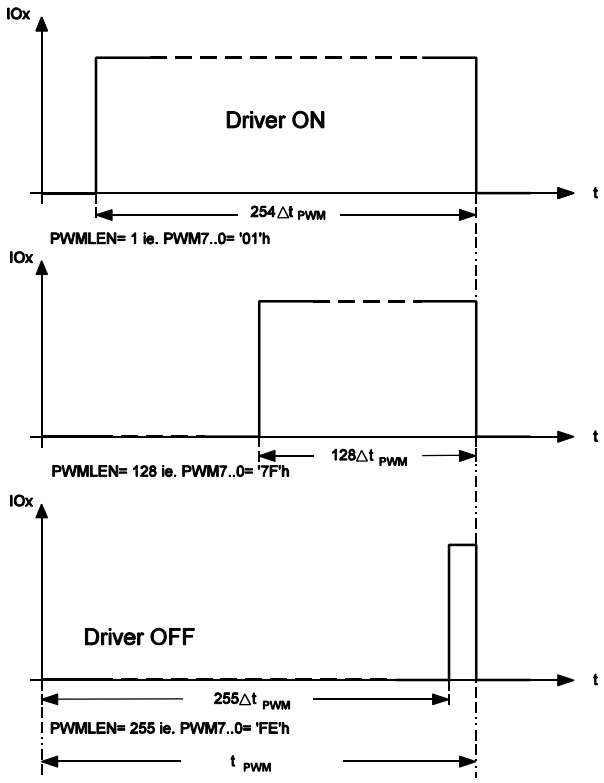


Fig. 5: PWM signal form

The following correlations apply:

$$f_{PWM} = \frac{f_{CLK}}{4096}\ ; \qquad \Delta t_{PWM} = \frac{1}{f_{PWM} \times 256}\ ; \qquad t_{PWMlo} = (PWMLEN + 1) \times \Delta t_{PWM}$$

f_{CLK} : Clock frequency CLK
f_{PWM} : frequency for the PWM signal at IOx
Δt_{PWM} : Smallest possible pulse duration 'lo' (8 µs with a 2 MHz clock)
t_{PWMlo} : pulse duration 'lo' (Iox = OFF with PWMPN = 1)
PWMLEN : Count pulse duration 'lo' stored in register PWM7..0

Selectable Pulse-Pause Ratios		
PWM7..0	PWMPN	Output signal
'00'h	0	Output stage "ON", Pin Iox = '1' (reset entry)
	1	Output stage "OFF", Pin Iox = '0'
'01'h .. 'FE'h	0	Output pin IOx goes for (PWMLEN + 1) × Δt_{PWM} to '0', and then for (255 - PWMLEN) × Δt_{PWM} to '1'
	1	Output pin IOx goes for (PWMLEN + 1) × Δt_{PWM} to '1', and then for (255 - PWMLEN) × Δt_{PWM} to '0'
'FF'h	0	Output stage "OFF", Pin Iox = '0'
	1	Output stage "ON", Pin Iox = '1'

ORDERING INFORMATION

Type	Package	Order designation
iC-JRX	PLCC44	iC-JRX PLCC44

For information about prices, terms of delivery, options for other case types, etc., please contact:

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