iC-PV

BATTERY-BUFFERED HALL-MULTITURN ENCODER

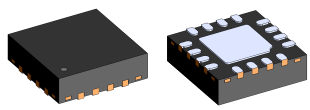
FEATURES

- Integrated Hall sensors with automatic gain and offset control
- Current consumption of only 2 µA to 30 µA in typ. applications
- Tracking speed of up to 120 000 rpm
- Configurable multiturn counting up to 40 bits
- Octal encoder mode (singleturn) with 3-bit parallel output
- Shift-register input for singleturn position
- Shift-register output of synchronized MT/ST position
- SSI multiturn data output with error, parity and sync. bits
- Adjustable multiturn preset value
- Pin-triggered preset and boot-up from external EEPROM
- I^{2}C multimaster interface to read EEPROM
- Supply voltage range of 3.0 V to 5.5 V
- Integrated supply switching to backup battery
- Error output on overspeed, low battery and CRC failure
- Space-saving 16-pin QFN package

APPLICATIONS

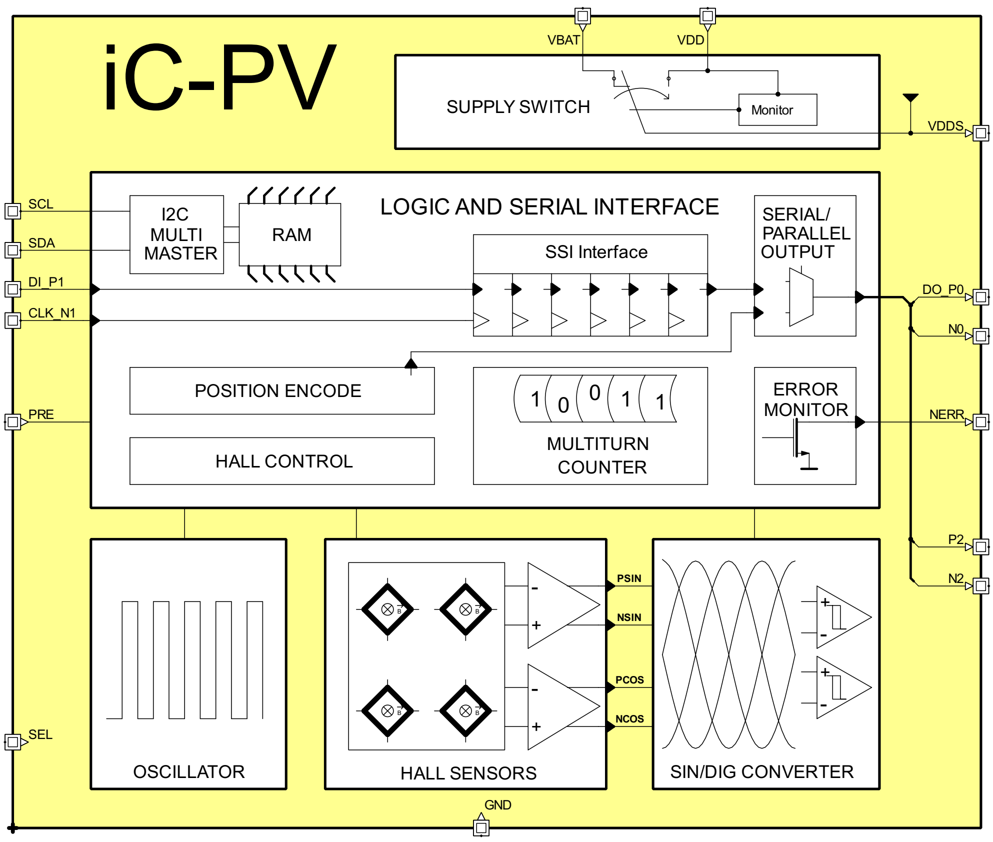
- Gearless revolution counting
- Multiturn encoders
- Absolute end-of-shaft encoders
- Period counters
- Metering applications

PACKAGES



QFN16
3 mm x 3 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-PV is an ultra low power magnetic multiturn encoder with up to 40 bit multiturn and 3 bit singleturn resolution, used for magnetic on-axis position sensing. On main power failure, the iC-PV switches to battery supply automatically and continues counting the correct multiturn position.

Together with an additional singleturn encoder iC (e.g. iC-MHM, iC-LG, iC-LNB, etc.) and a diametrically magnetized cylindrical permanent magnet it forms a complete multiturn encoder system. Depending on the used singleturn iC, a second magnetic or optical code disc might be mandatory. Furthermore the iC can function as a 3 bit parallel encoder. A multiturn encoder system can be built in combination with a microcontroller and an optional singleturn device.

The Hall signal processing stage is designed for ultra low power applications and can be configured to support angular accelerations up to 760 000 rad/s^2 at a maximum speed of 120 000 rpm. With higher demands on acceleration, the power consumption increases. The maximum supported acceleration is configurable, therefore an optimal trade-off between power consumption and supported acceleration can be individually chosen to meet the demands of the target application.

iC-PV reads its configuration from an external EEPROM via an I^2C interface with multimaster support. Among others, the bit length for multiturn and synchronization data, the interface mode, the maximum supported acceleration and the usage of error or parity bits can be configured. The configuration read-in is triggered by the preset pin PRE. A pulse on this pin resets the device and reads a new configuration from EEPROM. The multiturn counter is preset to a configurable value (default 0).

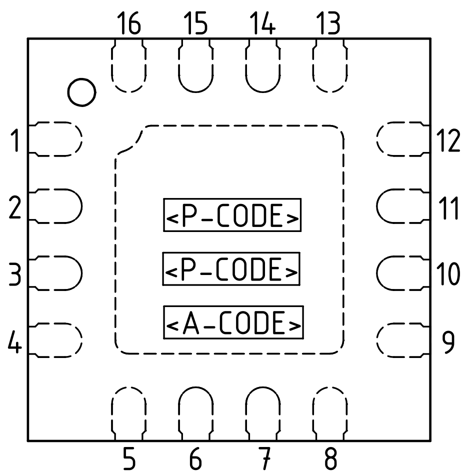
The configuration RAM and multiturn counter value are protected against bit errors by an 8 bit polynomial cyclic redundancy check. Additionally, an error is produced on excessive speed or acceleration. An integrated battery monitor can be used to signalize an empty battery as an error. A detected error is displayed via output NERR and is observable as an error bit in the SSI communication protocol.

While providing this wide range of functionality, the iC-PV multiturn encoder comes in a space-saving QFN16 package. This facilitates its integration in existing encoder systems or the design of new small encoders.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION
QFN16 3 mm x 3 mm (top view)

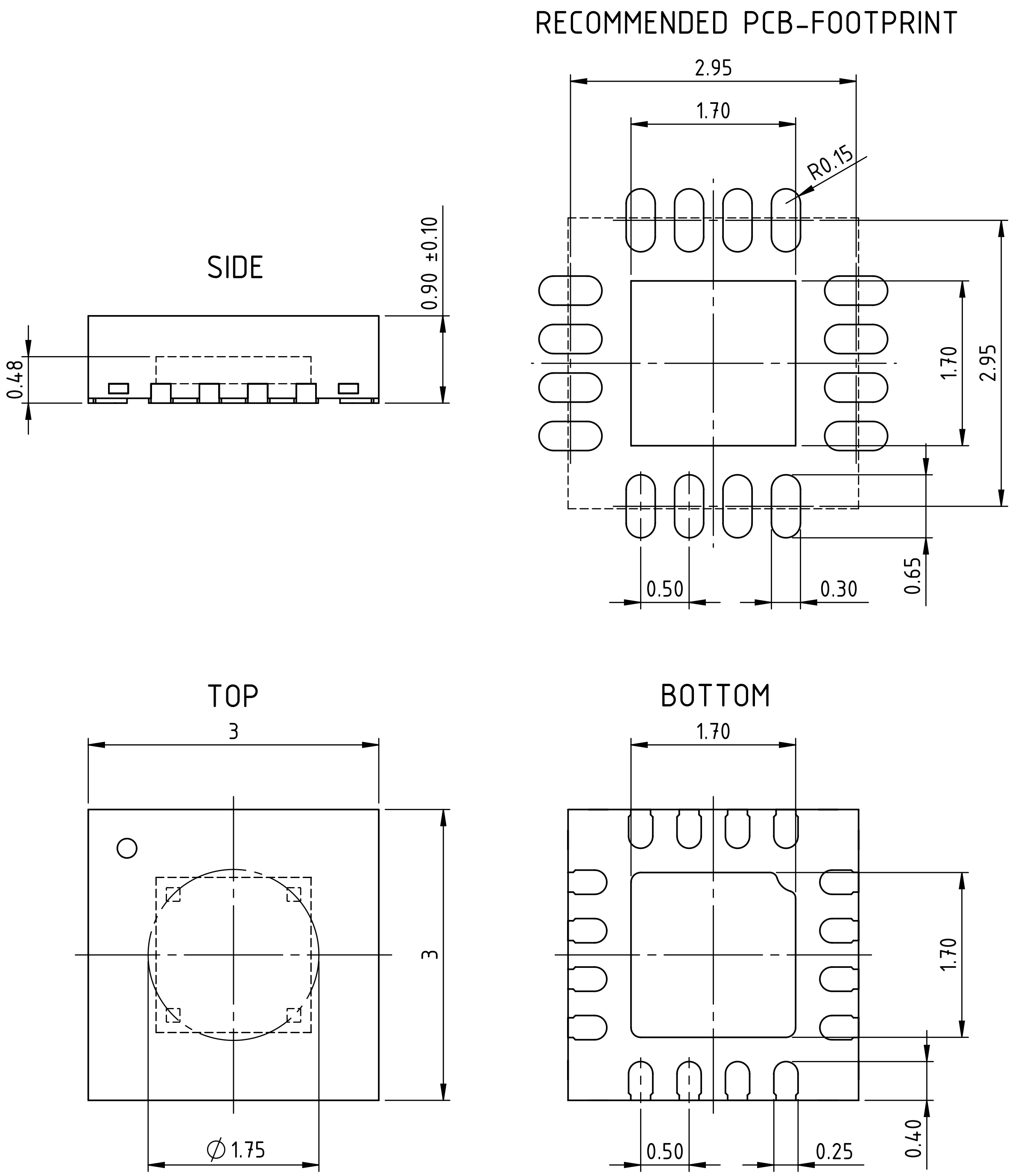


PIN FUNCTIONS

No.	Name	Function
1	SEL	Mode Select Input 1)
2	PRE	Preset Trigger Input
3	NERR	Error Monitor Output (active low)
4	SDA	EEPROM Interface, Data Line
5	GND	Ground
6	VBAT	Battery Supply Voltage (typ. 3.6 V)
7	VDDS	Switched Supply Voltage
8	VDD	+3.0...5.5 V Supply Voltage
9	N2	Parallel Output Bit 2 (negative logic)
10	P2	Parallel Output Bit 2 (positive logic)
11	N0	Parallel Output Bit 0 (negative logic)
12	n.c.	not connected
13	DO_P0	Multiturn Interface, Data Output and Parallel Output Bit 0 (positive logic)
14	CLK_N1	Multiturn Interface, Clock Line and Parallel Output Bit 1 (negative logic)
15	DI_P1	Multiturn Interface, Data Input and Parallel Output Bit 1 (positive logic)
16	SCL	EEPROM Interface, Clock Line
	BP	Backside paddle 2)

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Do not leave open. Low: Battery buffered counter with serial readout; High: 3 bit parallel complementary output
2) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS



All dimensions given in mm.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).
Tolerances of form and position according to JEDEC MO-220.

dra_qfn16-3x3-1_pv_y1_pack_1, 15:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V(VDD)	Supply Voltage at VDD	referenced to GND	-0.3	6	V
G002	V(VBAT)	Supply Voltage at VBAT	referenced to GND, if VDD > Von: VBAT < VDD + 1 V	-0.3	6	V
G003	V(VDDS)	Voltage at VDDS	referenced to GND	-0.3	6	V
G004	V()	Voltage at SCL, SDA, DI_P1, CLK_N1, DO_P0, N0, NERR, P2, N2, PRE, SEL	referenced to GND	-0.3	6	V
G005	I(VDD)	Current in VDD		-10	50	mA
G006	I(VBAT)	Current in VBAT		-10	50	mA
G007	I(VDDS)	Current in VDDS		-10	50	mA
G008	I(GND)	Current in GND		-50	10	mA
G009	I()	Current in SCL, SDA, DI_P1, CLK_N1, DO_P0, N0, NERR, P2, N2, PRE, SEL		-30	30	mA
G010	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Junction Temperature		-40	150	°C
G012	Ts	Storage Temperature Range	see package specifications	-40	150	°C

THERMAL DATA

Operating conditions: VDD = 3.0...5.5 V; VBAT = 3.0...5.0 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	Package QFN16	-40		125	°C
T02	Rthja	Thermal Resistance Chip/Ambience	QFN16-3x3 surface mounted to PCB according to JEDEC 51 thermal measurement standards		45		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 3.0...5.5 V, VBAT < VDD + 1 V, Tj = -40...125 °C, fslow calibrated to 8.5 kHz with IBIAS, 3 mm Ø NdFeB magnet, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	V(VDD)	Permissible Main Supply Voltage		3.0		5.5	V
002	I(VDD)	Supply Current in VDD	Tj = 27 °C, no load	1.0	3.0	5.0	mA
003	V(VBAT)	Permissible Battery Voltage	If VDD > Von: VBAT < VDD + 1 V	3.0	3.6	5.5	V
004	Iavg(VBAT)	Average Supply Current in VBAT	VBAT = 3.6 V, Tj = 27 °C, V(PRE) < 0.5 V	1	< 10	100	µA
005	Ispike()	Current Spikes in VDD and VBAT	Spikes < 5 µs		4.0	10.0	mA
006	Vc()hi	Clamp-Voltage hi at all pins	Vc()hi = V() - VDDS, I() = +1 mA	0.3	0.7	1.6	V
007	Vc()lo	Clamp-Voltage lo at all pins	I() = -1 mA	-1.6	-0.7	-0.3	V
008	tconfig	Power up Time After Preset	V(VDD) > 3 V, EEPROM data valid		12	20	ms
Hall Sensors							
101	Hsurf	Operating Magnetic Field Strength	at chip surface	10		100	kA/m
102	fmag	Magnetic Input Frequency	VDDS = 3.0 V, tested via electrical input			2 000	Hz
103	frot	Permissible Rotation Speed of Magnet	VDDS = 3.0 V, tested via electrical input			120 000	rpm
104	dsens	Diameter of Hall Sensor Circle	measured from center of each Hall plate		1.75		mm
105	AArel	Relative Angle Accuracy	referred to position output LSB = 45 °	-25		+25	%
106	hpac	Sensor-to-Package-Surface Distance	QFN16		0.4		mm
107	hmag	Permissible Sensor-to-Magnet Distance	3 mm diameter diametrical magnet (NdFeB), room temperature, see Table 22			4.0	mm
108	TOLrad	Permissible Radial Displacement	center of chip vs. center of axis, see Table 22			1.0	mm
109	TOLtan	Permissible Tangential Displacement (Chip Tilt)	chip to magnet coplanarity			5.0	°
Oscillators							
301	fslow	Slow Oscillator Frequency	calibrated to 8.5 kHz with IBIAS	8.0	8.5	9.0	kHz
302	ffast	Fast Oscillator Frequency	fslow calibrated with IBIAS	3.5	5.0	6.5	MHz
Supply Switch and Battery Monitoring							
401	Von	Switch to VDD Supply (VDD Power on)	increasing voltage at VDD; VBAT > 3.0 V	2.8	2.9	3.0	V
402	Voff	Switch Back to Battery Supply (VDD Power off)	decreasing voltage at VDD; VBAT > 3.0 V	2.7	2.8	2.95	V
403	Vhys	Hysteresis (VDD Switch)	Vhys = Von - Voff	25	100	150	mV
404	Vth_bat	Battery Monitoring Error Threshold Voltage		2.65	2.75	2.85	V
Digital Outputs: DI_P1, CLK_N1, DO_P0, N0, P2, N2							
501	Vs()hi	Saturation Voltage hi	Vs()hi = VDDS - V(), I() = -1.6 mA	0.05		0.4	V
502	Vs()lo	Saturation Voltage lo	I() = 1.6 mA	0.05		0.4	V
503	Isc()hi	Short-Circuit Current hi	VDDS = 3.0 V, V() = GND	-15		-4	mA
504	Isc()lo	Short-Circuit Current lo	VDDS = 3.0 V, V() = VDDS	4		15	mA
EEPROM Interface: SCL, SDA							
601	Vt()hi	Threshold Voltage hi			1.7	2	V
602	Vt()lo	Threshold Voltage lo		0.8	1.4		V
603	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	75	200	500	mV
604	Vs()lo	Saturation Voltage lo	I() = 1.6 mA	0.05		0.4	V
605	Isc()lo	Short-Circuit Current lo	VDDS = 3.0 V, V() = VDDS	8		30	mA
606	Ipu()	Pull-up Current at SCL and SDA	V() = 0 V ... VDDS - 1 V	-950	-300	-30	µA
607	fscl	I^2C Frequency at SCL			$f_{fast}/128$		kHz
Error Monitoring Output: NERR							
701	Vs()lo	Saturation Voltage lo	I() = 1.6 mA	0.05		0.4	V

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 3.0...5.5 V, VBAT < VDD + 1 V, Tj = -40...125 °C, fslow calibrated to 8.5 kHz with IBIAS, 3 mm Ø NdFeB magnet, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
702	Isc()lo	Short-Circuit Current lo	VDDS = 3.0 V, V() = VDDS	4		15	mA
Digital Inputs: DI_P1, CLK_N1							
801	Vt()hi	Threshold Voltage hi			1.7	2	V
802	Vt()lo	Threshold Voltage lo		0.8	1.4		V
803	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	75	200	500	mV
804	Ipd()	Pull-down Current	V() = 1 V ... VDDS	2	30	100	µA
806	fclk	Clock Frequency at CLK_N1				4	MHz
Mode Select Input: SEL							
901	Vt()hi	Threshold Voltage hi			1.7	2	V
902	Vt()lo	Threshold Voltage lo		0.8	1.4		V
903	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	75	200	500	mV
Preset Trigger Input: PRE							
A01	Vt()hi	Threshold Voltage hi			60	75	%VDD
A02	Vt()lo	Threshold Voltage lo		30	40		%VDD
A03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	0.7	1.0	1.4	V
A04	Ipd()	Pull-down Current	V() = 1 V ... VDDS, SEL = GND	10	120	300	µA
Serial Interface, SSI and CHAIN Mode							
B01	tphase	Propagation Delay: Clock Edge vs. DO Output		10		100	ns
B02	tout	Timeout	fslow calibrated with IBIAS	15	25	40	µs
Parallel Output Mode							
C01	tprocess	Processing Time (Parallel Output)	see Figure 10		10	30	µs

OPERATING REQUIREMENTS: Serial and Parallel Interface

Operating conditions: VDD = 3.0...5.5 V, VBAT < VDD + 1 V, Tj = -40...125 °C, fslow calibrated to 8.5 kHz with IBIAS, 3 mm Ø NdFeB magnet, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Serial Interface to Singleturn Sensor in SSI-Mode (INT_MODE = 0)						
I001	tpowr	Delay Power up to SSI Request		20		μs
I002	treq	Request Signal lo Level Duration		50		ns
I003	tperiod	Permissible Clock Period		0.25	$2 \cdot t_{out}$	μs
I005	thi	Clock Signal hi Level Duration		50		ns
I006	tlo	Clock Signal lo Level Duration		50		ns
I007	tcycle	Cyclic Multiturn Data Request Interval		85		μs
Serial Interface to Singleturn Sensor in CHAIN-Mode (INT_MODE = 1)						
I008	tpowup	Delay Power up to SSI Request		20		μs
I009	tperiod	Permissible Clock Period		0.25	$2 \cdot t_{out}$	μs
Parallel Output Mode						
I011	tstart	Length of Start Pulse on PRE Pin	see Figure 10	1		μs
I012	tcycle	Time between two Consecutive Sensor Read Cycles	see Figure 10	30		μs

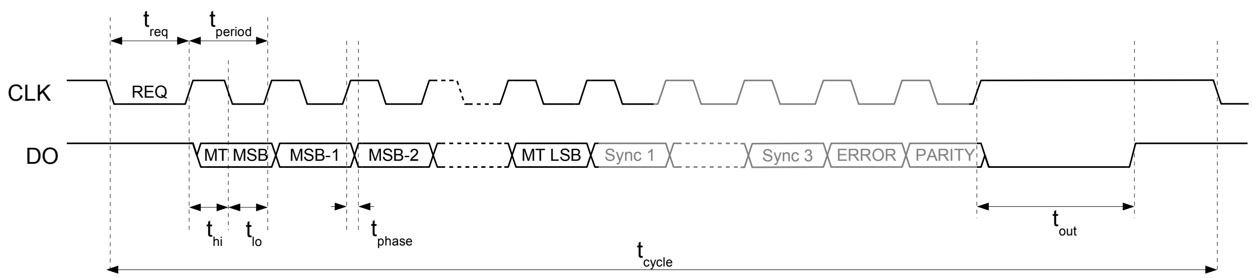


Figure 1: I/O line signals of the serial interface in SSI mode (INT_MODE = 0).

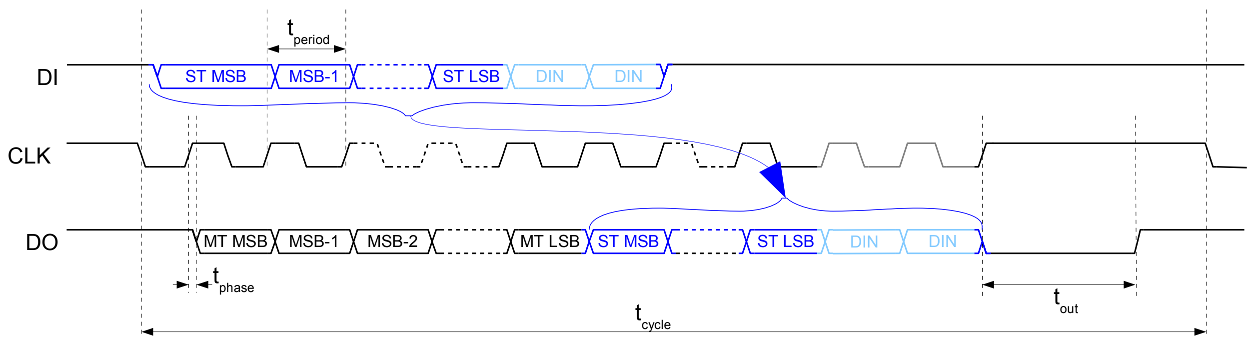


Figure 2: I/O line signals of the serial interface in chain mode (INT_MODE = 1).

CONFIGURATION PARAMETERS

Hall Sensor Conditioning
DIR: Code Direction (P. 12)
OS: Angle Offset (P. 12)

Serial Interface
INT_MODE: Serial Interface Operating Mode (P. 14)
ST_GRAY: Singleturn Input Data Format (P. 14)
MT_GRAY: Multiturn Output Data Format (P. 14)
MT_BW: Multiturn Bit Width (P. 14)
SYNC_BW: Synchronization Bit Width (P. 14)
ST_BW: Singleturn Input Bit Width (P. 14)
EN_ERR: Error Bit Enable (P. 15)
EN_PAR: Parity Bit Enable (P. 15)

Multiturn Counter
MT_PREL: Multiturn Preload Value (P. 16)

EEPROM CRC
CRC_CFG: Checksum for Chip Configuration (0x00-0x03) (P. 17)
CRC_CTR: Checksum for MT Counter Preload (0x05-0x09) (P. 17)

Supply Switch and Battery Monitoring
EN_BAT_MON:
Battery Monitoring Enable (P. 18)

Bias and Oscillator Calibration
IBIAS: Bias Current Calibration (P. 18)
A_MAX: Maximum Angular Acceleration (P. 19)

REGISTER MAP (iC-PV and EEPROM)

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interface and Hall Signal Processing								
0x00	EN_PAR		EN_ERR		DIR	ST_GRAY	MT_GRAY	INT_MODE
0x01	OS_MT2ST			MT_BW				
0x02	0	0	ST_BW				SYNC_BW	
Oscillator Configuration								
0x03	0	EN_BAT_MON	A_MAX			IBIAS		
CRC Configuration								
0x04	CRC_CFG(7:0)							
Counter Preload								
0x05	MT_PREL(7:0)							
0x06	MT_PREL(15:8)							
0x07	MT_PREL(23:16)							
0x08	MT_PREL(31:24)							
0x09	MT_PREL(39:32)							
CRC Counter								
0x0A	CRC_CTR(7:0)							
Note: Reserved registers must be programmed to zero.								

Table 5: Register layout

SENSOR PRINCIPLE

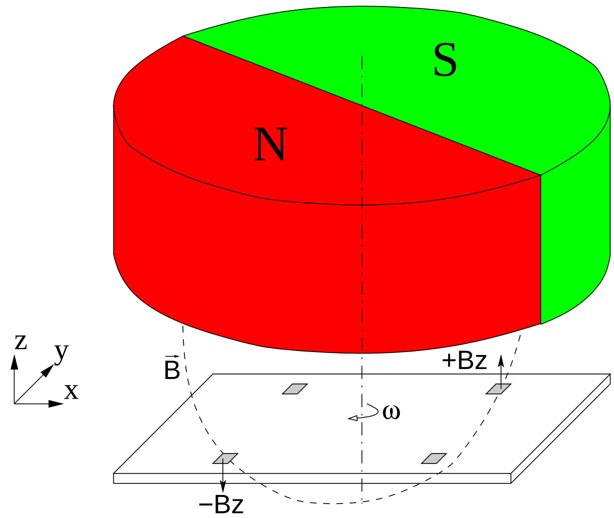


Figure 3: Sensor principle

In conjunction with a rotating permanent magnet, the iC-PV can be used to create a complete (multiturn) encoder system. A diametrically magnetized, cylindrical permanent magnet made of neodymium iron boron (NdFeB) or samarium cobalt (SmCo) generates optimum sensor signals. The diameter of the magnet should be between 2 to 8 mm.

The iC-PV has four Hall sensors adapted for angle determination and to convert the magnetic field into a measurable Hall voltage. Only the z-component of the magnetic field is evaluated, whereby the field lines pass through two opposing Hall sensors in the opposite direction. Figure 3 shows an example of field vectors. The arrangement of the Hall sensors is selected so that the mounting of the magnets relative to iC-PV is extremely tolerant. Two Hall sensors combined provide a differential Hall signal. When the magnet is rotated around the longitudinal axis, sine and cosine output voltages are produced, which can be used to determine the current angle.

In combination with a digital counter, this angle information is used to determine the absolute (multiturn) position, i.e., the iC-PV counts the revolutions of the permanent magnet.

POSITION OF THE HALL SENSORS

The Hall sensors are placed in the center of the QFN16 package at 90 ° to one another and arranged in a circle with a diameter of 1.75 mm as shown in Figure 4.

In order to calculate the angle position of a diametrically polarized magnet placed above the device, a difference in signal is formed between opposite pairs of Hall sensors, resulting in the sine being $V_{SIN} = V_{PSIN} - V_{NSIN}$ and the cosine $V_{COS} = V_{PCOS} - V_{NCOS}$. The zero angle position of the magnet is marked by the resulting cosine voltage value being at a maximum and the sine voltage value at zero.

In this case, the south pole of the magnet is exactly above the PCOS sensor and the north pole is above sensor NCOS, as shown in Figure 5. Sensors PSIN and NSIN are placed along the pole boundary so that neither generate a Hall signal.

When the magnet is rotated counterclockwise, the poles also cover the PSIN and NSIN sensors, resulting in the sine and cosine signals shown in Figure 6.

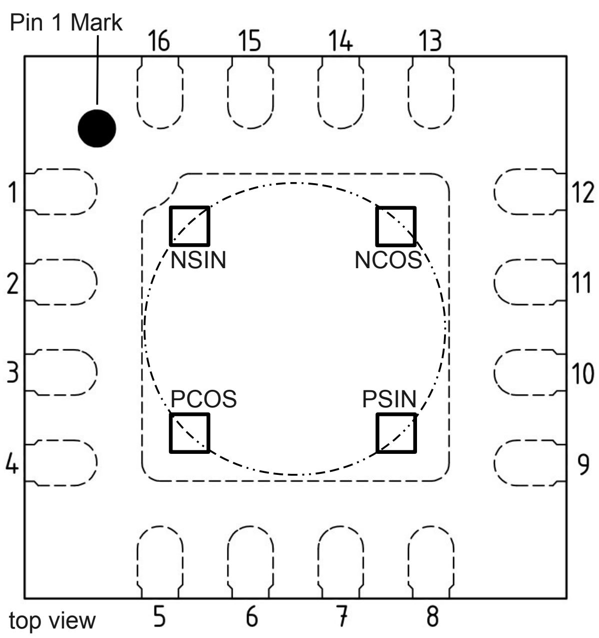


Figure 4: Position of the Hall sensors

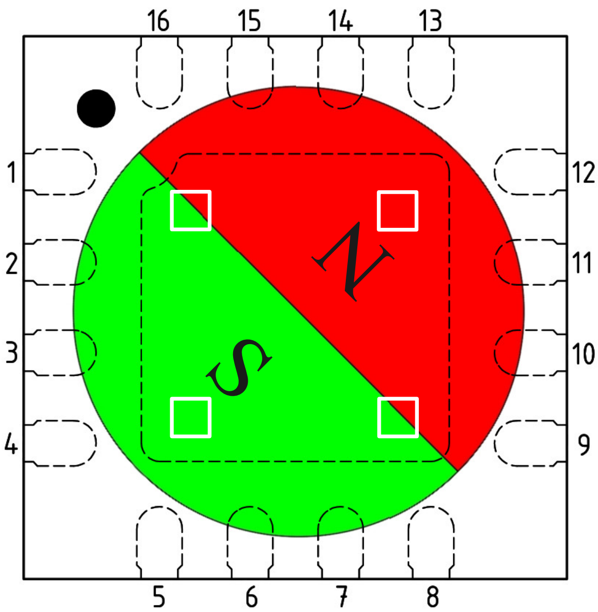


Figure 5: Magnet zero position (top view)

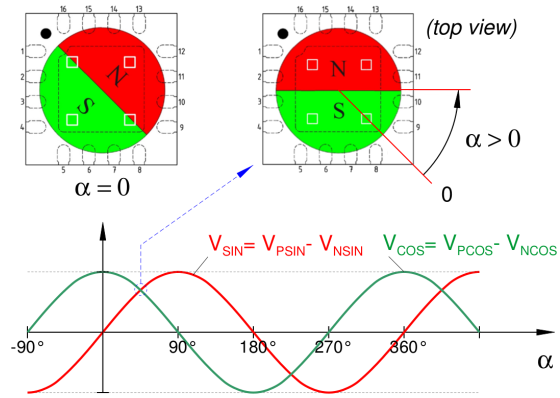


Figure 6: Pattern of analog sensor signals with corresponding angle of rotation

HALL SENSOR CONDITIONING: ANGLE OFFSET AND CODE DIRECTION

Assembled together with a diametrically polarized magnet, the integrated Hall sensor signal processing generates a 3 bit position word. Therefore, the iC-PV can deliver up to 3 synchronization bits to the singleturn sensor in SSI readout mode.

OS	Addr. 0x01; bit 7:5
Code	Phase shift
000	0 °, no shift
001	+45 ° leading
010	+90 ° leading
011	+135 ° leading
100	-180 ° leading or trailing
101	-135 ° trailing
110	-90 ° trailing
111	-45 ° trailing

Table 6: Angle offset

When the phase relationship between an additional singleturn iC and the iC-PV as multiturn encoder is unknown, or the singleturn sensor takes care of the synchronization (SSI mode) and expects a defined relationship, the position can be electrically manipulated to achieve the desired (leading or trailing) phase shift, regardless of the actual mounting position. An offset value is added to the digitized Hall sensor position according to parameter OS.

In applications where the chain operation mode is used (see Page 14), the iC-PV takes care of synchronization. Therefore, it has to be mounted leading in relation to the singleturn iC. The OS parameter can be used to achieve this phase shift on random mounting displacements. To ensure correct synchronization of multiturn and singleturn data, the resulting phase shift between multiturn and singleturn position must be in range 0 ° to 180 ° (MT leading)*.

DIR	Addr. 0x00; bit 3
Code	Direction
0	Normal
1	Inverted

Table 7: Code direction

For assembly situations were the mounting direction of the magnet is not known, the counting direction can be easily swapped with the configuration bit DIR. The bit would be typically used to invert the counting directions in applications where the iC-PV is assembled on the back side of a PCB.

* 0 ° to 180 ° is the ideal range for tolerated values of phase shift between ST and MT. This range is further reduced due to communication, propagation or processing delays for the specific application. Typically, it is reduced by few degrees, increasing with rotational velocity.

MODE SELECT INPUT SEL

The input SEL defines the operating mode of iC-PV. For the default application as battery buffered multiturn counter with serial position readout, it is mandatory to connect the SEL input to GND potential. In case a 3 bit parallel and differential position output is desired, a high state at SEL input selects the parallel mode. It is mandatory to connect SEL to a defined high or low potential.

MODE SELECT INPUT SEL	
State	iC-PV Operating Mode
Low	Battery buffered counter with serial readout
High	3 bit parallel complementary output
Open	Not allowed

Table 8: Mode selection via SEL pin

STARTUP BEHAVIOR AND PRESET FUNCTION

The iC-PV can be boot-up in three distinct operating modes. These are the SSI interface mode, a chain interface mode and a parallel encoder mode, respectively. In case of a wrong startup procedure, an error is indicated at pin NERR.

Figure 7 shows the startup procedure of iC-PV. The procedure starts when a battery supply is available. This would be the case if a battery is newly attached to the encoder system or the battery supply is switched on by an external microcontroller.

Subsequent to powering up the VBAT pin, a preset pulse must be applied to the interface pin (PRE). This resets the internal circuitry to its default initial state. Via SEL, the operating mode is selected according to Table 8. If SEL = high, the chip functions as a 3 bit encoder with parallel complementary output and encodes the current position as shown in Figure 10.

If SEL = low and V(VDD) > V_{on} during startup, the preset pulse triggers EEPROM readout, therefore VDD supply has to remain above V_{on} for at least t_{config}. The I^2C multimaster tries to readout the configuration data from an EEPROM connected to SCL and SDA. If the data can be read without errors, the iC-PV operates in SSI interface mode or CHAIN interface mode according to the configuration bit INT_MODE and stays in this operating mode as long as the battery supply remains above V_{off}. After three erroneous attempts, EEPROM readout is stopped and an error is indicated via NERR pin.

In parallel encoder mode an external microcontroller activates the iC-PV in distinct intervals to acquire the current position. The encoded position is valid when all complementary bits have changed their logic value (see Figure 10). After successful position readout, the battery supply may be switched off. Otherwise, iC-PV remains in ultra low power idle mode.

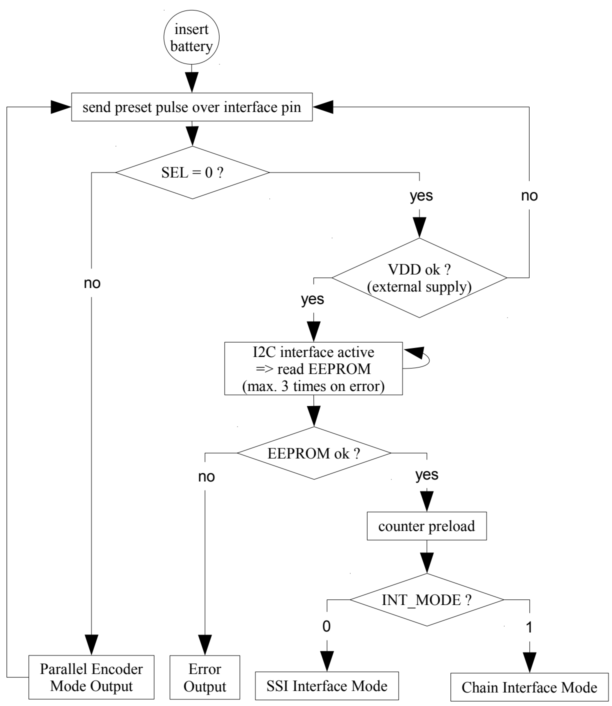


Figure 7: Startup behavior

SERIAL INTERFACE (SEL = LOW)

iC-PV can connect to an external singleturn sensor via a serial interface. To ensure compatibility with different types of singleturn sensors, the iC-PV's serial interface can operate in two distinct modes. These are a standard SSI conform operating mode and a chain mode, respectively.

In the SSI mode, the iC-PV expects an external singleturn sensor to request the multiturn data via a SSI protocol. The singleturn sensor takes care of synchronization and calculates a consistent absolute position. The data in pin (DI) is not used in this operating mode. iC-PV is compatible with all iC-Haus optical or magnetic singleturn encoders featuring a multiturn interface (MTI). For details please refer to application examples in Figure 12 up to Figure 15.
In this mode of operation, iC-PV can also be used as stand-alone magnetic revolution counter. The position can be read via a serial, SSI compatible protocol (see Figure 17).

In the chain mode, the singleturn sensor transmits the singleturn position first to the iC-PV via the data in pin (DI). In this configuration, the iC-PV takes care of synchronization, calculates a consistent absolute position and outputs it concurrently (MSB first) via the data out pin (DO), comparable to a shiftregister. An application example with iC-LNG as singleturn iC is shown in Figure 16.
The respective mode to operate in is set using parameter INT_MODE.

INT_MODE	Addr. 0x00; bit 0
Code	Mode
0	Standard SSI readout mode (SSI)
1	Chain mode (CHAIN)

Table 9: Serial interface operating mode

By default, the iC-PV expects the serial input at the data in pin (DI) to be binary. Similarly it outputs its counted multiturn position via DO in binary format. In case one of them or both are required to be in gray format, this can be configured by setting the ST_GRAY bit or the MT_GRAY bit, respectively.

ST_GRAY	Addr. 0x00; bit 2
Code	Format
0	Binary code
1	Gray code

Table 10: Singleturn input data format via pin DI

MT_GRAY	Addr. 0x00; bit 1
Code	Format
0	Binary code
1	Gray code

Table 11: Multiturn output data format via pin DO

The width of the internal multiturn counter is 40 bit. In applications where smaller counter depths are sufficient or are restricted by the bit width of the serial interface, the output length of the counter value can be configured with MT_BW as shown in Table 12.

MT_BW	Addr. 0x01; bit 4:0
Code	Bit width
0x00	9 bit
0x01	10 bit
.	...
0x1E	39 bit
0x1F	40 bit

Table 12: Multiturn bit width

Additionally iC-PV can transmit up to 3 synchronization bits, according to configuration parameter SYNC_BW shown in Table 13.

SYNC_BW	Addr. 0x02; bit 1:0	
Code	Bit width	Phase shift range
00	0 bit	no synchronization bit
01	1 bit	0°... 180°
10	2 bit	0°... 270°
11	3 bit	0°... 315°

Table 13: Synchronization bit width and resulting tolerable ideal phase shift

The singleturn bit width, iC-PV expects in chain mode at pin DI, can be configured in similar way with configuration parameter ST_BW (Table 14).

ST_BW	Addr. 0x02; bit 5:2
Code	Bit width
0x00	3 bit
0x01	4 bit
...	...
0x0F	18 bit

Table 14: Singleturn input bit width

After the transmission of the absolute position and the synchronization information, iC-PV's serial protocol allows the optional transmission of an error bit and a parity bit. The error bit signalizes errors occurred during startup phase, wrong CRC checksums, low battery or exceeded maximum rotary speed. Its polarity is configured with parameter EN_ERR shown in Table 15. The optional parity bit finishes the transmission. Its polarity is either even or odd according to parameter EN_PAR (Table 16).

EN_ERR	Addr. 0x00; bit 5:4
Code	Mode
00	Communication without error bit
01	Calibration mode and iC-Haus internal use only
10	Communication with additional error bit (negative polarity)
11	Communication with additional error bit (positive polarity)

Table 15: Enable error bit transmission

EN_PAR	Addr. 0x00; bit 7:6
Code	Mode
00	Communication without parity bit
01	iC-Haus internal use only
10	Communication with additional parity bit (even polarity)
11	Communication with additional parity bit (odd polarity)

Table 16: Enable parity bit transmission

The line signals for both interface modes are shown in Figure 8 and 9. Optional bits are drawn in light gray. The number of transmitted multiturn and singleturn bits depends on parameter MT_BW and ST_BW.

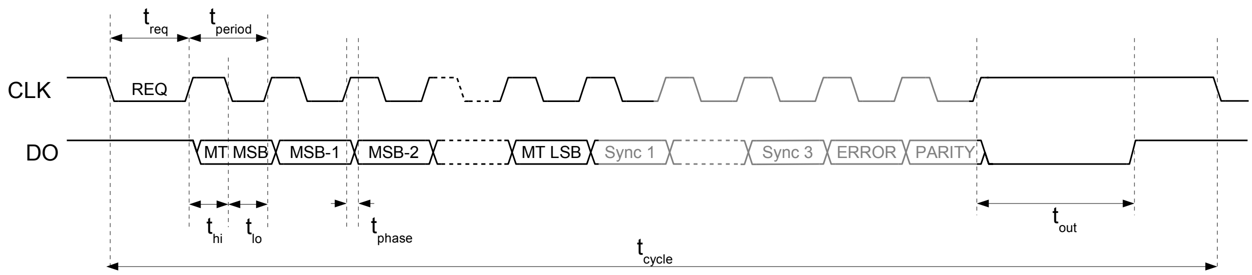


Figure 8: I/O line signals of the serial interface in SSI mode (INT_MODE = 0).

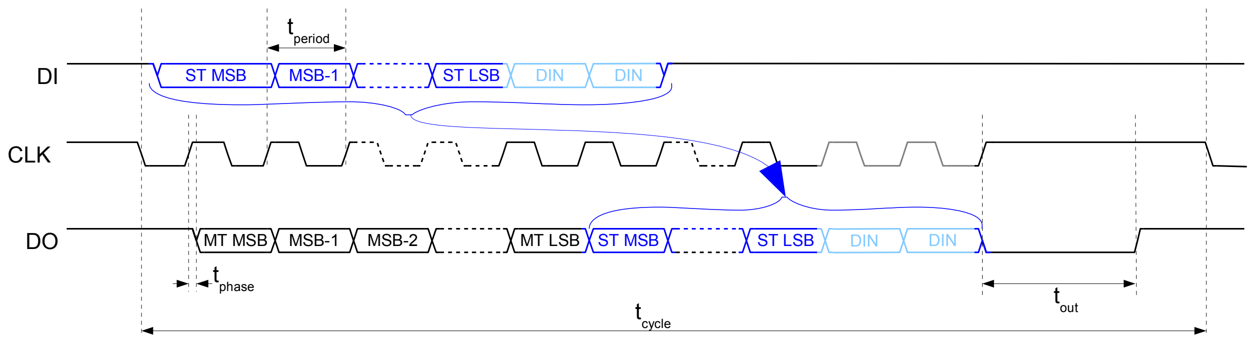


Figure 9: I/O line signals of the serial interface in chain mode (INT_MODE = 1).

PARALLEL MODE (SEL = HIGH)

The input/output behavior in parallel mode is described in Figure 10. A start pulse on the PRE line triggers the Hall sensor signal acquisition. The current position is sent as a 3 bit complementary word via pins P0, N0 to P2, N2. In this application, the iC-PV operates with a single power supply on pin VBAT. The pin VDD must be tied to GND in this mode, the select input SEL needs to be connected to a logic high potential, e.g. VBAT.

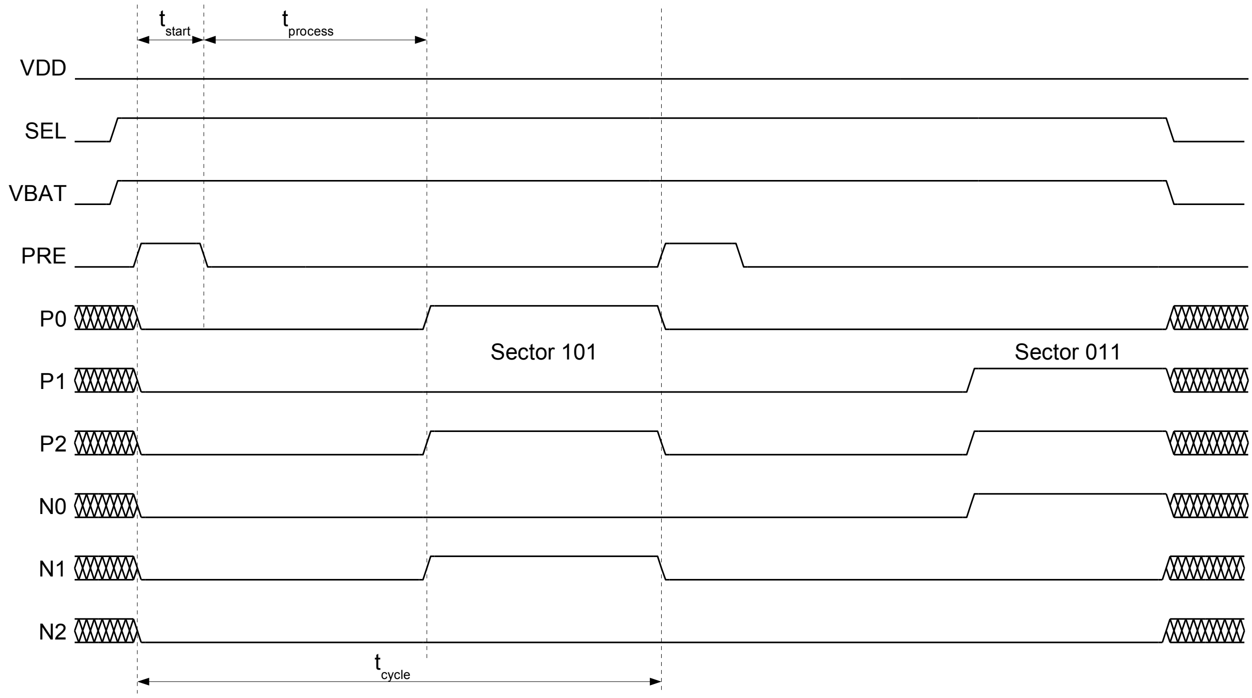


Figure 10: Line signals for parallel mode (3 bit complementary P0-P2 and N0-N2).

MULTITURN COUNTER

In battery buffered serial interface mode (SEL = low) and as long as the system is powered up correctly (battery or external supply), it will count the multiturn position up to $2^{MT\_BW} - 1$ revolutions. There is no counter overflow handling (positive or negative direction). The counter can be preloaded to a position given in configuration parameter MT_PREL as described in Table 17. The counter bit width is configured as described in Table 12.

The multiturn counter value as well as the configuration RAM are secured by an 8 bit polynomial cyclic redundancy check. Details can be found in the subsequent EEPROM paragraph.

MT_PREL	Addr. 0x09 - 0x05;
Code	Value
0x0000000000	0
0x0000000001	1
...	...
0x00000000FF	255
...	...
0xFFFFFFFFFF	$2^{40} - 1$

Table 17: Multiturn preload value

I2C MULTIMASTER INTERFACE TO EEPROM INTERFACE AND CRC PROTECTION

Pins SCL and SDA form an interface which can be used to communicate (read-only) with an external EEPROM according to I^2C protocol (with at least 128 bytes, e.g. 24C01, 24C02, 24C08 and maximum 24C16, extended address range is not supported).

This EEPROM is used to store the iC-PV configuration (addresses 0x00 to 0x0A) according to the register map on Page 10. The configuration is protected against bit errors by an 8 bit polynomial cyclic redundancy check. CRC checksum failure is displayed via output NERR and as an error bit at the end of the SSI communication protocol. The multiturn counter preload value is stored in its own configuration area (0x05 - 0x09) and is also saved with its own CRC on 0x0A. The CRC for the remaining four configuration bytes (0x00 - 0x03) is stored at address 0x04. Both CRC checksums are generated with the polynomial $X^8 + X^5 + X^3 + X^2 + X^1 + 1$ (0x2F sometimes also named as 0x12F). The CRC start value is zero.

Since iC-PV does only read configuration data, the write access to EEPROM is done via external inline programming via pins SCL and SDA (I^2C protocol). The direct EEPROM access to I^2C lines is shown in the application schematic on Page 24. In applications with shared EEPROM, e.g. with iC-MHM, the EEPROM programming for iC-PV configuration can be done via the BiSS interface of the iC-MHM (see Figure 12).

If no EEPROM is available or desired in the application, programming the iC-PV with a microcontroller unit (MCU) is possible. Therefore, the MCU has to emulate an I^2C slave, since iC-PV is acting as a bus master only. At startup, after a short high pulse at pin PRE, the iC-PV request the address 0x00 to 0x0A from the connected I^2C slave. This is done in a combined write/read command as shown in Figure 11. The shown sequence is repeated 11 times.

The expected slave address is 0x50 or "101 0000", the standard I^2C slave EEPROM address.

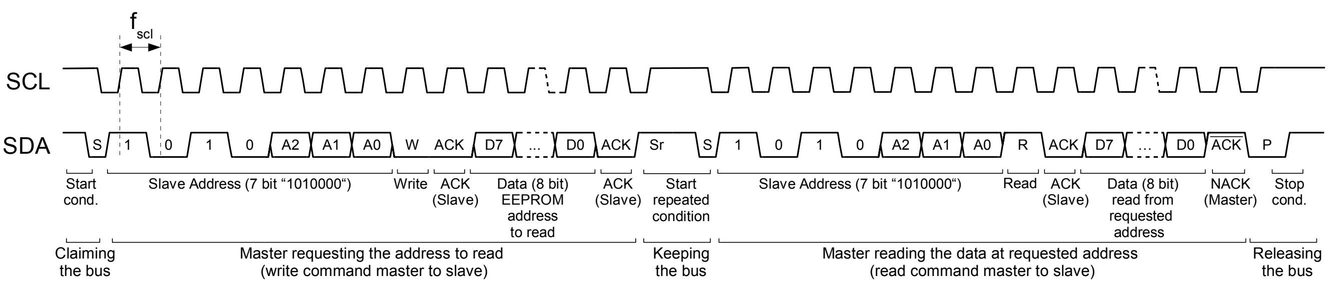


Figure 11: iC-PV combined write/read command reading one slave address.

SUPPLY SWITCH AND BATTERY MONITORING

To retain and acquire the absolute position even on main power failure, the iC-PV switches from VDD to a battery supply on pin VBAT. The switching point lies just below 3 V. So if the main supply voltage on VDD drops below 3 V, the internal circuitry will be powered by VBAT instead of VDD.

The supply switch has a build in hysteresis. The threshold voltages are defined in the electrical characteristics section named V_{off} (Item No. 402), i.e. the voltage at which the circuit switches from VDD supply to VBAT supply and V_{on} (Item No. 401), the voltage at which the circuit switches back to VDD.

Depending on the used energy storage, e.g. a 3.6 V battery with 1 Ah capacity, the device can operate for several years. The iC-PV monitors the voltage at pin VBAT to detect a low battery voltage. If it drops below a defined error threshold voltage (Item No. 404), an error is generated and signalized via pin NERR and as error bit in the SSI communication protocol. The battery monitoring function can be enabled/disabled with configuration parameter EN_BAT_MON as show in Table 18.

EN_BAT_MON	Addr. 0x03; bit 6
Code	Function
0	Battery monitoring off
1	Battery monitoring on

Table 18: Enable or disable the internal battery monitor.

BIAS AND OSCILLATOR CALIBRATION

The bias current for the internal oscillator can be configured with the configuration parameter IBIAS. An increase or decrease in bias current will directly influence the oscillator frequency. The bias current should be calibrated at the typical battery supply voltage so that the frequency of the oscillator is around 8.5 kHz (see Item No. 301). The clock frequency is observable in the dedicated calibration mode. The calibration mode is entered by configuring the EN_ERR parameter to "01" (see Table 15). The oscillator clock is then output on pin DI_P1.

IBIAS	Addr. 0x03; bit 2:0
Code	Frequency change
100	+20 %
101	+10 %
110	0 %
111	-10 %
000	-20 %
001	-30 %
010	-40 %
011	-50 %

Table 19: Bias current; oscillator frequency calibration.

CALCULATING CURRENT CONSUMPTION

Interface Mode (SEL = LOW)
The current consumption of the iC-PV can be configured by parameter A_MAX. Besides the current consumption, this parameter sets the maximum angle acceleration (from shaft halt) supported by the iC-PV in the respective configuration. The relationship between maximum acceleration and current consumption is shown in Table 20. For accelerations below $48 \cdot 10^3 rad/s^2$, the typical current consumption lies below 10 μA.

For applications were only sporadic motor movement is expected during battery supply, Table 20 mainly defines the current consumed by iC-PV. Additionally, Table 21 gives typical values in case of enduring movement at a certain angular velocity.

A_MAX	Addr. 0x03; bit 5:3			
Code	α_{max} $[\frac{\circ}{s^2}]$	α_{max} $[\frac{rad}{s^2}]$	typ. $I_{avg}[\mu A]$	max. $I_{avg}[\mu A]$
000	$40 \cdot 10^6$	$760 \cdot 10^3$	26	36
001	$10 \cdot 10^6$	$190 \cdot 10^3$	14	18
010	$2.5 \cdot 10^6$	$48 \cdot 10^3$	7	10
011	$625 \cdot 10^3$	$12 \cdot 10^3$	4	6
100	$160 \cdot 10^3$	$3 \cdot 10^3$	2.5	4
101	$40 \cdot 10^3$	$0.75 \cdot 10^3$	2	3
110	$10 \cdot 10^3$	$0.2 \cdot 10^3$	1.5	2.5
111	reserved			

Table 20: Maximum supported angular acceleration (from shaft halt) and average current consumption on shaft halt or slow angular velocity. V(VBAT) = 3.6 V, V(PRE) < 0.5 V.

I(VBAT) for angular velocity [RPM]								
$f[RPM]$	$f[Hz]$	$I_{avg}[\mu A]$ A_{MAX} = 110	$I_{avg}[\mu A]$ A_{MAX} = 101	$I_{avg}[\mu A]$ A_{MAX} = 100	$I_{avg}[\mu A]$ A_{MAX} = 011	$I_{avg}[\mu A]$ A_{MAX} = 010	$I_{avg}[\mu A]$ A_{MAX} = 001	$I_{avg}[\mu A]$ A_{MAX} = 000
0	0	1.5	2	2.5	4	7	14	26
< 125	< 2	1.5	2	2.5	4	7	14	26
< 250	< 4	2	2	2.5	4	7	14	26
< 500	< 8	2.5	2.5	2.5	4	7	14	26
< 1000	< 16	4	4	4	4	7	14	26
< 2000	< 33	7	7	7	7	7	14	26
< 4000	< 66	14	14	14	14	14	14	26
< 8000	< 133	26	26	26	26	26	26	26
< 16000	< 266	51	51	51	51	51	51	51

Table 21: Average current consumption vs. angular velocity. Typical values for V(VBAT) = 3.6 V, T_a = 25 °C and V(PRE) < 0.5 V.

Parallel Encoder Mode (SEL = HIGH)
The current consumption in parallel encoder mode is directly proportional to the sampling frequency, f_s. Lower sampling frequencies use less current and higher frequencies use more current. The typical mean value of current consumed by iC-PV, is calculated as shown below (V(VBAT) = 3.6 V, T_j = 25 °C) :

$$I_{avg}[\mu A] = 25 \cdot f_s[kHz]$$

For instance, at a sampling frequency of 1 000 samples per second, f_s = 1 kHz and I = 25 µA. At 100 samples per second, I = 2.5 µA.

APPLICATION NOTES: Operating distance sensor to magnet

The iC-PV is highly tolerant for assembly displacements between the magnet and the iC itself. The final setup has to meet the specified operating magnetic field strength (Item No. 101). Depending on the used magnet, this leads to different permissible sensor to magnet distances. For typical magnets made of NdFeB the operating distances are shown in Table 22. The third column defines the permissible radial displacement. The permissible tangential displacement (tilt error) is defined in Item No. 109.

Assembly tolerances sensor to magnet		
Ø Magnet	Distance	Radial Displacement
3 mm	up to 4.0 mm	up to 1.0 mm
4 mm	up to 6.0 mm	up to 1.5 mm
8 mm	up to 7.0 mm	up to 3.0 mm

Table 22: Assembly tolerances: Operating distance sensor to magnet and permissible radial displacement.

APPLICATION NOTES: Singleturn iCs with multiturn interface (SSI-Mode)

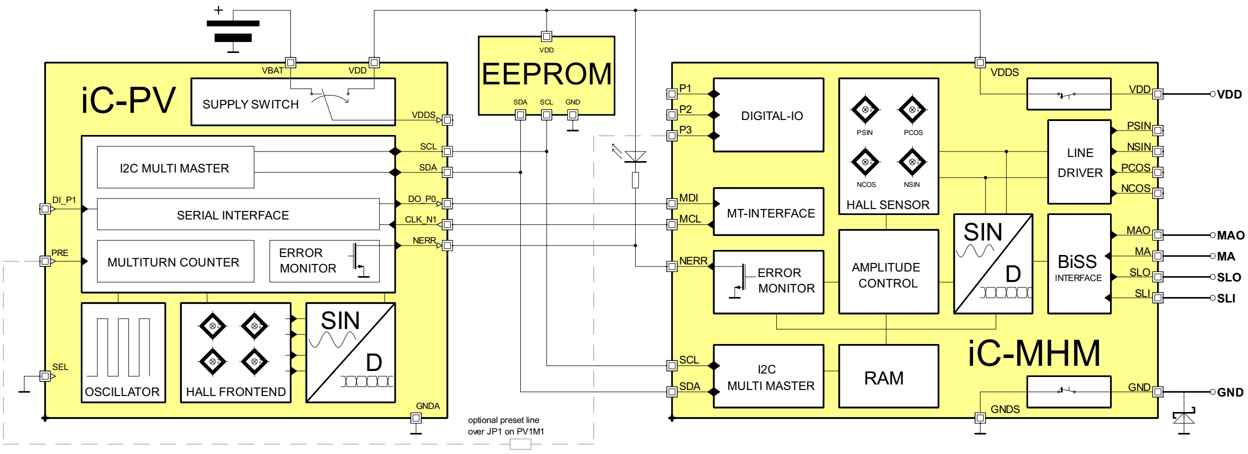


Figure 12: Application example iC-PV as battery-buffered multiturn device connected to the MT interface of the iC-MHM singleturn encoder. Interface operating in SSI-Mode (INT_MODE = 0). The two iC's share one common EEPROM for configuration. EEPROM is written via iC-MHM, BiSS register access. The position (MT + ST) is transmitted via the serial BiSS interface (please see iC-MHM specification for further details).

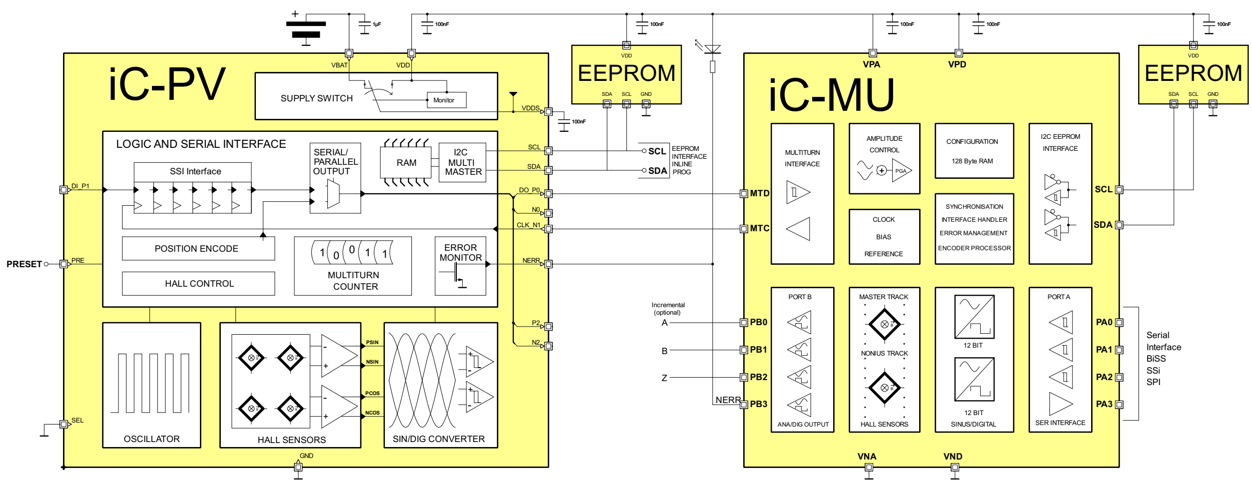


Figure 13: Application example iC-PV as battery-buffered multiturn device connected to the MT interface of the iC-MU absolute singleturn encoder. Interface operating in SSI-Mode (INT_MODE = 0). One EEPROM per iC mandatory for configuration. iC-PV EEPROM, direct access via SCL, SDA. BiSS, SPI and SSI are available for serial data transmission (please see iC-MU specification for further details).

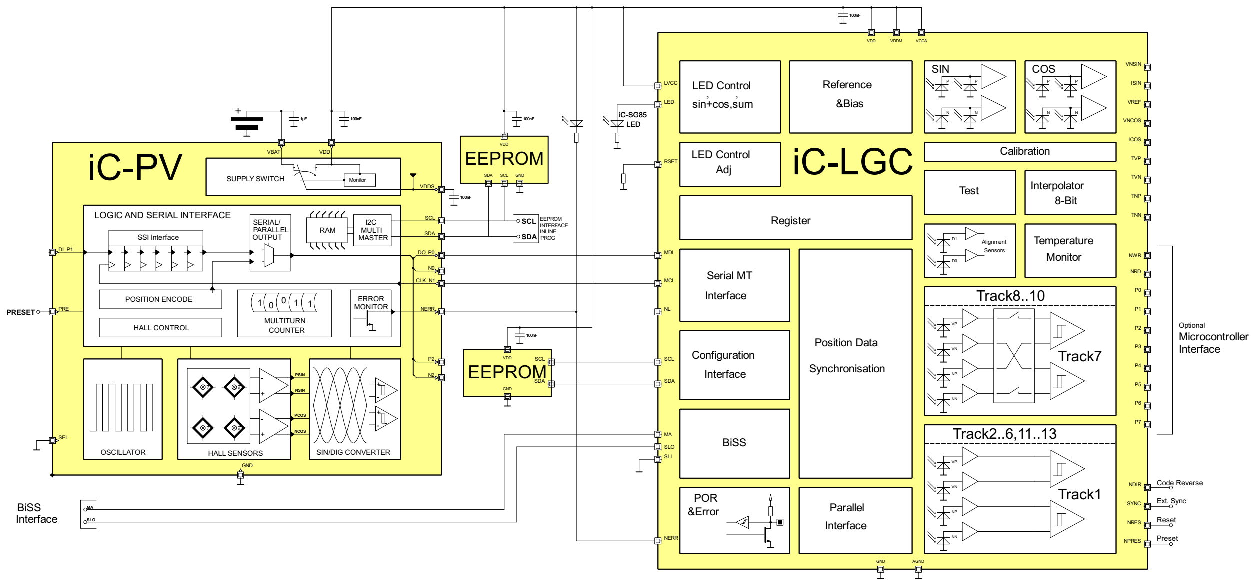


Figure 14: Application example iC-PV as battery-buffered multiturn device connected to the MT interface of the iC-LGC optical singleturn encoder. Interface operating in SSI-Mode (INT_MODE = 0). One EEPROM per iC mandatory for configuration. iC-PV EEPROM, direct access via SCL, SDA. BiSS, SPI and SSI are available for serial data transmission (please see iC-LGC specification for further details).

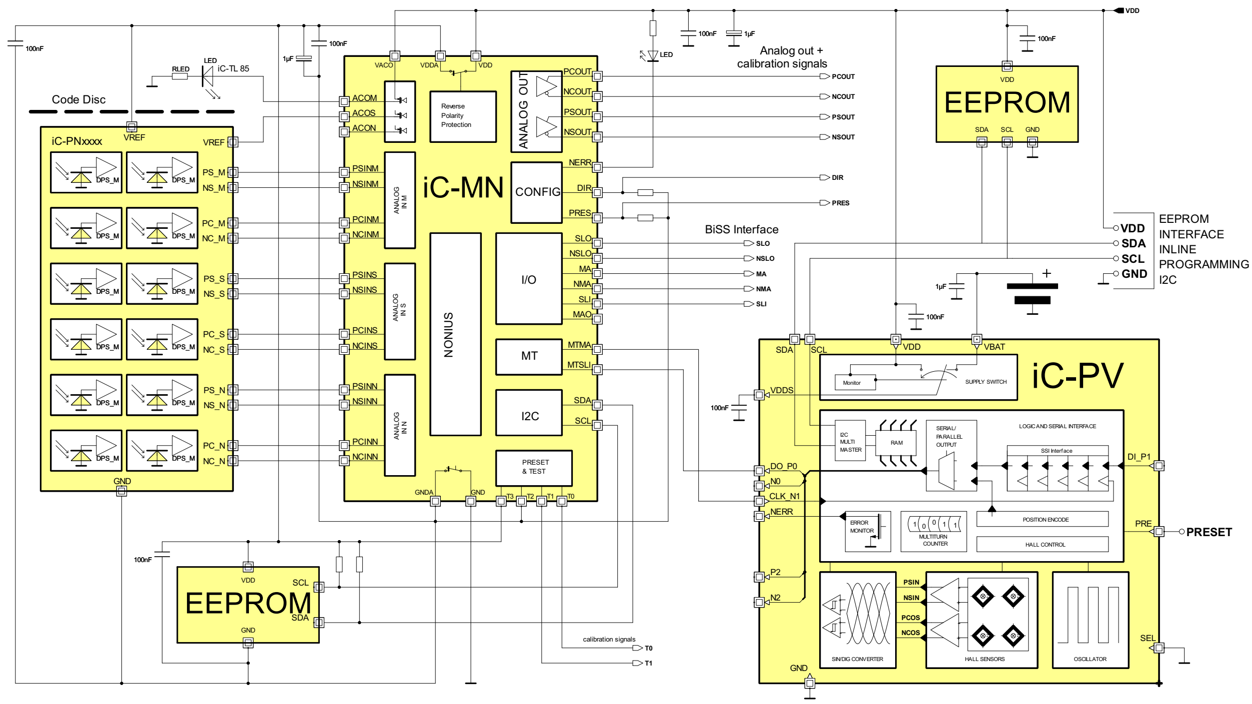


Figure 15: Application example iC-PV as battery-buffered multiturn device connected to the MT interface of the iC-MN nonius encoder (together with an iC-PN type phased array). iC-PV Interface operating in SSI-Mode (INT_MODE = 0). One EEPROM per iC mandatory for configuration. iC-PV EEPROM, direct access via SCL, SDA. BiSS or SSI are available for serial data transmission (please see iC-MN/PNxxxx specification for further details).

APPLICATION NOTES: Chain operating mode

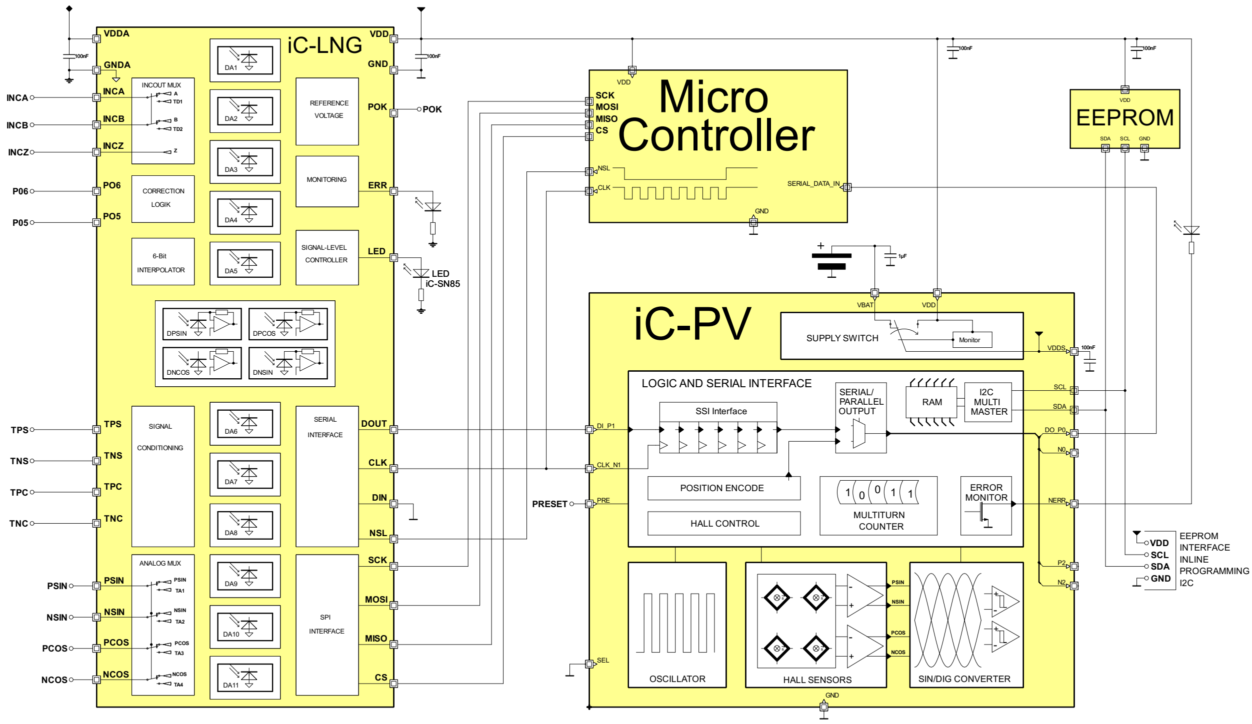


Figure 16: Application example iC-PV as battery-buffered multiturn device connected in chain mode (INT_MODE = 1) to the serial data output (DOUT) of the iC-LNG singleturn encoder. An external microcontroller is mandatory for position readout. iC-PV configuration via EEPROM, iC-LNG configuration via SPI interface by the microcontroller. iC-PV EEPROM, direct access over SCL, SDA. Instead of iC-LNG, iC-LNB could be used in this configuration (please see iC-LNG/LNB specification for further details).

APPLICATION NOTES: iC-PV as battery powered revolution counter or metering device

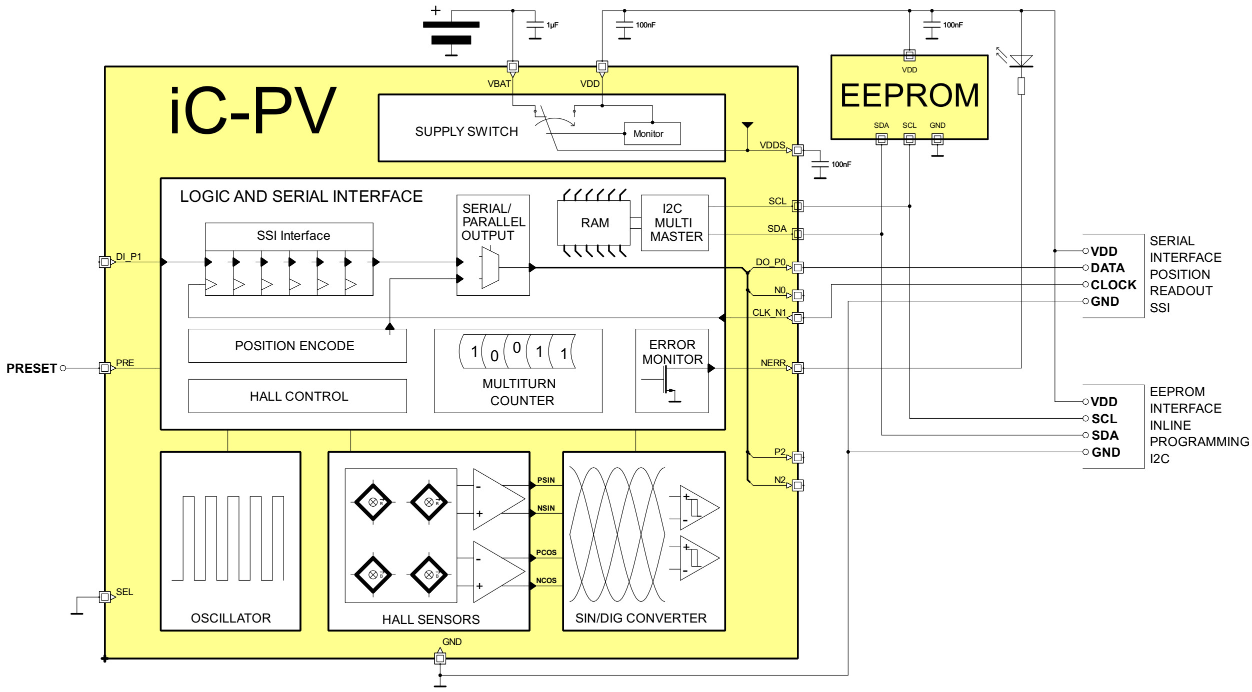


Figure 17: Application example iC-PV as battery powered multiturn counter, e.g. in a metering application. Interface operating in SSI-Mode (INT_MODE = 0) is used to readout the internal counter value. iC-PV is battery powered. VDD Supply is only needed during readout. EEPROM programming inline over SCL/SDA.

APPLICATION NOTES: iC-PV as 3 bit parallel mode (µC application)

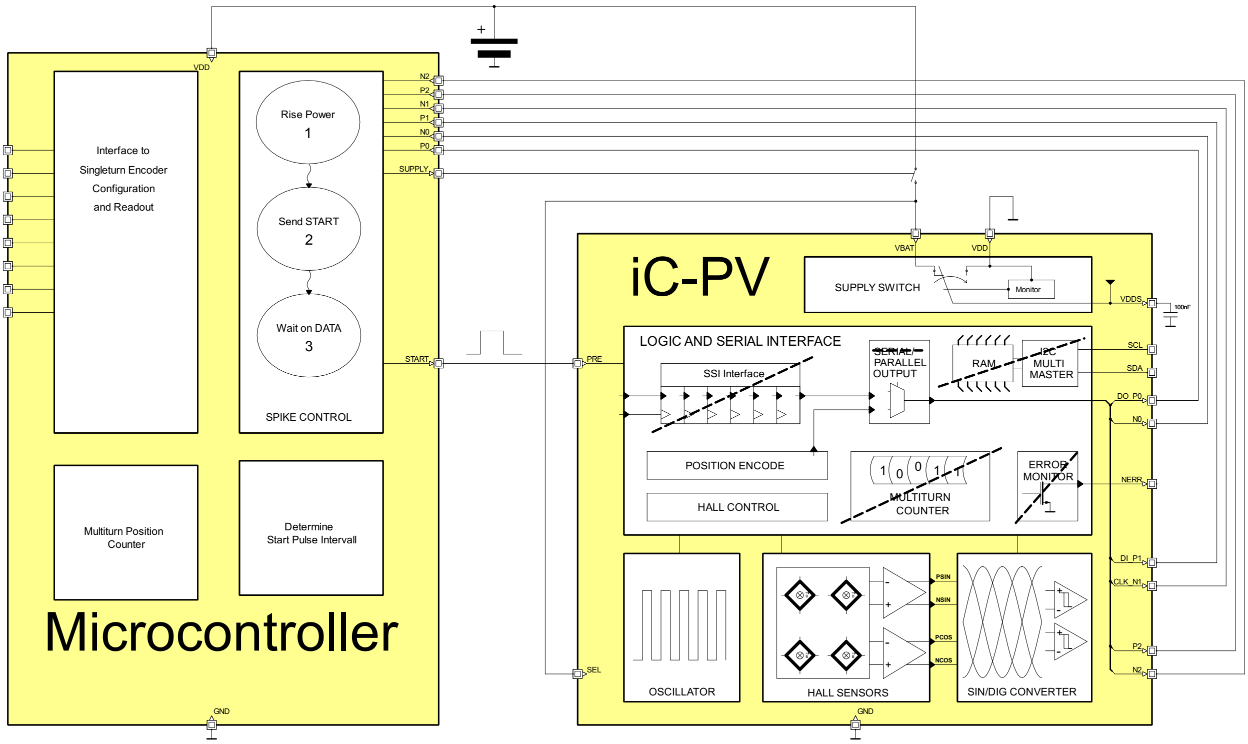


Figure 18: Application example of iC-PV acting as parallel mode (3 bit). All intelligence (counting, spike control and period selection etc.) is provided by the mandatory microcontroller in this arrangement. Hence, the crossed-out blocks are not used in this operating mode.

DESIGN REVIEW : Notes On Chip Functions

iC-PV ...		
No.	Function, Parameter/Code	Description and Application Hints
1		For any former chip release, please refer to datasheet release C1.

Table 23: Notes on chip functions regarding former iC-PV chip releases

iC-PV Y3		
No.	Function, Parameter/Code	Description and Application Hints
1		No further notes at time of printing.

Table 24: Notes on chip functions regarding iC-PV chip release Y3.

REVISION HISTORY

Rel.	Rel. Date	Chapter	Modification	Page
B1	13-11-25	All	Initial release (reference)	all

Rel.	Rel. Date	Chapter	Modification	Page
C1	14-09-19	PACKAGING INFORMATION	"Pin DI_P1 should be wired to GND if unused." removed	4
		PACKAGE DIMENSIONS QFN16 3x3	Sensor circle and iC dimensions complemented	5
		ELECTRICAL CHARACTERISTICS	Item 004 condition: V(PRE) < 0.5 V Item 008: max. = 20 ms Item 104: dsens = 1.75 mm Item 105: AArel, Relative Angle Accuracy, new Item Item 302: min. = 3.5 and max. = 6.5 Item 702: [8-30 mA] => [4-15 mA]	7,8
		OPERATING REQUIREMENTS	Item I012: min. = 30 µs	9
		EEPROM INTERFACE AND CRC PROTECTION	New paragraph	17
		CALCULATING CURRENT CONSUMPTION	New paragraph	18
		APPLICATION NOTES	EEPROM access in circuit schematics	19ff
		APPLICATION NOTES	Removed ambiguous presentation of pins DI_P1 and CLK_N1 in circuit schematics	19ff
		ORDERING INFORMATION	Update evaluation kit and gui	26

Rel.	Rel. Date	Chapter	Modification	Page
D1	15-05-22	All	Global update	All
		ELECTRICAL CHARACTERISTICS	Item 103: max. limit Item 107, 108, 109: max. limits Item 301: min. and max. limits Item 402: max. limit Item 403: min. limit Item 606: min. and max. limits Item B02: max. limit	7f

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-PV	QFN16-3x3		iC-PV QFN16-3x3
Evaluation kit	PCB 38 mm diameter		iC-PV EVAL PV1M1
iC-PV GUI		Evaluation software for Windows PC	For download link refer to www.ichaus.com/pv_gui

Please send your purchase orders to our order handling team:

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