iC-MA3 ANGULAR HALL SENSOR WITH SIN/COS OUTPUT, CASCADABLE

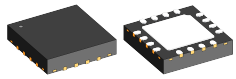
FEATURES

- Single supply operation from 3.0 V to 5.5 V
- For rotational speeds of up to 60,000 rpm
- Quad Hall array for high assembly tolerances
- High immunity to external stray fields
- Automatic gain control
- Digital control error output (loss-of-magnet indicator)
- Analog gain signal for magnetic field strength monitoring
- Two output modes: differential, or single-ended with reference and gain signal
- Pin-selectable output level: 250 mV, 500 mV, 1 V
- Pin-selectable power modes: full, reduced, eco
- Pin-selectable bandwidth of 500 Hz, 5 kHz, 10 kHz
- Bus-capable outputs for chain operation of multiple devices
- Quick start from power saving standby
- Operating temperature range of -40 °C to 125 °C

APPLICATIONS

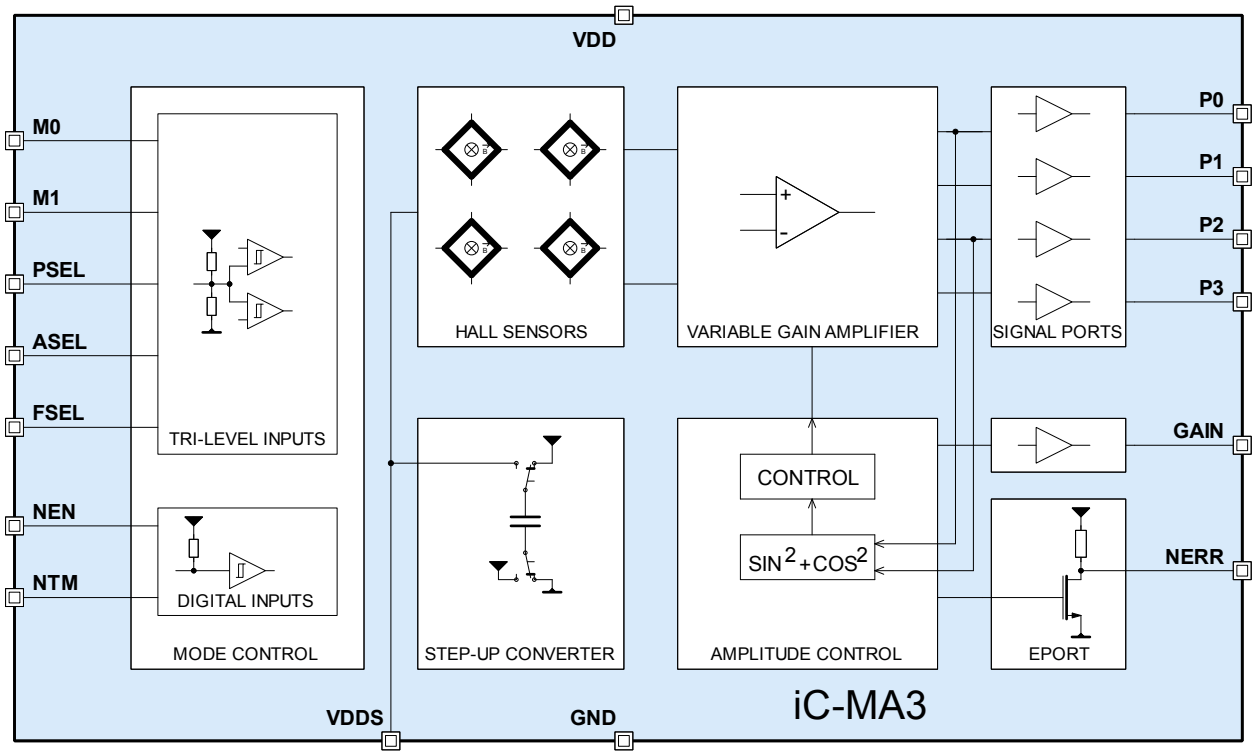
- Precision magnetic angle sensing
- Absolute rotary position sensors
- Magnetic multiturn encoders

PACKAGES



QFN16
4 mm x 4 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The magnetic angle sensor iC-MA3 is easily configured by pins and runs off a single 3 V to 5.5 V supply. The device outputs conditioned sine/cosine signals representing the axis angle, introduced by a diametric permanent magnet facing the package.

An array of four Hall sensors is used for the differential scanning of the magnetic field, whereas unwanted external stray fields are nearly compensated, and thus not detected. Besides, a high lateral mechanical placement tolerance is obtained easing device installation.

The sine/cosine signals can be output either single-ended or differential, with a pin-configured amplitude controlled to 0.25 V, 0.5 V or 1 V. At full signal bandwidth of 10 kHz, iC-MA3 can track the magnet rotation at up to 60,000 rpm.

The signal bandwidth can be lowered to 5 kHz or 500 Hz by pin configuration, to cut noise and improve the measurement precision. Furthermore, the Hall sensors' sampling rate can be reduced to lower the power consumption of the device.

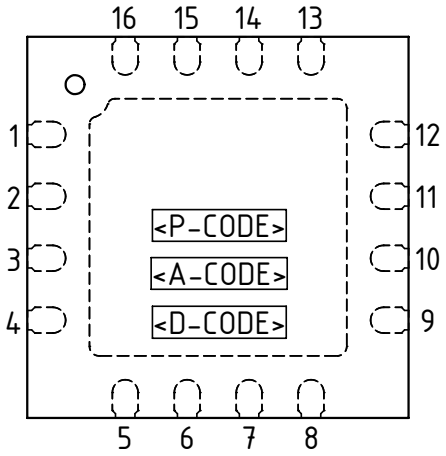
The analog gain signal is output to pin GAIN and indicates the magnet-to-sensor operating distance. At an excessive distance, the GAIN signal saturates and open-drain output NERR indicates the loss-of-magnet failure by a low signal.

Multiple iC-MA3 devices can be cascaded to sense several rotary axes, one at a time, but sharing a common analog signal bus to report the angle positions.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION

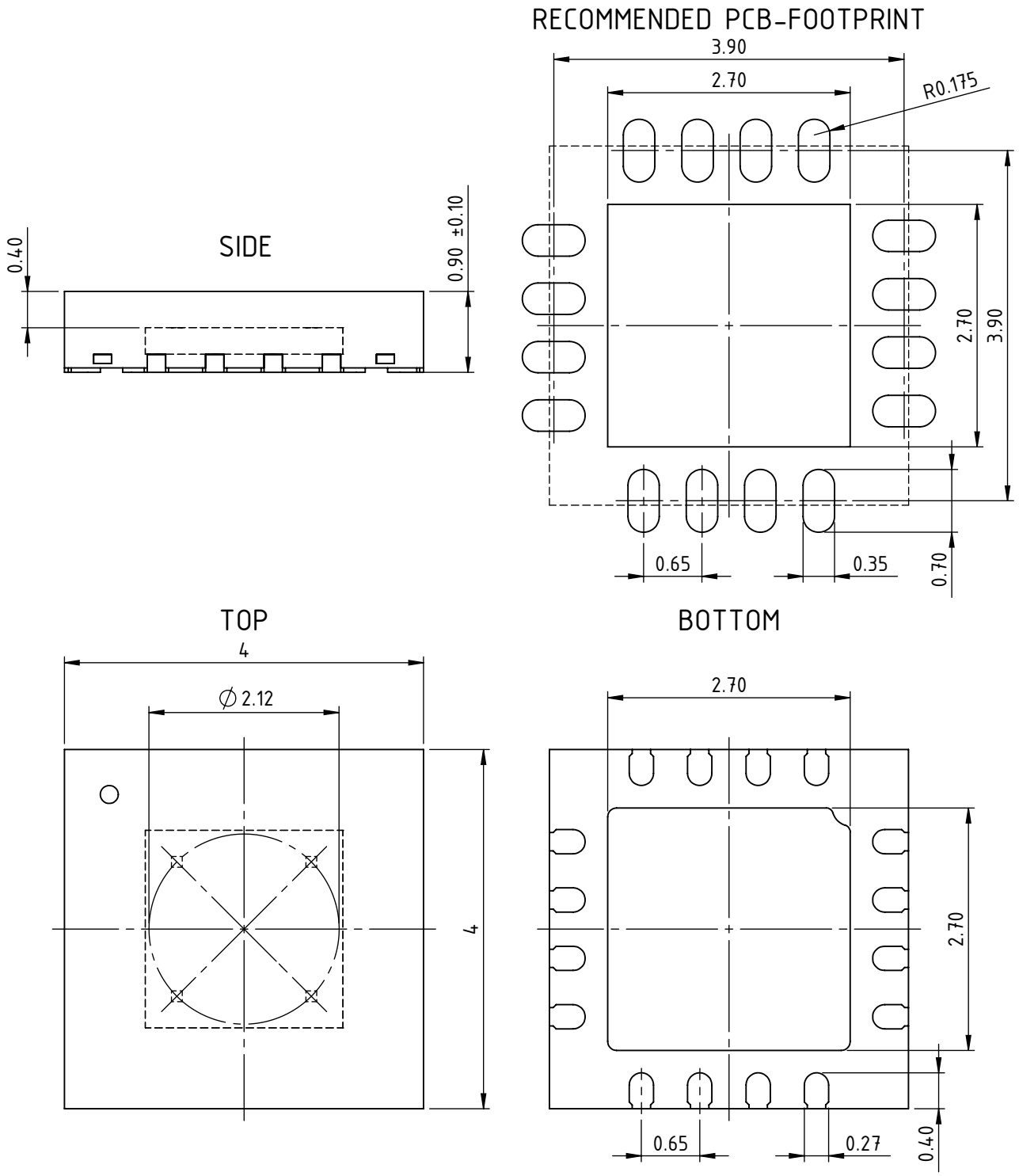


PIN FUNCTIONS

No.	Name	Function
1	VDDS [1]	Internal Supply Voltage (Step-Up Converter Output)
2	M0 [2]	Operating Mode Input 0: hi = differential output lo = single-ended output
3	M1 [2]	Operating Mode Input 1: hi = chain operation lo = single-chip operation
4	NTM [3]	Test Mode Input, low active
5	P0	Signal Port 0 / Input CLK
6	P1	Signal Port 1
7	P2	Signal Port 2
8	P3	Signal Port 3 / Output NENO
9	NEN	Enable Input, low active
10	PSEL	Power Setting Input: hi = full, mid (open) = eco, lo = low power
11	ASEL	Output Level Setting Input: hi = 1 V, mid (open) = 250 mV, lo = 500 mV
12	FSEL	Speed Setting Input: hi = max, mid (open) = 1/20, lo = half
13	GAIN	Amplitude Control Gain Output
14	VDD	+3.0 ... +5.5 V Supply Voltage Input
15	GND	Ground
16	NERR	Error Output, low active
	BP [4]	Backside Paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
1) Do not load. Connecting a backup capacitor is recommended (refer to Page 16).
2) Cycling the input level of NEN is required to alter the operating mode.
3) The test mode input NTM may remain unconnected. However, wiring this pin to VDD is recommended to avoid any impact of disturbances.
4) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±0.10mm / ±1° (with respect to backside pad).

dra_qfn16-4x4-2_mal_1_pack_1, 15:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.3	6	V
G002	V()	Voltage at M0, M1, PSEL, ASEL, FSEL, NEN, NTM, P0, P1, P2, P3, GAIN, NERR, VDDS	V() < VDD + 0.3 V	-0.3	6	V
G003	I(VDD)	Current in VDD		-30	30	mA
G004	I()Pad	Current in M0, M1, PSEL, ASEL, FSEL, NEN, NTM, P0, P1, P2, P3, GAIN, NERR		-5	5	mA
G005	I(VDDS)	Current in VDDS		-20	20	µA
G006	Vd()	ESD Susceptibility at all pins	HBM 100pF discharged through 1.5 kΩ		2	kV
G007	Tj	Junction Temperature		-40	150	°C
G008	Ts	Chip Storage Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VDD = 3.0 V...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	package mounted on PCB, *backside paddle* at approx. 2 cm² cooling area		30	40	K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 3.0 V...5.5 V, Tj = -40...125 °C, 4 mm NdFeB magnet, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD	Supply Voltage VDD		3		5.5	V
002	I(VDD)full	Supply Current in VDD	PSEL = VDD (full power mode) VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 4.5 5	 8 11	 15 20	 mA mA
003	I(VDD)red	Supply Current in VDD	PSEL = GND (reduced power mode) VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 3 3	 5 6	 9 9	 mA mA
004	I(VDD)eco	Supply Current in VDD	PSEL = open (eco power mode) VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 2.5 2.5	 4 5	 8 8	 mA mA
005	I(VDD)sby	Standby Current in VDD	NEN = VDD, NTM = VDD			200	µA
006	Vt(VDD)on	Power-on Threshold at VDD				3	V
007	Vt(VDD)off	Power-off Threshold at VDD	decreasing voltage at VDD			3	V
008	tp(VDD)on	Power-on Propation Delay	without backup capacitor at VDDS		15	30	µs
009	tp(VDD)off	Power-off Propagation Delay	without backup capacitor at VDDS		3		µs
010	Vc()hi	Clamp Voltage hi at M0, M1, NTM, P0, P3, NEN, PSEL, ASEL, FSEL, GAIN, NERR	Vc()hi = V() - VDD, I() = 1 mA	0.3		1.5	V
011	Vc()lo	Clamp Voltage lo at VDD, VDDS, M0, M1, NTM, P0, P1, P2, P3, NEN, PSEL, ASEL, FSEL, GAIN, NERR	I() = -1 mA	-1.5		-0.3	V
Hall Sensors							
101	Hext	Permissible Magnetic Field Strength	at chip surface, field frequency < 0.1 x fc(); VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 20 15		 110 65	 kA/m kA/m
102	dsens	Diameter of Hall Sensor Circle			2.1		mm
103	xdis	Permissible Lateral Displacement of Magnet Axis to Center of Hall Sensors	4 mm magnet, for an interpolation accuracy of >7 bit without additional signal conditioning		0.25		mm
104	xpac	Displacement Chip Center to Package Center	package QFN16-4x4	-0.15		0.15	mm
105	ϕpac	Angular Alignment of Chip vs. Package	vs. backside paddle of QFN16-4x4	-1		1	DEG
106	hpac	Distance Chip Surface to Package Surface	package QFN16-4x4		0.4		mm
107	fc()	Hall Signal Cut-Off Frequency (-3 dB)	PSEL = VDD (full power mode); FSEL = VDD FSEL = GND FSEL = open	 	 10 5 0.5	 	 kHz kHz kHz
109	tp()	Signal Propagation Delay (Position Lag vs. Field Angle)	PSEL = VDD (full power mode), FSEL = VDD (see also Table 10)		16		µs
Amplitude Control and Output GAIN							
201	ts()ctrl	Amplitude Control Settling Time	Hext = 40 kA/m, from 0 → 80 % of final setpoint			200	µs
202	Vout()fs	Output Signal at Maximum Gain	field strength Hext below minimum		2.5		V
203	I()max	Permissible Load Current		-0.5		+0.5	mA

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 3.0 V...5.5 V, Tj = -40...125 °C, 4 mm NdFeB magnet, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Mode Control Inputs, tri-level: M0, M1, PSEL, ASEL, FSEL							
301	Vt()hi	Threshold Voltage hi		70		80	%VDD
302	Vt()lo	Threshold Voltage lo		20		30	%VDD
303	V0()	Pin-Open Voltage		40		60	%VDD
304	Ri()pu, pd	Internal Pull-Up/Down Resistors			200		kΩ
305	t()filter	Input Debouncing Time at PSEL, ASEL, FSEL			8		µs
Mode Control Inputs, digital: NEN, NTM							
401	Vt()hi	Threshold Voltage hi				2.0	V
402	Vt()lo	Threshold Voltage lo		0.8			V
403	Vt()hys	Threshold Voltage Hysteresis	Vt()hys = Vt()hi - Vt()lo	100		440	mV
404	Ipu()	Pull-Up Current	V() = 0 V ... VDD - 1 V; VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 -25 -62	 -12 -28	 -4 -7	 µA µA
Signal Ports: P0, P1, P2, P3							
501	Vref	Signal Reference Voltage	M0 = lo, M1 = lo, measured at port P0	45	50	55	%VDD
502	Vout()pk	Sin/Cos Signal Amplitude	ASEL = VDD ASEL = GND ASEL = open		1000 500 250		mV mV mV
503	I()max	Permissible Load Current		-0.5		0.5	mA
Signal Ports: P0 (input CLK) and P3 (output NENO) during chain operation (M1 = lo)							
601	Vt()hi	Threshold Voltage hi at P0				2.0	V
602	Vt()lo	Threshold Voltage lo at P0		0.8			V
603	Vt()hys	Threshold Volt. Hysteresis at P0	Vt()hys = Vt()hi - Vt()lo	100		440	mV
604	Ipd()	Pull-Down Current at P0	V() = 1 V ... VDD; VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 4 7	 12 28	 40 103	 µA µA
605	Vs()hi	Saturation Voltage hi at P3	Vs()hi = VDD - V(), I() = -4 mA; VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 130 100		 420 320	 mV mV
606	Vs()lo	Saturation Voltage lo at P3	I() = 4 mA; VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 80 60		 400 300	 mV mV
607	tr()	Rise Time at P3	CL() = 30 pF			20	ns
608	tf()	Fall Time at P3	CL() = 30 pF			20	ns
Error Port: NERR							
701	Vs()lo	Saturation Voltage lo	I() = 4 mA; VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 80 60		 400 300	 mV mV
702	Ipu()	Pull-Up Current	V() = 0 ... VDD - 1 V; VDD = 3.3 V ±10% VDD = 5.0 V ±10%	 -25 -62	 -12 -28	 -4 -7	 µA µA
703	tf()	Fall Time	CL() = 30 pF			20	ns
Step-Up Converter: VDDS							
801	VDDS	Step-Up Voltage Output	no load permissible	5			V
802	C(VDDS)	Recommended Backup Capacitor	M1 = lo M1 = hi (chain operation)		1	100 1	nF nF

HALL SENSORS

Principle of operation

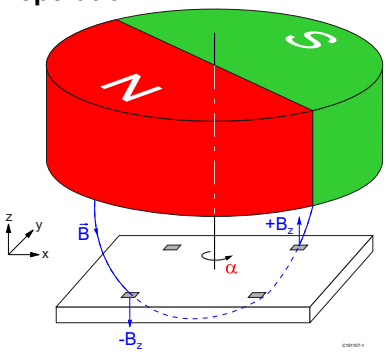


Figure 1: Principle of magnetic field measurement using Hall sensors

iC-MA3 has four Hall sensors which convert the magnetic field into measurable Hall voltages. The arrangement of the array has been specifically selected to allow a very tolerant assembly of iC-MA3 to the magnet axis. Solely the magnetic field's z-component is evaluated at which the field lines pass through two opposing sensors in opposite directions (Figure 1).

Differential signals are generated by the combination of two Hall sensors each. When the magnet rotates along its longitudinal axis, sine and cosine output signals are created which can be evaluated by the subsequent electronic to derive the angle position of the axis holding the magnet.

A diametrically magnetized, cylindrical permanent magnet made of Neodymium Iron Boron (NdFeB) or Samarium Cobalt (SmCo) generates optimum sensor signals. The magnet cylinder's diameter should be in the range of 3 mm to 6 mm.

Hall sensor array and zero angle

The four Hall sensors are placed in the center of the QFN16 package on a circle of 2.1 mm in diameter and have a 90 ° angle distance to one another (Figure 2).

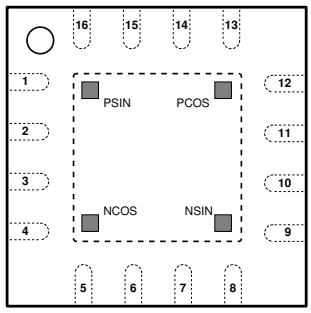


Figure 2: Position of the Hall sensors in the QFN package (top view)

The diametric magnet is to be placed centrically above the device package (Figure 3).

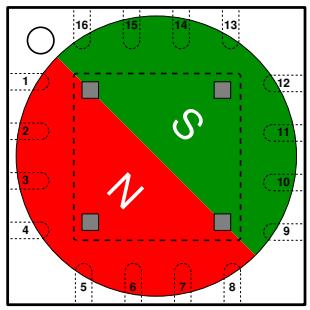


Figure 3: Magnet in zero position (0°)

Each Hall sensor only measures the z-component of the magnetic field. For the two Hall sensors located directly beneath the poles, the absolute value of the measured field strength is maximum but with different polarity.

For the two Hall sensors which are located at the interface of the north and south pole, the magnetic field has no component in z-direction, thus, their signal is 0.

When the magnet rotates counterclockwise, the measured signal changes sinusoidal with the rotary angle. The angle of 90° between two neighboring Hall sensors yields phase-shifted sine- and cosine-signals with positive (PSIN, PCOS) and negative (NSIN, NCOS) polarity.

MODE CONTROL

Operation modes
The pins M0 and M1 are used to choose between single-ended and differential measurement and to set single-chip operation or chain operation to evaluate multiple devices connected to a bus line.

Changing the operation mode
The operation mode configured by pins M0 and M1 is stored internally following power-up. So if changing the pin state of M0 or M1 during operation, it does not immediately alter the operation mode. To activate the new pin set, enable input NEN must first be released to high to disable the IC. After pulling NEN low again, the new operation mode comes effective.

Note: Changes to pins PSEL, ASEL, and FSEL come into play immediately after exceeding their debouncing time (refer to Elec. Char. No. 305).

Mode	M0	M1	Port P0	Port P1	Port P2	Port P3
Single-chip operation						
Single-ended output	low	low	VREF	PSIN	PCOS	GAIN
Differential output	high	low	NSIN	PSIN	PCOS	NCOS
Chain operation						
Single-ended output	low	high	CLK	PSIN / VREF	PCOS / GAIN	NENO
Differential output	high	high	CLK	PSIN / NSIN	PCOS / NCOS	NENO

Table 4: Operation modes

Power saving modes
Two power saving modes are selectable by pin PSEL which reduce the current consumption of iC-MA3. If selected, the Hall sensors are no longer operated continuously but only activated periodically for a short time. On one hand this reduces the IC's current consumption, on the other hand it decreases the update rate of the measurements, what reduces the permissible maximum rotary frequency accordingly.

A power saving mode can be freely combined with any setting of integration time.

Mode	PSEL	Update Rate	Notes
Full Power	high	÷1	continuous measurement
Reduced Power	low	÷6	
Eco Power	open	÷18	

Table 5: Power saving modes

Speed setting (integration time)
If the maximum rotary frequency of a system is lower than the Hall sensors cut-off frequency (refer to Elec. Char. No. 107), pin FSEL can allow for a longer averaging of measurements reducing signal noise.

Note that the maximum rotary frequency listed in Table 6 refers to full power mode (continuous measurements).

Any setting of integration time can be freely combined with a power saving mode.

If combining the modes, the permissible maximum rotary frequency scales according to the product of both factors: factor of Tab. 5 multiplied by factor of Tab. 6.

Mode	FSEL	Max. Rotary Freq.	Notes
Full Speed	high	÷1	normal
Half Speed	low	÷2	halved
Min Speed	open	÷20	minimal

Table 6: Speed setting (integration time)

Output level setting
Pin ASEL selects the target amplitude to which the sin/cos signals output at ports P0 to P3 are regulated to. In any case Vref, the half of the supply voltage, remains to be the reference voltage.

Mode	ASEL	Signal Amplitude	Notes
High-Level Output	high	±1000 mV	V(P0...P3) = Vref ±Vout()pk
Mid-Level Output	low	±500 mV	
Low-Level Output	open	±250 mV	

Table 7: Output level setting

Standby
If pin NEN, featuring an internal pull-up, is not forced low by an external signal, iC-MA3 remains in standby mode. During this mode the tri-level mode control inputs M0, M1, PSEL, ASEL, FSEL, and the signal ports P0 to P3 are all high impedance, so that a minimal current consumption is obtained.

Mode	NEN	Mode Control Inputs M0, M1, PSEL, ASEL, FSEL	Signal Ports P0, P1, P2, P3, GAIN, NERR	Notes
Standby	high	high impedance	high impedance[1]	

Table 8: Standby

[1] During chain operation, pin P3 remains active high to disable the subsequent IC.

Test Mode
With pin NTM, iC-MA3 can be set to test mode for iC-Haus device testing. If there is no external signal forcing pin NTM low, the pin's internal pull-up disables the test mode. However, for safety pin NTM should be connected to VDD to avoid any unwanted function.

Mode	NTM	Mode Control Inputs M0, M1, PSEL, ASEL, FSEL	Signal Ports P0...P3	Notes
Test Mode	low			device test only

Table 9: Test mode

SINGLE-CHIP OPERATION and OUTPUT SIGNALS

In single-chip operation, the pins P0 to P3 are configured as outputs for the sine and cosine signals. Two output modes are available: single-ended output (Figure 4), and differential output (Figure 5).

Single-ended output

The measurement is performed single-ended using a reference voltage. The sine signal is available at pin P1, the cosine signal at pin P2, and their reference voltage at pin P0.
Additionally, the gain signal of the amplitude control can be monitored at pin P3 (refer to SENSOR MONITORING, Page 15, for description).

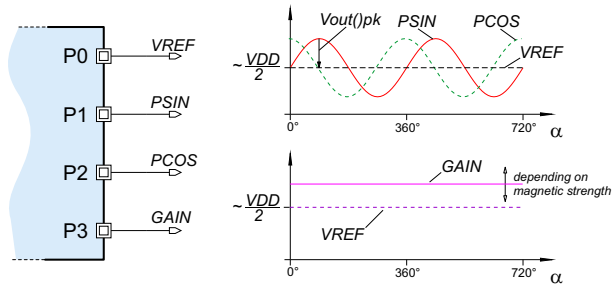


Figure 4: Single-chip operation with single-ended output of sine/cosine (PSIN, PCOS), with reference (VREF) and gain signal (GAIN).

The sin/cos signal amplitude Vout()pk refers to the reference voltage Vref, which is approximately half the supply voltage. This means a pin's output signal varies in the range of Vref ± Vout()pk.

For single-ended output, the measurement signal is ± Vout()pk, and doubles with differential output to ± 2 x Vout()pk. In both cases, the axis angle applied by the magnet's field is to be calculated by the ratio of the sine and cosine signals. By taking the signal's polarity into account, the angle is distinct over a full turn of the axis.

Note that three different output levels are selectable by pin ASEL (see Table 7), allowing the adaption of iC-MA3 to the evaluating system.

Differential output

The differential output features the advantage of a doubled amplitude compared to single-ended. A positive- and a negative-going sine signal is available at pins P1 and P0, respectively, a positive- and negative-going cosine signal at pins P2 and P3.

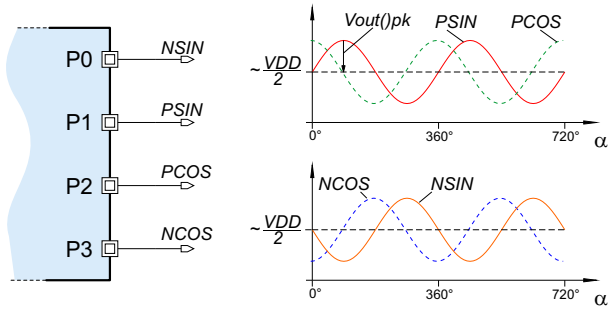


Figure 5: Single-chip operation with differential output of sine (PSIN, NSIN) and cosine (PCOS, NCOS).

Activation

The voltage at enable input NEN must first undershoot its low threshold to activate the mode configured by M0 and M1. Due to the IC's amplitude control settling, the output signals require some time to reach the preset level (refer to ts()ctrl, Elec. Char. No. 201).

MULTI-CHIP CHAIN OPERATION

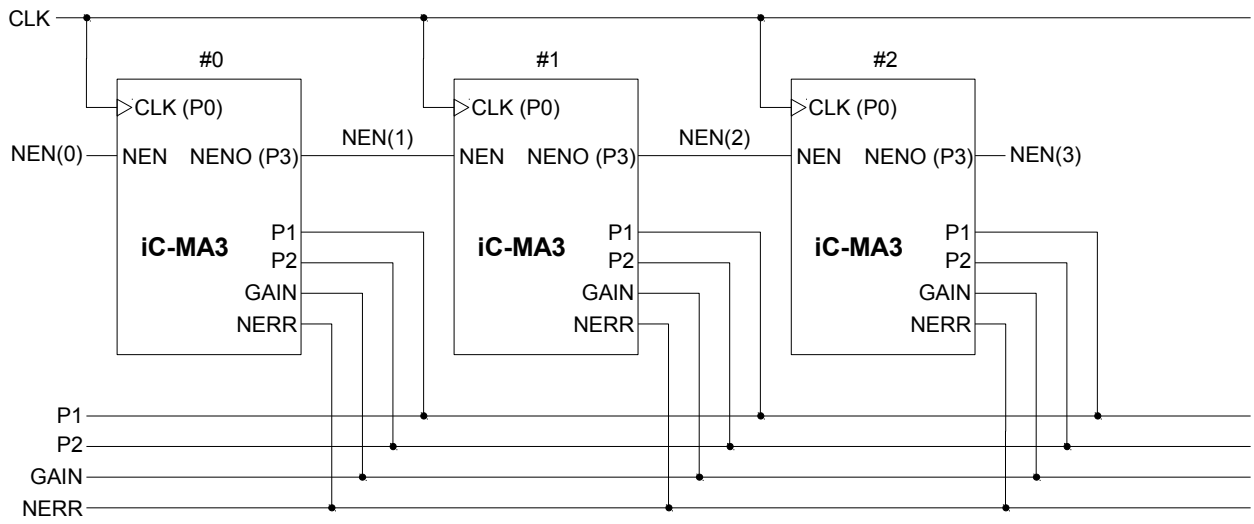


Figure 6: Multiple sensors in chain operation (example with single-ended output)

In chain operation, multiple sensors connected to a common signal bus can be readout sequentially, at a reduced line count (Figure 6).

By pulling enable input NEN of IC #0 to low, the first sensor is activated. With the first rising edge of input CLK, the bus outputs of IC #0 (P1, P2, GAIN, NERR) are activated, the bus outputs of IC #1 and IC #2 remain on high impedance ('High-Z').

With the falling edge of the second CLK pulse, the bus outputs IC #0 (P1, P2, GAIN, NERR) become high impedance and NENO changes from high to low, activating the subsequent IC #1, which is then active for the following two CLK pulses. Thus, the outputs of only one IC are active at a time, and other bus outputs remain high impedance.

Finally, at the end of the chain, all bus outputs are set back to high impedance. A new measurement cycle can be introduced by disabling and re-enabling IC #0 (NEN(0) = high, then followed by a low).

An asynchronous reset of the chain is possible at any time, by setting NEN(0) = high. This sets back the bus outputs of IC #0 to high impedance, and outputs a high on NENO (pin P3) disabling the subsequent IC's.

Line signals
Single-ended or differential output signals are available during chain operation (according to Table 4).

Single-ended output
The measurement is performed single-ended with VREF as the reference potential. After the first rising edge of the CLK signal, PSIN is available at P1 and PCOS at P2. After the second rising edge of CLK, VREF is available at P1 and GAIN at P2. Refer to chapter SENSOR MONITORING, Page 15, for a description of the GAIN signal.

Differential output
The measurement is performed differentially. After the first rising edge of the CLK signal, PSIN is available at pin P1, and PCOS at pin P2. After the second rising edge of CLK, NSIN is available at pin P1, and NCOS at pin P2.

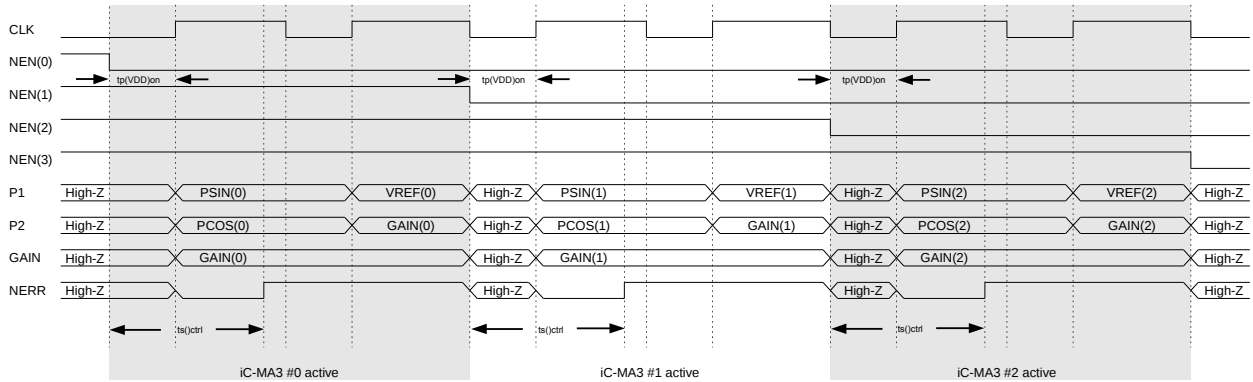


Figure 7: Line signals and timing for chain operation (example for single-ended output)

Line timing
A settling time ts()ctrl is required for the adaption to the magnet field strength and its processing. Only after this initial settling the first values (here PSIN and PCOS) can be read correctly. As there is no further settling required for the second cycle, reading and evaluating the second values (here VREF and GAIN) can follow quicker.

After enabling an IC, the bus outputs are activated with the first rising edge of the CLK signal. Note that also the analog bus lines need to settle following output activation. Thus, the accuracy of the measurement signals can be improved if the outputs are activated early, soon after enabling a device (by setting CLK high).

Note that the operation mode has to be read after IC activation (by NEN = low), so that the power-on progation delay tp(VDD)on must be passed before an IC is able to react on the signal at input CLK.

For chain operation, the following procedure is recommended:

1. Set CLK to low, then activate the chain with NEN(0) = low.
2. After the activation of the chain, wait at least tp(VDD)on, then set CLK = high.
3. Wait at least until NERR changes from low to high before reading the first values of IC #0.
4. With the second rising edge of CLK, the second values of IC #0 are available on the bus lines, which can be directly read.
5. The second falling edge of CLK causes the activation of IC #1 by NEN(1).
6. After the activation of IC #1, wait at least for tp(VDD)on again, before setting CLK = high.

The sequence described in steps 3 through 6 repeats until the end of the chain is reached and a new measurement cycle is started by resetting the chain (NEN(0) = high).

POWER SAVING OPERATION

A power saving mode reduces the current consumption of the IC. There are three modes available, according to Table 5, Page 9.

The power saving modes vary the time between two active phases of the Hall sensors (Figure 8). M1 is the constant current consumption without power saving; the Hall sensors are active permanently.

Using power saving, the Hall sensors are activated only for time t()on, and are deactivate for time t()off. This yields a current consumption shown as M2.

The ratio of $\frac{t()on}{t()on+t()off}$ is the value listed under column Update Rate in Table 5.

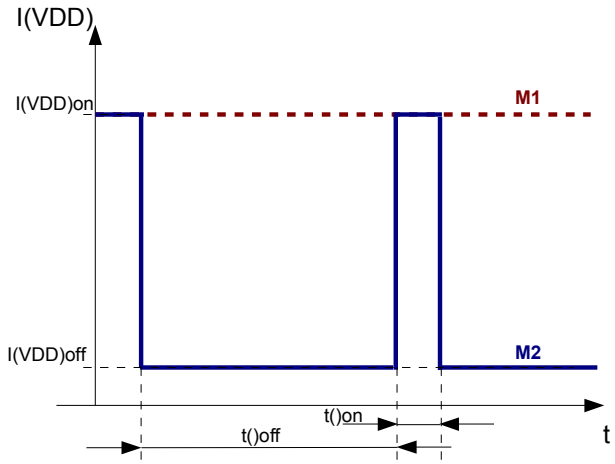


Figure 8: Current consumption with power saving

As the Hall sensors are not permanently active, the permissible maximum rotary frequency reduces according to the given ratio. Note that the IC's current consumption does not reduce by the same ratio, as only the Hall sensors are deactivated and the current consumption is still higher than during standby.

A power saving mode (selected by pin PSEL) can be freely combined with any speed mode (selected by pin FSEL).

Power savings are obtained by a lower sampling rate for measurements, whereas speed settings change the integration time by additional filtering. Both modes operate independently from each another, but both take influence on the permissible maximum rotary frequency. If combining the modes, the permissible maximum rotary frequency reduces according to the product of the factors given by Tables 5 and 6.

Example
The reduced power mode (PSEL = low) reduces by a factor of 6, the minimal speed setting (FSEL = open) by a factor of 20. Thus, the combination reduces the permissible maximum rotary frequency from 60,000 rpm to 500 rpm.

SPEED SETTING (Integration Time)

iC-MA3 has been designed to precisely measure high rotary frequencies and fast changes of the rotary angle. To cater for applications where the rotary frequency is always significantly lower than the IC's performance, the bandwidth can be limited by pin FSEL. This enlarges the integration time and improves the accuracy of the measured signals.

A speed setting (selected by pin FSEL) can be freely combined with any power saving mode (selected by pin PSEL). Refer to the forementioned Example (Page 14) explaining the impact on the permissible maximum rotary frequency.

In any case, the measurement signals are filtered to suppress noise and disturbances, and the signal path can be considered as a 1st order low-pass filter with a cut-off frequency (fc). Due to this, a time lag (tlag) does exist between the applied input angle (by the magnet field) and the measured rotary angle (the output signal). The table below reflects the principal dependencies.

Note that the low-pass characteristic also reduces the amplitude of the measured Hall signals, what has to be compensated by the amplitude control. Thus, the measureable magnetic field strength Hext is valid for a signal frequency fin $< 0.1 \cdot$ fc.

	Full Speed	Half Speed	Min Speed
Full Power	10 kHz 16 µs	5 kHz 32 µs	500 Hz 320 µs
Reduced Power	1.7 kHz 90 µs	850 Hz 180 µs	85 Hz 1800 µs
Eco Power	550 Hz 290 µs	275 Hz 580 µs	30 Hz 5800 µs

Table 10: Typical values for cut-off frequency and time lag (at fin $< 0.1 \cdot$ fc)

SENSOR MONITORING

Monitoring by output GAIN
The analog signal at output GAIN represents the actual amplification of the Hall signals, which is required to reach the selected output level for the ports P0. . . P3. Thus, it is a measure of the magnetic field strength seen by the Hall sensors.

A lower magnetic field strength requires a higher amplification, so that it causes a higher signal level at output GAIN. When the signal level at GAIN saturates, the maximum amplification has been reached and the outputs may not show the preset level anymore.

The gain signal is always present at pin GAIN. The gain signal is also output to pin P2 or P3, if single-ended output is selected by mode control inputs M0 and M1.

Depending on the output pin, the gain signal has different voltage ranges:

At pin GAIN, the voltage range is:
V(GAIN) = 0 . . . Vout(GAIN)fs
(refer to Elec. Char. No. 202).

The voltage is zero at minimum gain (max. field strength), and reaches Vout(GAIN)fs at maximum gain (min. field strength).

At pins P2 and P3, the voltage range is:
V(P2, P3) = Vref . . . Vref + Vout()pk
(refer to Elec. Char. No. 501 and 502).

Here, Vout()pk is the signal amplitude according to the output level preset by pin ASEL. The output voltage is equal to Vref at minimum gain (max. field strength), and reaches Vref + Vout()pk at maximum gain (min. field strength).

Signal examples for output GAIN
For the following examples we assume iC-MA3 is configured for single-chip operation, single-ended and mid-level output: signal GAIN is output at P3.

Example 1: Gain at 50 % of maximum
At VDD = 5.0 V, the output reference Vref is 2.5 V.
Due to mid-level output, 500 mV is the maximum signal level that can be reached at P3.
In this case, the voltage at pin GAIN is:
V(GAIN) = 0.5 x Vout(GAIN)fs
approx. 0.5 x 2.5 V = 1.25 V

And at pin P3, the max. voltage is:
V(P3) = Vref + 0.5 x Vout()pk
approx. 2.5 V + 0.5 x 500 mV = 2.75 V.

At VDD = 3.3 V we obtain:
V(GAIN) approx. 1.25 V
V(P3) approx. 1.65 V + 0.5 x 500 mV = 1.9 V
due to a lower Vref.

Example 2: Gain at maximum (insuffient field strength)
At VDD = 5.0 V, the output reference Vref is 2.5 V.
Due to mid-level output, 500 mV is the maximum signal level that can be reached at P3.
In this case, the voltage at pin GAIN is:
V(GAIN) = Vout(GAIN)fs, approx. 2.5 V

And at pin P3, the voltage is:
V(P3) = Vref + Vout()pk
approx. 2.5 V + 500 mV = 3.0 V.

At VDD = 3.3 V we obtain:
V(GAIN) approx. 2.5 V
V(P3) approx. 1.65 V + 500 mV = 2.15 V
due to a lower Vref.

Monitoring by output NERR
After enabling the IC, the amplitude control needs time for settling (ts()ctrl), for the adaption to the external field strength and to get to the preset output level. During this phase, the low-active error output NERR shows a low signal, indicating that the output amplitude is poor and may not allow accurate measurements. The error output NERR releases to high, as soon as the controlled amplitude has reached approx. 80 %. of the preset level.

Any insufficient field strength, a loss-of-magnet condition for instance, leads to amplitude control saturation at maximum gain. If the output amplitude does not keep approx. 80% of the preset level, error outout NERR indicates a low.

STEP-UP CONVERTER

The built-in step-up converter supplies certain internal circuit sections, which benefit from a higher supply voltage. To further stabilize this internally used supply voltage, and to prevent it from impact of disturbances, an additional external capacitor may be connected at pin VDDS versus pin GND.

Note: When iC-MA3 is powered up, any capacitor at VDDS slows down the ramp-up of the step-up voltage, and so the signal output experiences a delay. Thus, for the selection of the capacitor value, the startup-time required by the application may need to be considered.

Mode	CVDDS
Single-chip operation	1 . . . 100nF
Chain operation	approx. 1nF

Table 11: Recommended bypass capacitor at VDDS vs. GND

APPLICATION CIRCUITS

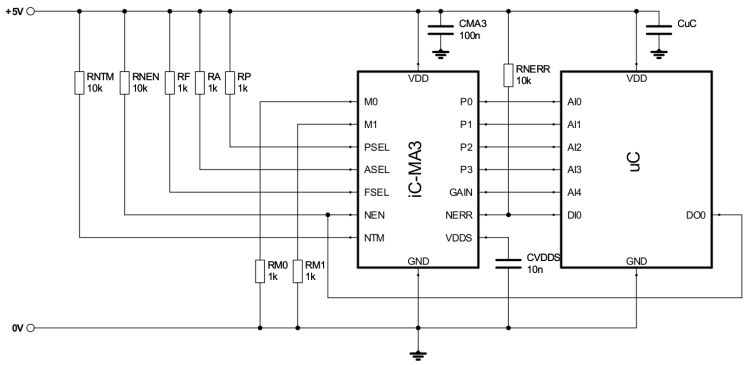


Figure 9: Single-chip operation with microcontroller

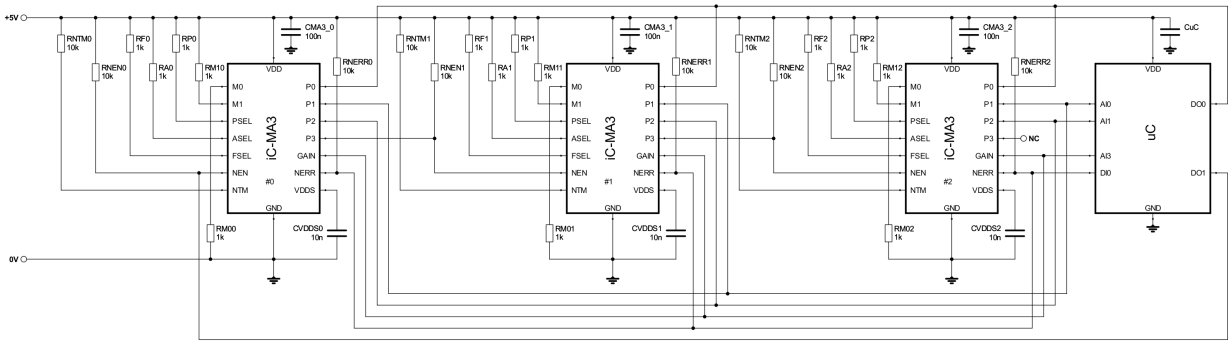


Figure 10: Chain operation with microcontroller

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2015-05-11		Initial release	all

Rel.	Rel. Date*	Chapter	Modification	Page
A2	2016-10-20	ELECTRICAL CHARACTERISTICS	Item 005, condition added: NTM = VDD Item 103: condition supplemented, typ. value instead of max. value	6

* Release Date format: *YYYY-MM-DD*

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Type	Package	Order Designation
iC-MA3	16-pin QFN, 4 mm x 4 mm RoHS compliant	iC-MA3 QFN16-4x4

Please send your purchase orders to our order handling team:

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For technical support, information about prices and terms of delivery please contact:

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