iC-MH16

12-BIT ANGULAR HALL ENCODER

preliminary

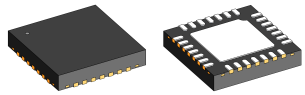
FEATURES

- Real-time system for full resolution at up to 200 000 rpm
- Integrated Hall sensors with automatic offset compensation
- 4x sensor arrangement for fault-tolerant adjustment
- Amplitude control for optimum operating point
- FlexCount® interpolator with 1 to 1024 CPR, resolution up to 4 096 / 0.08 °
- UVW commutation signals with 1 to 16 CPR, for motors of up to 16 pole pairs
- Programmable resolution, hysteresis, edge spacing, zero position and rotating direction
- Up to 16 MHz incremental edge rate
- RS422-compatible AB encoder signals with index Z
- BiSS/SSI interface for data output and configuration
- Integrated Zapping ROM for default setup and OEM data
- Errors signalized via pin and serial interface
- Single 5 V supply with reversed-polarity monitoring and sub-system switching
- Extended temperature range from -40 to +125 °C

APPLICATIONS

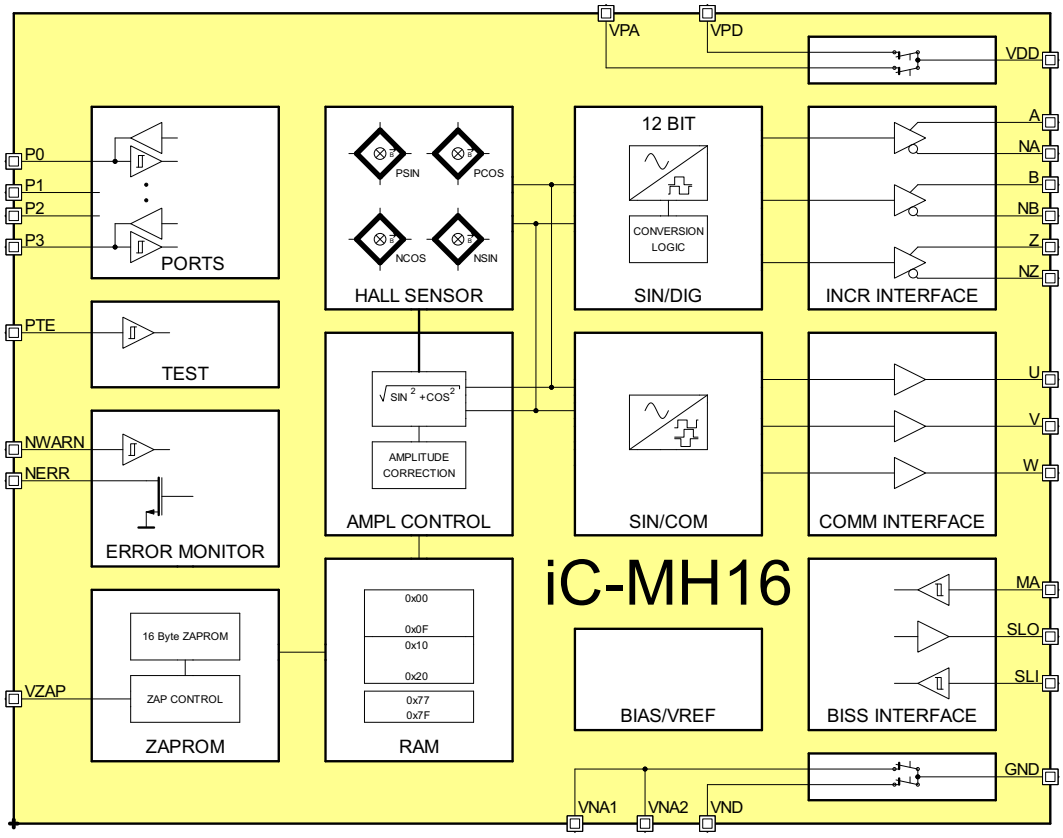
- Digital angular sensor technology, 0–360 °
- Incremental angular encoder
- Absolute angular encoder
- Brushless motors
- Motor feedback
- Rotational speed control

PACKAGES



QFN28
5 mm x 5 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The iC-MH16 12-bit angular encoder is a position sensor with integrated Hall sensors for scanning a permanent magnet. The signal conditioning unit generates constant-amplitude sine and cosine voltages that can be used for angle calculation. The resolution can be programmed up to a maximum of 4 096 angular increments per rotation; the zero position is adjustable.

The incremental interface with the pins A, B and Z supplies quadrature signals with an edge rate of up to 16 MHz. Interpolation is performed with maximum resolution at a speed of 200 000 rpm.

The RS422-compatible outputs of the incremental interface are programmable in the output current and the slew rate.

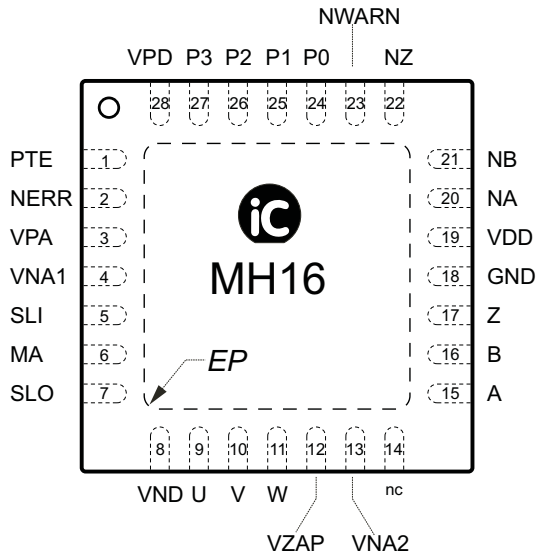
The commutation interface with the signals U, V and W provides 120 ° phase-shifted signals for block commutation of EC motors with up to 16 pole pairs.

The integrated serial interface also enables the position data to be read out to several networked sensors. The integrated memory can be written embedded in the data protocol.

In conjunction with a rotating permanent magnet, the iC-MH16 module forms an one-chip encoder including protection against a reversed power supply voltage. The entire configuration can be stored in the internal parameter ROM with zapping diodes. The integrated programming algorithm assumes writing of the ROM structure.

PACKAGING INFORMATION

PIN CONFIGURATION
QFN28 5 mm x 5 mm x 0.9 mm
(according to JEDEC Standard MO-220)

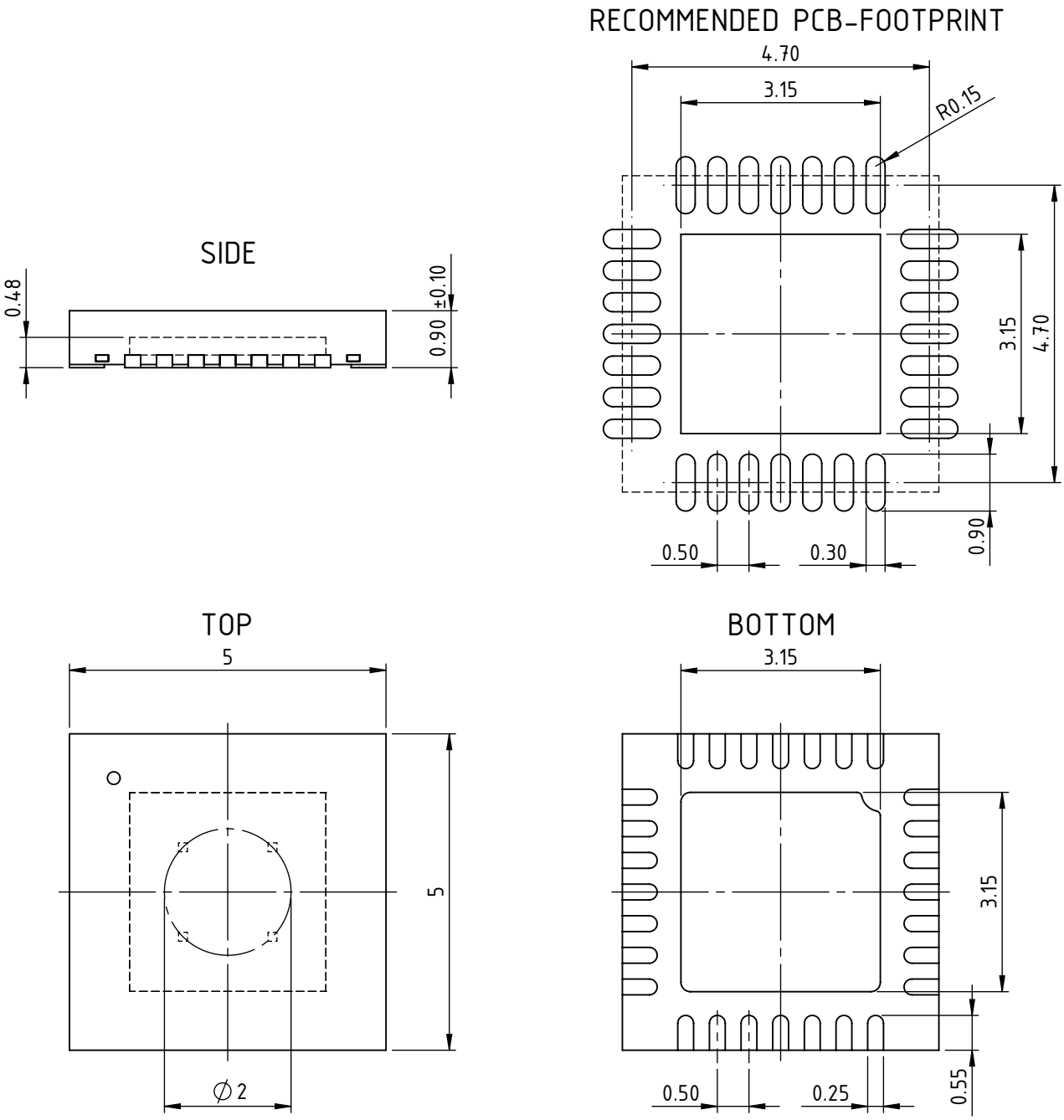


PIN FUNCTIONS

No.	Name	Function
1	PTE	Test Enable Pin
2	NERR	Error output(active low)
3	VPA	+5 V Supply Voltage (analog)
4	VNA1	Ground (analog)
5	SLI	Serial Interface, Data Input
6	MA	Serial Interface, Clock Input
7	SLO	Serial Interface, Data Output
8	VND	Ground (digital)
9	U	Commutation U
10	V	Commutation V
11	W	Commutation W
12	VZAP	Zener Zapping Programming Voltage
13	VNA2	Ground (analog)
14	nc	not connected
15	A	Incremental A
16	B	Incremental B
17	Z	Index Z
18	GND	Ground (line)
19	VDD	+5 V Supply Voltage (line)
20	NA	Incremental NA
21	NB	Incremental NB
22	NZ	Incremental NZ
23	NWARN	Warning input (active low)
24	P0	Bidirectional Port No. 0
25	P1	Bidirectional Port No. 1
26	P2	Bidirectional Port No. 2
27	P3	Bidirectional Port No. 3
28	VPD	+5 V Supply Voltage (digital)
	EP	Exposed Pad

The *Exposed Pad (EP)* has to be connected to common ground (VNA1, VNA2, VND) on the PCB. Orientation of the logo (iC MH16 CODE ...) is subject to alteration.

PACKAGE DIMENSIONS



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad). dra_qfn28-5x5-2_mh8_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, GND, A, B, Z, NA, NB, NZ, U, V, W, MA, SLI, SLO		-6	6	V
G002	V(VZAP)	Zapping voltage		-0.3	8	V
G003	V()	Voltage at NERR, NWARN, P0, P1, P2, P3, PTE		-0.3	6	V
G004	I()	Current in VDD		-10	20	mA
G005	I()	Current in GND		-20	200	mA
G006	I()	Current in A, B, Z, NA, NB, NZ, SLO, U, V, W		-100	100	mA
G007	I()	Current in MA, SLI, NERR, PTE		-10	10	mA
G008	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged over 1.5 kΩ		2	kV
G009	Ts	Storage Temperature		-40	150	°C
G010	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VPA, VPD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	surface mounted to PCB, *thermal pad* linked to cooling area of approx. 2 cm²		40		K/W

All voltages are referenced to pin VNA1 unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDD = 5 V ±10 %, EP = VNA1 = VNA2 = VND, Tj = -40...125 °C, IBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	V(VDD)	Permissible Supply Voltage		4.5		5.5	V
002	I(VDD)	Supply Current in VDD	PRM = 0x0, without load, fmag = 0 rpm	10	20	30	mA
003	fI(VDD)	Supply Current in VDD Rotating Speed Dependance	PRM = 0x0, without load, fmag = 0...3.3 kHz		1.4		mA/kHz
006	Vc()hi	Clamp-Voltage hi at P0, P1, P2, P3, PTE, NERR, NWARN	Vc()hi = V() – VPD, I() = 1 mA	0.4		1.5	V
007	Vc()lo	Clamp-Voltage lo	I() = -1 mA	-1.5		-0.3	V
Hall Sensors and Signal Conditioning							
101	Hext	Permissible Magnetic Field Strength	at chip surface	20		100	kA/m
102	fmag	Operating Magnetic Field Frequency				3.33	kHz
103	rpm	Rotating Speed of Magnet				200 000	rpm
104	dsens	Diameter of Hall Sensor Array			2		mm
105	xdis	Permissible Lateral Displacement of Magnet Axis to Center of Hall Sensors				0.2	mm
106	xpac	Displacement Chip Center to Package Center	package QFN28	-0.15		0.15	mm
107	ϕpac	Angular Alignment of Chip vs. Package	package QFN28	-3		+3	Deg
108	hpac	Displacement of Chip Surface to Package Surface	package QFN28		0.4		mm
109	Vos	Trimming Range of Output Offset Voltage	VOSS or VOSC = 0x7F			-55	mV
110	Vos	Trimming Range of Output Offset Voltage	VOSS or VOSC = 0x3F	55			mV
111	Vopt	Optimal Differential Output Voltage	Vopt = Vpp(PSIN) – Vpp(NSIN), ENAC = 0x0, see Figure 7		4		Vpp
112	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS), GCC = 0x3F	1.09			
113	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS), GCC = 0x40			0.92	
Signal Level Control							
201	Vpp	Differential Peak-to-Peak Output Amplitude	Vpp = Vpk(Px) – Vpk(Nx), ENAC = 0x1, see Figure 7	3.2		4.8	Vpp
202	ton	Controller Settling Time	to ±10 % of final amplitude			300	µs
203	Vt()lo	MINERR Amplitude Error Threshold	see Item No. 201	1.0		2.8	Vpp
204	Vt()hi	MAXERR Amplitude Error Threshold	see Item No. 201	4.8		5.8	Vpp
Bandgap Reference							
401	Vbg	Bandgap Reference Voltage		1.18	1.25	1.32	V
402	Vref	Reference Voltage		45	50	55	%VPA
403	Iibm	Bias Current	CIBM = 0x0 CIBM = 0xF bias current adjusted	 -370 -220	 -200	-100 -180	µA µA µA
404	VPDon	Turn-on Threshold VPD, System on	V(VPD) – V(VND), increasing voltage	3.65	4.0	4.3	V
405	VPDoff	Turn-off Threshold VPD, System reset	V(VPD) – V(VND), decreasing voltage	3	3.5	3.8	V
406	VPDhys	Hysteresis System on/reset		0.3			V

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDD = 5 V ±10 %, EP = VNA1 = VNA2 = VND, Tj = -40...125 °C, IBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
407	Vosr	Reference Voltage Offset Compensation		470	500	530	mV
Clock Generation							
501	f()sys	System Clock	bias current adjusted	0.8	1.0	1.2	MHz
502	f()sdc	Sine/Digital Converter Clock	bias current adjusted	13.65	16	19	MHz
Sine/Digital Converter							
601	RESsdc	Sine/Digital Converter Resolution			12		bit
602	AAabs	Absolute Angular Accuracy	Vpp() = 4 V, adjusted	-0.35		0.35	Deg
603	AArel	Relative Angular Accuracy	with reference to an output period at A, B. CFGRES = 0x0FF, ENF = 0x1, PRM = 0x0, GAING = 0x0, Vpp(SIN/COS) = 4 Vpp. see Figure 19		± 10		%
604	f()ab	Output Frequency at A, B	CFGMTD = 0x0, CFGRES = 0x3FF CFGMTD = 0x1, CFGRES = 0x3FF CFGMTD = 0x2, CFGRES = 0x3FF CFGMTD = 0x3, CFGRES = 0x3FF		4.0 2.0 0.5 0.125		MHz MHz MHz MHz
Serial Interface, Digital Outputs MA, SLO, SLI							
701	Vs(SLO)hi	Saturation Voltage hi	Vs(SLO)hi = V(VDD) − V(), I(SLO) = -4 mA			0.4	V
702	Vs(SLO)lo	Saturation Voltage lo	I(SLO)lo = 4 mA, with reference to GND			0.4	V
703	Isc(SLO)hi	Short-Circuit Current hi	V(SLO) = V(VDD), 25 °C	-60		-18	mA
704	Isc(SLO)lo	Short-Circuit Current lo	V(SLO) = V(GND), 25 °C	18		60	mA
705	tr(SLO)	Rise-Time	CL = 50 pF, rise 10 % to 90 %			60	ns
706	tf(SLO)	Fall-Time	CL = 50 pF, fall 90 % to 10 %			60	ns
707	Vt()hi	Threshold Voltage hi at MA, SLI	with reference to VND			2	V
708	Vt()lo	Threshold Voltage lo at MA, SLI	with reference to VND	0.8			V
709	Vt()hys	Threshold Hysteresis at MA, SLI		140	250		mV
710	Ipu(MA)	Pull-up Current	V() = 0...VPD − 1 V	-60	-30	-6	µA
711	Ipd(SLI)	Pull-down Current	V() = 1 V...VPD	6	30	60	µA
712	f(MA)	Permissible MA Clock Frequency				10	MHz
713	Ilk(SLO)tri	Tristate Leakage Current	reversed supply	-20		20	µA
Ports P0, P1, P2, P3 and Test PTE							
801	Vs()hi	Saturation Voltage hi at P0, P1, P2, P3	Vs()hi = V(VPD) − V(), I() = -4 mA			0.4	V
802	Vs()lo	Saturation Voltage lo at P0, P1, P2, P3	I() = 4 mA, with reference to VND			0.4	V
803	tr()	Rise-Time at P0, P1, P2, P3	CL = 50 pF, rise 10 % to 90 %			60	ns
804	tf()	Fall-Time at P0, P1, P2, P3	CL = 50 pF, fall 90 % to 10 %			60	ns
805	Vt()hi	Threshold Voltage hi	with reference to VND			2	V
806	Vt()lo	Threshold Voltage lo	with reference to VND	0.8			V
807	Vt()hys	Hysteresis	Vt()hys = Vt()hi − Vt()lo	140	250		mV
808	Ipd()	Pull-down Current	V() = 1 V...VPD	6	30	60	µA
Error Monitor NERR, NWARN							
901	Vs()lo	Saturation Voltage lo at NERR	I() = 4 mA , with reference to VND			0.4	V
902	Vt()hi	Input Threshold Voltage hi	with reference to VND			2	V
903	Vt()lo	Input Threshold Voltage lo	with reference to VND	0.8			V
904	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	140	250		mV
905	Ipu()	Pull-up Current Source at NERR	V(NERR) = 0...VPD − 1 V	-800	-300	-80	µA
906	Isc()lo	Short-Circuit Current lo at NERR	V(NERR) = V(VPD), Tj = 25°C		50	80	mA
907	tf()hilo	Delay Time at NERR	CL = 50 pF			60	ns
908	Ipu()	Pull-up Current at NWARN	V() = 0...VPD − 1 V	-60	-30	-6	µA

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDD = 5 V ±10 %, EP = VNA1 = VNA2 = VND, Tj = -40...125 °C, IBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Zapping VZAP							
A01	Vt()hi	Input Threshold Voltage hi	with reference to VND			2	V
A02	Vt()lo	Threshold Voltage lo	with reference to VND	0.8			V
A03	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo	140	250		mV
A06	V()zap	Zapping Voltage	PROG = '1'	6.9	7.0	7.1	V
A09	Rpd()	Pull-Down Resistor		30		55	kΩ
Incr Interface Line Driver Outputs A, B, Z, NA, NB, NZ							
P01	Vs()hi	Saturation Voltage hi	Vs() = VDD – V(); CFGDR(1:0) = 0x00, I() = -4 mA CFGDR(1:0) = 0x01, I() = -50 mA CFGDR(1:0) = 0x10, I() = -50 mA CFGDR(1:0) = 0x11, I() = -20 mA			 200 700 700 400	 mV mV mV mV
P02	Vs()lo	Saturation Voltage lo	with reference to GND; CFGDR(1:0) = 0x00, I() = -4 mA CFGDR(1:0) = 0x01, I() = -50 mA CFGDR(1:0) = 0x10, I() = -50 mA CFGDR(1:0) = 0x11, I() = -20 mA			 200 700 700 400	 mV mV mV mV
P03	Isc()hi	Short-Circuit Current hi	V() = GND; CFGDR(1:0) = 0x00 CFGDR(1:0) = 0x01 CFGDR(1:0) = 0x10 CFGDR(1:0) = 0x11	 -12 -125 -125 -60		 -4 -50 -50 -20	 mA mA mA mA
P04	Isc()lo	Short-Circuit Current lo	V() = VDD; CFGDR(1:0) = 0x00 CFGDR(1:0) = 0x01 CFGDR(1:0) = 0x10 CFGDR(1:0) = 0x11	 4 50 50 20		 12 125 125 60	 mA mA mA mA
P05	Ilk()tri	Tristate Leakage Current	TRIHL(1:0) = 0x11 or reversed supply	-20		20	µA
P06	tr()	Rise-Time lo to hi	RL = 100 Ω to GND; CFGDR(1:0) = 0x00 CFGDR(1:0) = 0x01 CFGDR(1:0) = 0x10 CFGDR(1:0) = 0x11	 5 5 50 5		 20 20 350 40	 ns ns ns ns
P07	tf()	Fall-Time hi to lo	RL = 100 Ω to VDD; CFGDR(1:0) = 0x00 CFGDR(1:0) = 0x01 CFGDR(1:0) = 0x10 CFGDR(1:0) = 0x11	 5 5 50 5		 20 20 350 40	 ns ns ns ns
Comm Interface Outputs U, V, W							
Q01	Vs()hi	Saturation Voltage hi	Vs() = VDD – V(); I() = -12 mA			400	mV
Q02	Vs()lo	Saturation Voltage lo	with reference to GND; I() = -12 mA			400	mV
Q03	Isc()hi	Short-Circuit Current hi	V() = GND	-60		-20	mA
Q04	Isc()lo	Short-Circuit Current lo	V() = VDD	20		60	mA
Q05	Ilk()tri	Tristate Leakage Current	reversed supply voltage	-20		20	µA
Q06	tr()	Rise Time	RL = 100 Ω to VDD	5		40	ns
Q07	tf()	Fall Time	RL = 100 Ω to GND	5		40	ns
Reverse Polarity Protection VPA, VPD, VNA1, VNA2, VND							
R01	Vs()	Saturation Voltage at VPA, VPD	Vs() = VDD – V(); I() = -10 . . . 0 mA			450	mV
R02	Vs()	Saturation Voltage at VNA1, VNA2, VND	Vs() = GND – V(); I() = -10 . . . 0 mA			450	mV

OPERATING REQUIREMENTS: Serial Interface

Operating conditions: VDD = 5 V ±10 %, Ta = -40...125 °C, IBM calibrated to 200 µA;
Logic levels referenced to VND: lo = 0...0.45 V, hi = 2.4 V...VPD

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI Protocol (ENSSI = 1)						
I001	T_{MAS}	Permissible Clock Period	t_{tos} according to Table 29	250	2x t_{tos}	ns
I002	t_{MASh}	Clock Signal hi Level Duration		25	t_{tos}	ns
I003	t_{MASl}	Clock Signal lo Level Duration		25	t_{tos}	ns
BiSS C Protocol						
I004	T_{MAS}	Permissible Clock Period	t_{tos} according to Table 29	100	2x t_{tos}	ns
I005	t_{MASh}	Clock Signal hi Level Duration		25	t_{tos}	ns
I006	t_{MASl}	Clock Signal lo Level Duration		25	t_{tos}	ns

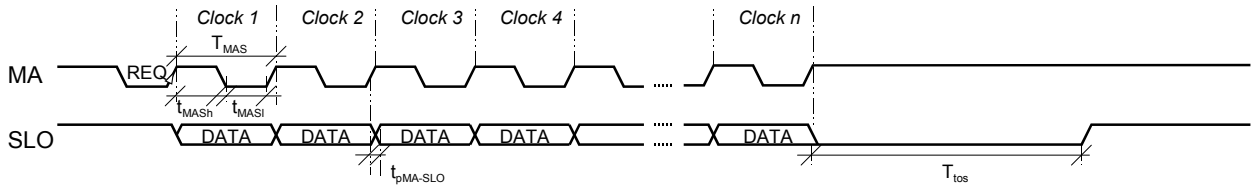


Figure 1: Timing diagram in SSI protocol.

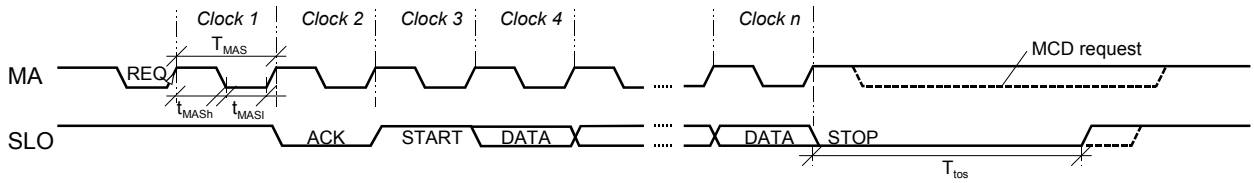


Figure 2: Timing diagram in BiSS C protocol.

REGISTERS

OVERVIEW

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Hall Signal Conditioning								
0x00 *z*	GAING(1:0)		GAINF(5:0)					
0x01 *z*	ENAC	GCC(6:0)						
0x02 *z*	ENF	VOSS(6:0)						
0x03 *z*	PRM	VOSC(6:0)						
0x04 *z*	DCS	DPU	-	ENADAP	CIBM(3:0)			
RS422 Driver								
0x05 *z*	ENSSI	CFGPROT	CFGMTD(1:0)		TRIHL(1:0)		CFGDR(1:0)	
Sine/Digital Converter								
0x06 *z*	CFGRES(7:0)							
0x07 *z*	CFGHYS(1:0)		CFGDIR	CFGSU	CFGAB(1:0)		CFGRES(9:8)	
0x08 *z*	CFGZPOS(7:0)							
0x09 *z*	CFGCOM(3:0)				CFGZPOS(11:7)			
0x0A *z*	-			HARMCAL(4:0)				
0x0B *z*	-							
0x0C *z*	-							
0x0D *z*	-							
Test Settings								
0x0E *p*	TEST(7:0)							
0x0F	ENHC	res.	res.	res.	res.	res.	res.	PROGZAP
ZAP Diodes (read only)								
0x10 .. 0x20	ZAP diodes for addresses 0x00..0x0D and 0x7D..0x7F							
not used								
0x21 .. 0x41	'invalid addresses'							
Profile Identification (read only)								
0x42	Profile - 0x2C							
0x43	Profile - 0x0				R_ST			
not used								
0x44 .. 0x74	'invalid address'							
Ports								
0x75	DIR3	DIR2	DIR1	DIR0	P3	P2	P1	P0
Status Messages (read only; messages will be set back during reading)								
0x76	GAIN							
0x77	PROGERR	ERRSDATA	ERRAMIN	ERRAMAX	ERREXT	WARNEXT	res.	PROGOK

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Identification (0x78 bis 0x7B read-only)								
0x78	Device ID - 0x4D ('M')							
0x79	Device ID - 0x48 ('H')							
0x7A	Revision - 0x67 ('g')							
0x7B	Revision - 0x32 ('2')							
0x7C	-							CFGTOS
0x7D *z*	Manufacturer Revision - 0x00							
0x7E *z*	Manufacturer ID - 0x00							
0x7F *z*	Manufacturer ID - 0x00							

z: Register value programmable by zapping

p: Register value write protected; can only be changed while V(VZAP)> Vt()hi

Table 5: Register layout

SENSOR PRINCIPLE

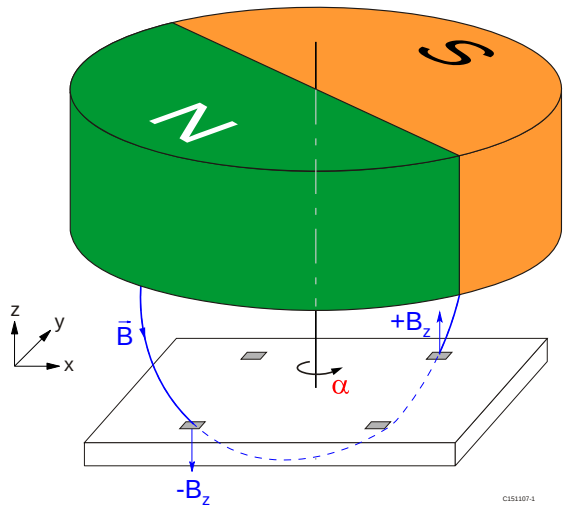


Figure 3: Sensor principle

In conjunction with a rotating permanent magnet, the iC-MH16 module can be used to create a complete encoder system. A diametrically magnetized, cylindrical permanent magnet made of neodymium iron boron (NdFeB) or samarium cobalt (SmCo) generates optimum sensor signals. The diameter of the magnet should be in the range of 3 to 6 mm.

The iC-MH16 has four Hall sensors adapted for angle determination and to convert the magnetic field into a measurable Hall voltage. Only the z-component of the magnetic field is evaluated, whereby the field lines pass through two opposing Hall sensors in the opposite direction. Figure 3 shows an example of field vectors. The arrangement of the Hall sensors is selected so that the mounting of the magnets relative to iC-MH16 is extremely tolerant. Two Hall sensors combined provide a differential Hall signal. When the magnet is rotated around the longitudinal axis, sine and cosine output voltages are produced which can be used to determine angles.

POSITION OF THE HALL SENSORS AND THE ANALOG SENSOR SIGNAL

The Hall sensors are placed in the center of the QFN28 package at 90 ° to one another and arranged in a circle with a diameter of 2 mm as shown in Figure 4.

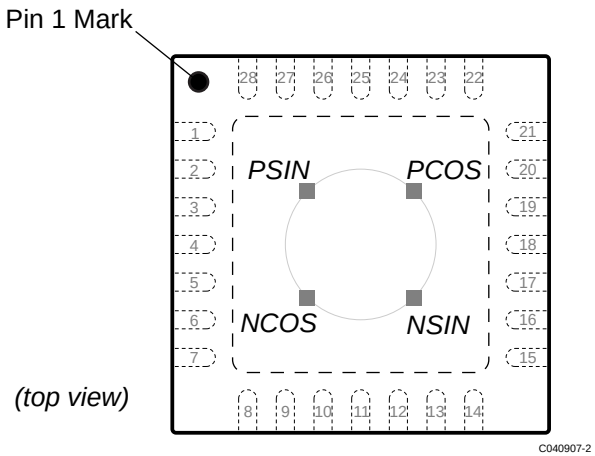


Figure 4: Position of the Hall sensors

In order to calculate the angle position of a diametrically polarized magnet placed above the device a difference in signal is formed between opposite pairs of Hall sensors, resulting in the sine being $V_{SIN} = V_{PSIN} - V_{NSIN}$ and the cosine $V_{COS} = V_{PCOS} - V_{NCOS}$. The zero angle position of the magnet is marked by the resulting cosine voltage value being at a maximum and the sine voltage value at zero.

This is the case when the south pole of the magnet is exactly above the PCOS sensor and the north pole is above sensor NCOS, as shown in Figure 5. Sensors PSIN and NSIN are placed along the pole boundary so that neither generate a Hall signal.

When a magnetic south pole comes close to the surface of the package the resulting magnetic field has a positive component in the +z direction (i.e. from the top of the package) and the individual Hall sensors each generate their own positive signal voltage.

When the magnet is rotated counterclockwise the poles then also cover the PSIN and NSIN sensors, resulting in the sine and cosine signals shown in Figure 6 being produced.

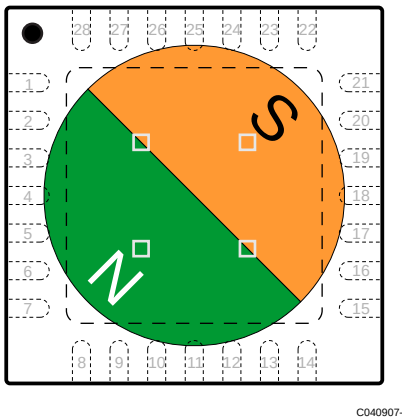


Figure 5: Zero position of the magnet

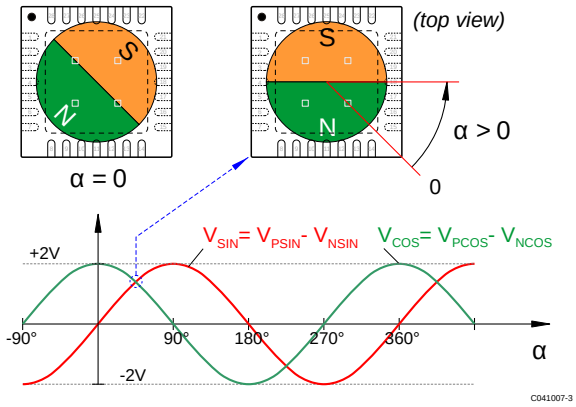


Figure 6: Pattern of the analog sensor signals with the angle of rotation

HALL SIGNAL PROCESSING

The iC-MH16 module has a signal calibration function for compensating signal and adjustment errors. The Hall signals are amplified in two stages. With the first amplifier stage the field strength within which the Hall sensor is operated is roughly selected. The first amplifier stage can be programmed in the following ranges:

GAING(1:0)	Addr. 0x00; bit 7:6
00	5-fold
01	10-fold
1-	20-fold

Table 6: Range selection for Hall signal amplification

The operating range can be specified in advance in accordance with the temperature coefficient and the magnet distance. The integrated amplitude control can vary the signal amplitude between 1 and 20 via another amplification factor. Should the signal amplitude reach the range limits, a different signal amplification must be selected via GAING.

GAINF(5:0)	Addr. 0x00; bit 5:0
0x00...0x02	1.098
0x03	1.150
...	$exp(\frac{ln(20)}{64} \cdot GAINF)$
0x3E...0x3F	18.213

Table 7: Hall signal amplification

The second amplifier stage can be varied in an additional range. With the amplitude control (ENAC = 0x0) deactivated, the amplification in the GAINF register is used. With the amplitude control (ENAC = 0x1) activated, the GAINF register bits have no effect.

GCC(6:0)	Addr. 0x01; bit 6:0
0x00	1.000
0x01	1.0015
...	$exp(\frac{ln(20)}{2048} \cdot GCC)$
0x3F	1.0965
0x40	0.9106
...	$exp(-\frac{ln(20)}{2048} \cdot (128 - GCC))$
0x7F	0.9985

Table 8: Amplification calibration cosine

The GCC register is used to correct the sensitivity of the sine channel in relation to the cosine channel. The cosine amplitude can be corrected within a range of approximately ±10 %.

ENAC	Addr. 0x01; bit 7
0	amplitude control deactivated
1	amplitude control active

Table 9: Activation of amplitude control

The integrated amplitude control can be activated with the ENAC bit. In this case the differential signal amplitude is adjusted to 4 Vss and the values of GAINF have no effect here.

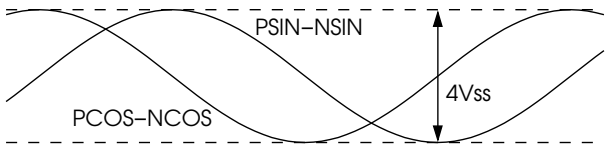


Figure 7: Definition of differential amplitude

After switch-on the amplification is increased until the setpoint amplitude is reached. The amplification is automatically corrected in case of a change in the input amplitude by increasing the distance between the magnet and the sensor, in case of a change in the supply voltage or a temperature change. The sine signals are therefore always converted into high-resolution quadrature signals at the optimum amplitude.

VOSS(6:0) Addr. 0x02; bit 6:0 **VOSC(6:0)** Addr. 0x03; bit 6:0	
0x00	0 mV
0x01	1 mV
...	...
0x3F	63 mV
0x40	0 mV
0x41	-1 mV
...	...
0x7F	-63 mV

Table 10: Offset calibration for sine and cosine

An offset in the sine or cosine signal can be corrected by the VOSS and VOSC registers. The output voltage can be shifted by ±63 mV in each case to compensate for the offset.

HARMCAL Addr. 0x0A; bit 4:0	
0x00	0 LSB
0x01	1 LSB
...	...
0x0F	15 LSB
0x10	0 LSB
0x11	-1 LSB
...	...
0x1F	-15 LSB

Table 11: Harmonic calibration

After calibration of offset and gain a residual error with four times period remains. This error can be reduced with the calibration parameter HARMCAL. The mode of operation shows Fig. 8.

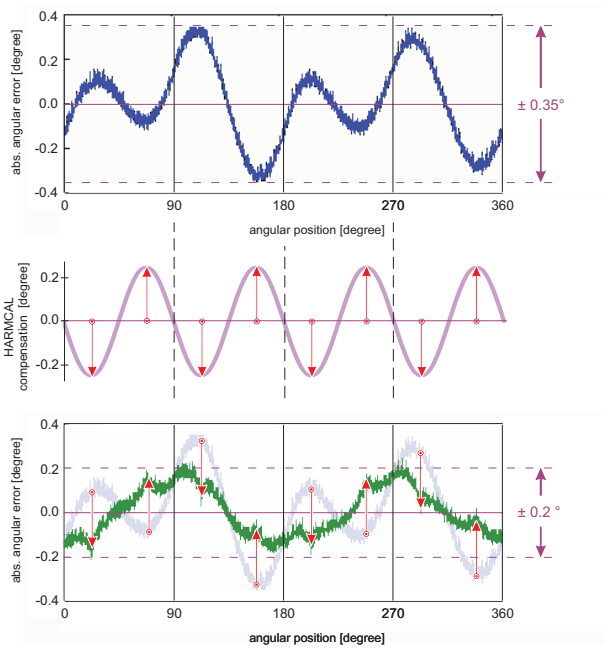


Figure 8: Harmonic calibration

ENF Addr. 0x02; bit 7	
Code	Description
0x0	16 kHz cutoff frequency
0x1	3 kHz cutoff frequency

Table 12: Filter

The amplifier cutoff frequency can be programmed with ENF.

PRM Addr. 0x03; bit 7	
0	Energy-saving mode deactivated
1	Energy-saving mode active

Table 13: Energy-saving mode

In the energy-saving mode the current consumption of the Hall sensors can be quartered. This also reduces the maximum rotating frequency by a factor of 4.

CIBM(3:0) Addr. 0x04; bit 3:0	
0x0	-40 %
...	...
0x8	0 %
0x9	+5 %
...	...
0xF	+35 %

Table 14: Calibration of bias current

The bias current is factory calibrated to 200 µA. The calibration can be verified in test mode (TEST = 0x43) by measuring the current from Pin B to Pin VNA.

TEST MODES FOR SIGNAL CALIBRATION

For signal calibration iC-MH16 has several test settings which make internal reference quantities and the amplified Hall voltages of the individual sensors accessible at external pins A, B, Z and NA for measurement purposes. This enables the settings of the offset (VOSS, VOSC), gain (GAING, GAINF) and amplitude ratio of the cosine to the sine signal (GCC) to be directly observed on the oscilloscope.

Test mode can be triggered by connecting pin VZAP to VPD and programming the TEST register (address 0x0E). The individual test modes are listed in the following table:

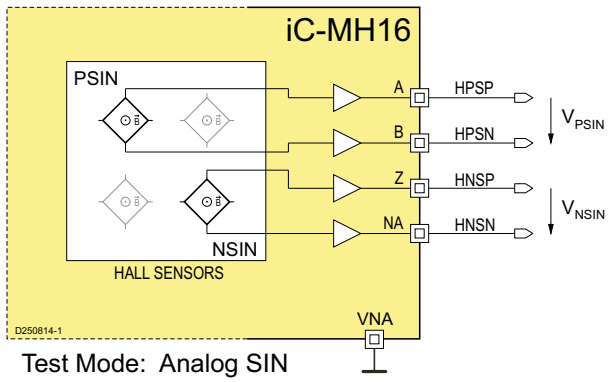
Output signals in test mode					
Mode	TEST	Pin A	Pin B	Pin Z	Pin NA
Normal	0x00	A	B	Z	U
Analog SIN	0x20	HPSP	HPSN	HNSP	HNSN
Analog COS	0x21	HPCP	HPCN	HNCP	HNCN
Analog OUT	0x22	PSIN	NSIN	PCOS	NCOS
Analog REF	0x43	VREF	IBM	VBG	VOSR
Digital CLK	0xC0	CLKD			

Table 15: Test modes and available output signals

The output voltages are provided as differential signals with an average voltage of 2.5 V. The gain is determined by register values GAING and GAINF and should be set so that output amplitudes from the sine and cosine signals of about 1 V are visible.

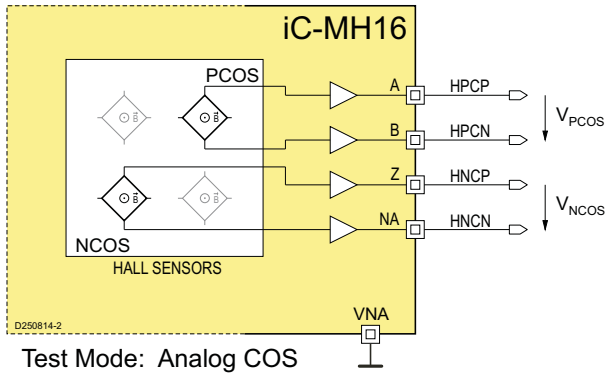
Test modes Analog SIN and Analog COS
In these test modes it is possible to measure the signals from the individual Hall sensors independent of one another. The name of the signal is derived from the sensor name and position. **HPSP**, for example, is the (amplified) **H**all voltage of sensor **PS**IN at the **p**ositive signal path; similarly, **HNCN** is the **H**all voltage of sensor **NC**OS at the **n**egative signal path. The effective Hall voltage is accrued from the differential voltage between the positive and negative signal paths of the respective sensor.

Test mode Analog OUT
In this test mode the sensor signals are available at the outputs as they would be when present internally for further processing on the interpolator. The interpolation accuracy which can be obtained is determined by the quality of signals V_{sin} and V_{cos} and can be influenced in this particular test mode by the calibration of the offset, gain and amplitude ratio.



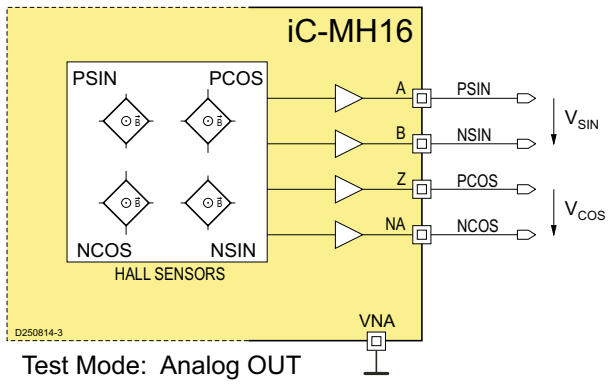
Test Mode: Analog SIN

Figure 9: Output signals of the sine Hall sensors in test mode Analog SIN



Test Mode: Analog COS

Figure 10: Output signals of the cosine Hall sensors in test mode Analog COS



Test Mode: Analog OUT

Figure 11: Differential sine and cosine signals in test mode Analog OUT

Test mode Analog REF
In this mode various internal reference voltages are provided. VREF is equivalent to half the supply voltage (typically 2.5 V) and is used as a reference voltage for the Hall sensor signals. VBG is the internal bandgap reference (1.24 V), with VOSR (0.5 V) used to gener-

ate the range of the offset settings. Bias current IBM determines the internal current setting of the analog circuitry. In order to compensate for variations in this current and thus discrepancies in the characteristics of the individual iC-MH16 devices (due to fluctuations in production, for example), this can be set within a range of -40 % to +35 % using register parameter CIBM. The nominal value of 200 µA is measured as a short-circuit current at pin B to ground.

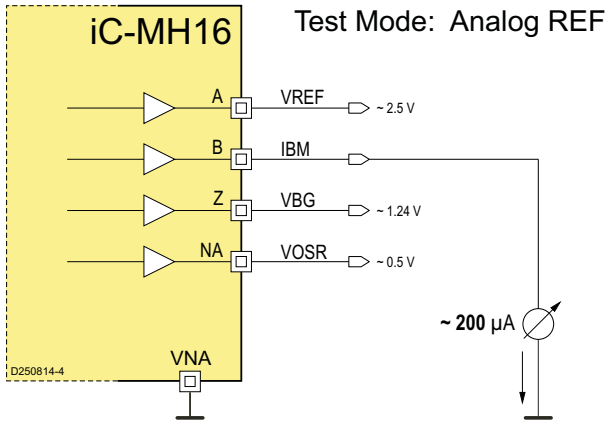


Figure 12: Setting bias current IBM in test mode Analog REF

Test mode Digital CLK
If, due to external circuitry, it is not possible to measure IBM directly, by way of an alternative clock signal CLKD at pin A can be calibrated to a nominal 1 MHz in this test mode via register value CIBM.

CALIBRATION PROCEDURE

The calibration procedure described in the following applies to the optional setting of the internal analog sine and cosine signals and the mechanical adjustment of the magnet and iC-MH16 in relation to one another.

BIAS setting
The BIAS setting compensates for possible manufacturing tolerances in the iC-MH16 devices. A magnetic field does not need to be present for this setting which can thus be made either prior to or during the assembly of magnet and iC-MH16.

If the optional setup process is not used, register CIBM should be set to an average value of 0x8 (which is equivalent to a change of 0 %). As described in the previous section, by altering the value in register CIBM in test mode Analog REF current IBM is set to 200 µA or, alternatively, in test mode Digital CLK signal CLKD is set to 1 MHz.

Mechanical adjustment
iC-MH16 can be adjusted in relation to the magnet in test modes Analog SIN and Analog COS, in which the Hall signals of the individual Hall sensors can be observed while the magnet rotates.

In test mode Analog SIN the output signals of the sine Hall sensors which are diagonally opposite one another are visible at pins A, B, Z and NA. iC-MH16 and the magnet are then adjusted in such a way that differential signals V_{PSIN} and V_{NSIN} have the same amplitude and a phase shift of 180 °. The same applies to test mode Analog COS, where differential signals V_{PCOS} and V_{NCOS} are calibrated in the same manner.

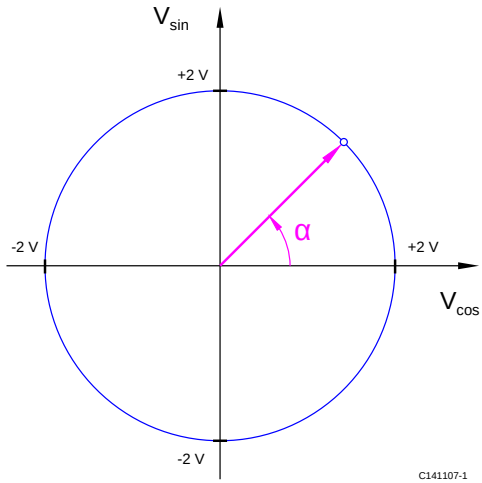


Figure 13: Ideal Lissajous curve

Calibration using analog signals
In test mode Analog OUT as shown in Figure 6 the internal signals which are transmitted to the sine/digital converter can be tapped with high impedance. With a rotating magnet it is then possible to portray the differential signals V_{SIN} and V_{COS} as an x-y graph (Lissajous curve) with the help of an oscilloscope. In an ideal setup the sine and cosine analog values describe a perfect circle as a Lissajous curve, as illustrated by Figure 13.

At room temperature and with the amplitude control switched off (ENAC = 0x0) a rough GAING setting is selected so that at an average fine gain of GAINF = 0x20 (a gain factor of ca. 4.5) the Hall signal amplitudes are as close to 1 V as possible. The amplitude can then be set more accurately by varying GAINF. Variations in the gain factor, as shown in Figure 14, have no effect on

the Lissajous curve, enabling the angle information for the interpolator to be maintained.

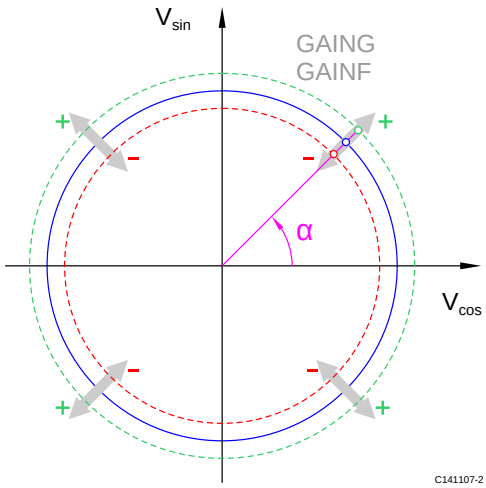


Figure 14: Effect of gain settings GAING and GAINF

Deviations of the observed Lissajous curve from the ideal circle can be corrected by varying the amplitude offset (register VOSS, VOSC) and amplitude ratio (register GCC). Changes in these parameters are described in the following figures 15 to 17. Each of these settings has a different effect on the interpolated angle value. A change in the sine offset thus has a maximum effect on the angle value at 0 ° and 18 °, with no alterations whatsoever taking place at angles of 90 ° and 270 °. When varying the cosine offset exactly the opposite can be achieved as these angle pairs can be set independent of one another. Setting the cosine/sine amplitude ratio does not change these angles (0 °, 90 °, 180 ° and 270 °); however, in-between values of 45 °, 135 °, 225 ° and 315 ° can still be influenced by this parameter.

Once calibration has been carried out a signal such as the one illustrated in Figure 13 should be available.

In the final stage of the process the amplitude control can be switched back on (ENAC = 0x1) to enable deviations in the signal amplitude caused by variations in the magnetic field due to changes in distance and temperature to be automatically controlled.

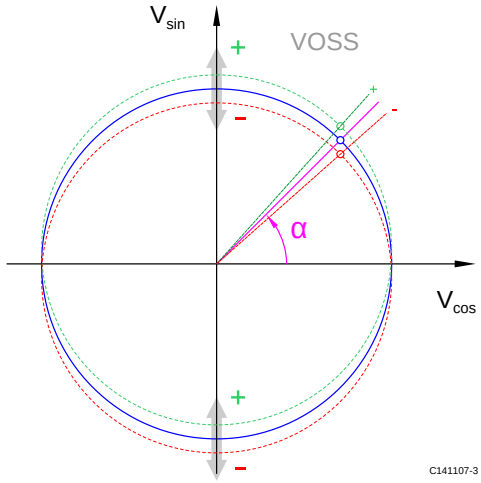


Figure 15: Effect of the sine offset setting

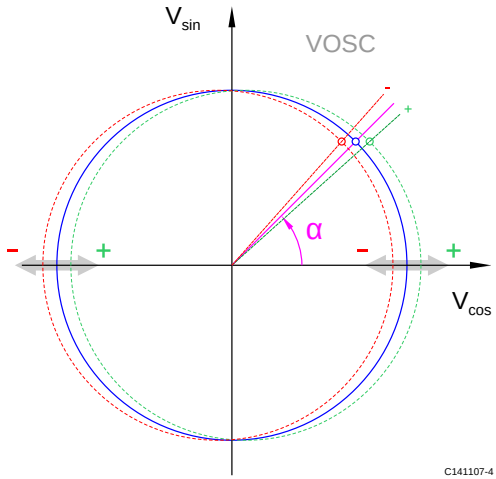


Figure 16: Effect of the cosine offset setting

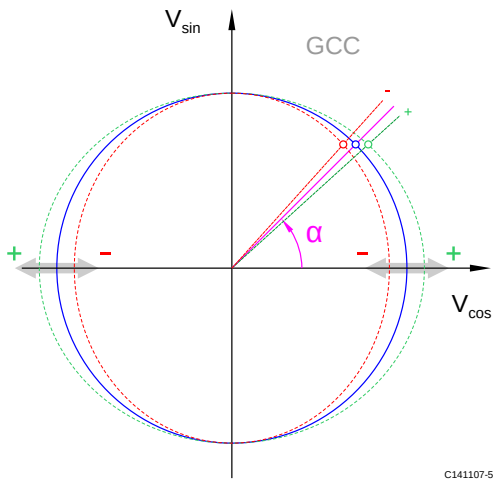


Figure 17: Effect of the amplitude ratio

Calibration using incremental signals

If test mode cannot be used, signals can also be calibrated using the incremental signals or the values read out serially. In order to achieve a clear relationship between the calibration parameters which have an effect on the analog sensor signals and the digital sensor values derived from these, the position of the zero pulse should be set to ZPOS = 0x0 and the rotating direction should be set to CFGDIR = 0x0, so that the digital signal starting point matches that of the analog signals.

At an incremental resolution of 8 edges per revolution (CFGRES = 0x01) those angle values can be displayed at which calibration parameters VOSS, VOSC and GCC demonstrate their greatest effect. When rotating the magnet at a constant angular speed the incremental signals shown in Figure 18 are achieved, with which the individual edges ideally succeed one another at a temporal distance of an eighth of a cycle (a 45 ° angle distance). Alternatively, the angle position of the magnet can also be determined using a reference encoder, rendering an even rotational action unnecessary and allowing calibration to be performed using the available set angle values.

The various possible effects of parameters VOSS, VOSC and GCC on the flank position of incremental signals A and B are shown in Figure 18. Ideally, the distance of the rising edge (equivalent to angle positions of 0 ° and 180 °) at signal A should be exactly half a period (PER). Should the edges deviate from this in distance, the offset of the sine channel can be adjusted using VOSS. The same applies to the falling edges of the A signal which should also have a distance of half a period; deviations can be calibrated using the offset of cosine parameter VOSC. With parameter GCC the distance between the neighboring flanks of signals A and B can then be adjusted to the exact value of an eighth of a cycle (a 45 ° angle distance).

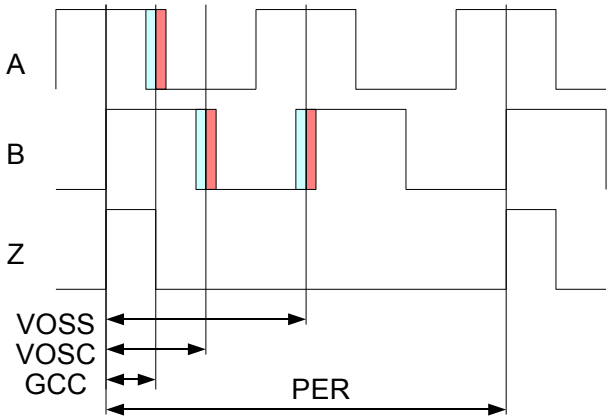


Figure 18: Calibration using incremental signals

SINE/DIGITAL CONVERTER

The iC-MH16 module integrates a high-resolution sine/digital converter. In the highest output resolution with an interpolation factor of 1 024, 4 096 edges per rotation are generated and 4 096 angular steps can be differentiated. Even in the highest resolution, the absolute position can be calculated in real time at the maximum speed depending on CFGMTD. After programming a register at address 4 to 9, a module reset is triggered internally and the absolute position is recalculated.

The resolution of the incremental output signals is programmed with CFGRES. The value of the 12-bit sine/digital converter is available in a resolution according to CFGRES via the serial interface.

CFGRES(7:0) Addr. 0x06; bit 7:0 **CFGRES(9:8)** Addr. 0x07; bit 1:0	
0x000	1
0x001	2
...	...
0x07E	127
0x07F	128
...	...
0x0FE	255
0x0FF	256
...	...
0x1FE	511
0x1FF	512
...	...
0x3FE	1023
0x3FF	1024

Table 16: Programming interpolation factor

If the magnet is mounted on top of the chip and turned counter clockwise, then cosine is leading sine and the digital output value increases. For incremental output, A is assigned to sine and B is assigned to cosine.

CFGAB(1:0) Addr. 0x07; bit 3:2	
0x0	A and B not inverted
0x1	A normal, B inverted
0x2	A inverted, B normal
0x3	A and B inverted

Table 17: Inversion of AB signals

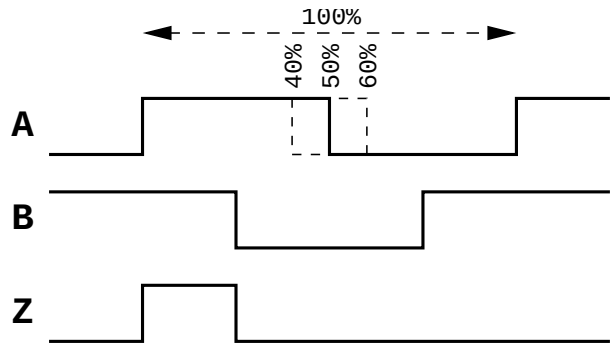


Figure 19: ABZ signals and relative accuracy

The incremental signals can be inverted again independently of the output drivers. As a result, other phase angles of A and B relative to the index pulse Z can be generated. The standard is A and B high level for the zero point, i.e. Z is equal to high.

Figure 19 shows the position of the incremental signals around the zero point. The relative accuracy of the edges to each other at a resolution setting of 10 bit is better than 10 %. This means that, based on a period at A or B, the edge occurs in a window between 40 % and 60 %.

CFGHYS(1:0) Addr. 0x07; bit 7:6	
0x0	0 °
0x1	0.17 °
0x2	0.35 °
0x3	0.7 °

Table 18: Programming angular hysteresis

With rotating direction reversal, an angular hysteresis prevents multiple switching of the incremental signals at the reversing point. The angular hysteresis corresponds to a slip which exists between the two rotating directions. However, if a switching point is approached from the same direction, then the edge is always generated at the same position on the output. The following Figure shows the generated quadrature signals for a resolution of 360 edges per rotation (interpolation factor 90) with hysteresis.

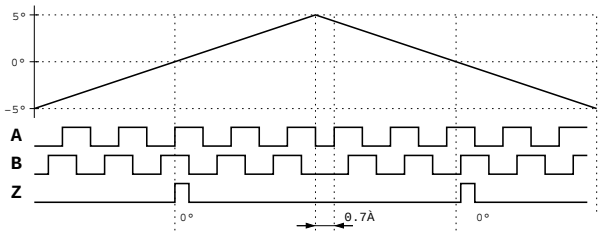


Figure 20: Quadrature signals for rotating direction reversal with hysteresis (CFGDIR = 0)

At the reversal point at +10 °, first the corresponding edge is generated at A. As soon as an angle according to the hysteresis has been exceeded in the other direction, the return edge is generated at A again first. This means that all edges are shifted by the same value in the rotating direction.

CFGZPOS(7:0) Addr. 0x08; bit 7:0 **CFGZPOS(11:8)** Addr. 0x09; bit 3:0	
0x0	0 °
0x1	0.08 °
0x2	0.16 °
...	$\frac{360}{4096}$ ·CFGZPos
0xff	359.9 °

Table 19: Programming zero position

The zero position can be set in 0.08 ° steps. It is valid for the quadrature and commutation signals. An 12-bit register is provided for this purpose, which can shift the Z-pulse once over 360 °.

CFGMTD(1:0) Addr. 0x05; bit 5:4	
0	62.5 ns
1	125 ns
2	500 ns
3	2 µs

Table 20: Minimum edge spacing

The CFGMTD register defines the time in which two consecutive position events can be output at the highest resolution. The default is a maximum output frequency of 500 kHz on A. This means that at the highest resolution, speeds of 25 000 rpms can still be correctly shown. In the setting with an edge spacing of 62.5 ns, the edges can be generated even at the highest revolution and the maximum speed. However, the counter connected to the module must be able to correctly process all edges in this case. The settings with 2 µs can be used for slower counters. It should be noted then, however, that the maximum rotation speed is reduced.

CFGDIR Addr. 0x07; bit 5	
0	Rotating direction CCW
1	Rotating direction CW

Table 21: Rotating direction reversal

The rotating direction can easily be changed with the bit CFGDIR. When the setting is CCW (counter-clockwise, CFGDIR = 0x0) the resulting angular position values will increase when rotation of the magnet is performed as shown in Figure 6. To obtain increasing angular position values in the CW (clockwise) direction, CFGDIR then has to be set to 0x1.

The internal analog sine and cosine signal which are available in test mode are not affected by the setting of CFGDIR. They will always appear as shown in Figure 6.

CFGSU Addr. 0x07; bit 4	
0	ABZ output "111" during startup
1	AB instantly counting to actual position

Table 22: Configuration of output startup

Depending on the application, a counter cannot bear generated pulses while the module is being switched on. When the supply voltage is being connected, first the current position is determined. During this phase, the quadrature outputs are constantly set to "111". In the setting CFGSU = 0x1, edges are generated at the output until the absolute position is reached. This enables a detection of the absolute position with the incremental interface.

The converter for the generation of the commutation signals can be configured for up to 16 pole pair motors. Three rectangular signals each with a phase shift of 120 ° are generated. With a two pole pair setting, the commutation sequence is generated twice per rotation.

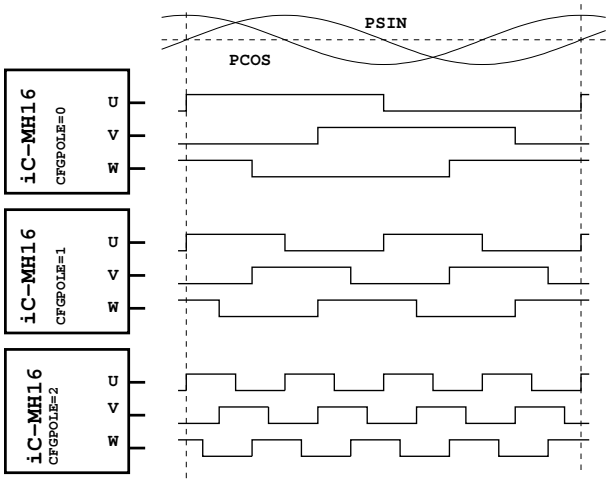


Figure 21: UVW signals for different settings of CFG-COM

CFGCOM(1:0)	Addr. 0x9; bit 7:4
0x0	1 pole pair commutation
0x1	2 pole pair commutation
...	...
0xF	16 pole pair commutation

Table 23: Commutation

The commutation signals, which has a much shorter latency, are synchronized to the sine/digital converter.

For an autonomous and torque optimized motor commutation it is recommended, to deactivate the synchronization with the parameter DCS.

DCS	Addr. 0x5; bit 7
0	Commutation signal synchronization enabled
1	Commutation signal synchronization disabled

Table 24: Synchronization of commutation signals

After changing the direction of rotation, the commutation signal which appears within 0.7 ° after the reversal point is shifted; the distance between two consecutive transitions is max. 0.7 ° shorter. At constant direction no systematical error occurs.

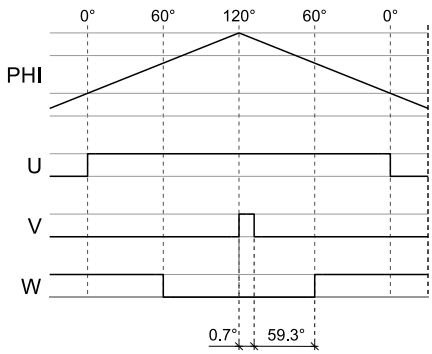


Figure 22: Hysteresis for UVW signals

OUTPUT DRIVERS

Three RS422-compatible output drivers for the incremental signals **A - NA**, **B - NB** and **Z - NZ** are available.

The property of the RS422 driver of the connected line can be adjusted in the CFGDR register.

CFGDR(1:0)	Addr. 0x05; bit 1:0
0x00	10 MHz 4 mA (default)
0x01	10 MHz 60 mA
0x10	300 kHz 60 mA
0x11	3 MHz 20 mA

Table 25: Driver property for incremental signals

Signals with the highest frequency can be transmitted in the setting CFGDR = 0x00. The driver capability is at least 4 mA, however it is not designed for a 100 Ω line. This mode is ideal for connection to a digital input on the same assembly. With the setting CFGDR = 0x01 the same transmission speed is available and the driver power is sufficient for the connection of a line over a short distance. Steep edges on the output enable a high transmission rate. A lower slew rate is offered by the setting CFGDR = 0x10, which is excellent for longer lines in an electromagnetically sensitive environment. Use of the setting CFGDR = 0x11 is advisable at medium transmission rates with a limited driver capability.

TRIHL	Addr. 0x05; bit 3:2
0x00	Push, pull output stage
0x01	Highside driver
0x10	Lowside driver
0x11	Tristate

Table 26: Tristate Register for incremental signals

The drivers consist of a push-pull stage in each case with low-side and high-side drivers which can each be activated individually. As a result, open-drain outputs with an external pull-up resistor can also be realized.

REVERSE POLARITY PROTECTION

The line drivers in iC-MH16 are short-circuit-proof and protected against reverse polarity. A defective connecting cable within the module or an incorrectly connected wire damages neither iC-MH16 nor the devices protected against reverse polarity by VPA, VPD and VNA1,VNA2,VND. The following pins are protected against reverse polarity: A, B, Z, NA, NB, NZ, U, V, W, MA, SLI and SLO.

Boundary conditions: Pins VNA1, VNA2, VND may only be charged to VPA, VPD. The maximum voltage difference between the pins must not exceed 6 V.

If the reverse polarity feature is not required, pins VPA and VPD have to be connected directly to VDD while VNA1, VNA2 and VND have to be connected to GND.

SERIAL INTERFACE: BiSS C protocol

The serial interface operates in BiSS C protocol mode and enables sensor data to be output in uninterruptible cycles (data channel SCD). At the same time parameters can be exchanged via bidirectional register communication (data channel CD).

The sensor data produced by iC-MH16 contains the binary coded angle value (ST) with 12 bits, two status bits (nE and nW) and 6 CRC bits (CRC). In case of lower resolution the angle data is left aligned and filled-up with zero. The low-active error bit nE a 0x0 indicates an error which can be further identified by reading the status register. The following bit nW corresponds to the state of the NWARN pad. The status bits are latched, until readout via single cycle data. The 6 CRC bits are calculated over ST(11:0), nE and nW with the polynom 0x43, the start value zero and inverted transmitted.

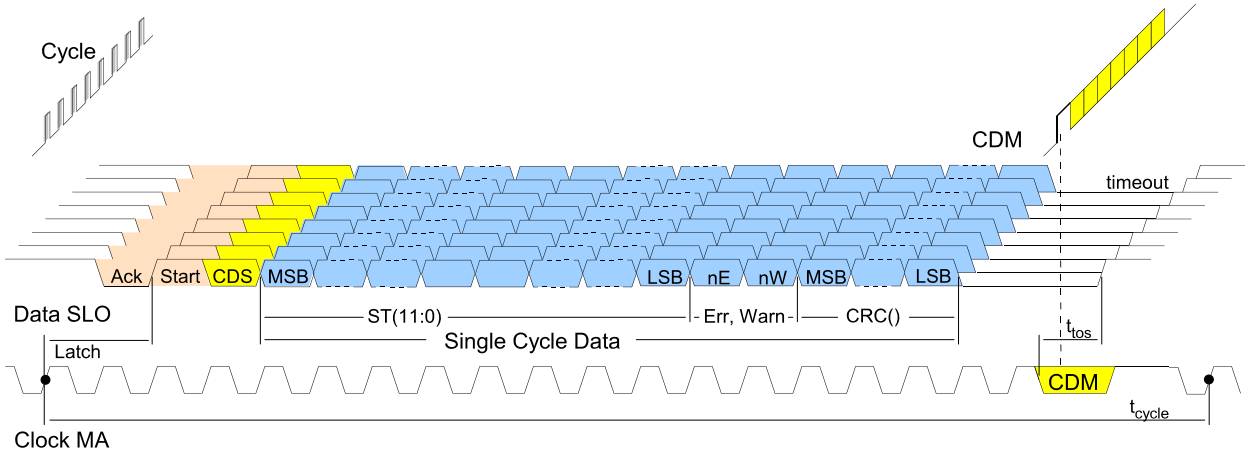


Figure 23: Example line signals (BiSS C)

Single Cycle Data Channel: SCD		
Bits	Typ	Label
12	DATA	Angle data ST(11:0) (singleturn position)
1	ERROR	Error bit nE (low active)
1	ERROR	Warning bit nW (low active)
6	CRC	Polynomial 0x43 $x^6 + x^1 + x^0$ (inverted bit output)

Table 27: BiSS data channels

CFGTOS	Adr 0x7C, bit 0		
Code	Clock	Timeout t_{tos}	fclk(MA) min*
0x0	19-20	ca. 20 µs	50 kHz
0x1	3-4	ca. 3.5 µs	300 kHz
ENADAP	Addr 0x04, bit 4		
0x0	see CFGTOS		
0x1	adaptive with $T_{CLK} = \frac{1.33}{f()sys}$	see BiSS specification	50 kHz
Notes	A ref. clock count is equal to f()sys (see El. Char., Item No. 501).		

Table 29: Timeout configuration

Interface Parameters With BiSS C Protocol

ENSSI	Addr. 0x05; bit 7	
Code	Protocol	Information
0 1	BiSS C SSI	BiSS INTERFACE www.biss-interface.com

Table 28: Protocol version

Short BiSS Timeout

If the adaptive timeout is not used, iC-MH16 has a short BiSS timeout function regardless of register protection settings according to the description of the BiSS C protocol (see Page 19, Table 2, El. Char., Item No. 6). The timeout can be programmed to a shorter value with the CFGTOS bit. However, this setting is reset to the default value 20 µs again following a reset.

Register Communication

iC-MH16 uses standard BiSS C register mapping with one bank for addresses 0x00 to 0x3F; Bank select is not implemented.

The register range 0x00..0x0F is equivalent to the settings with which the IC can be parameterized. The settings directly affect the corresponding switching parts. The range 0x10..0x20 is read-only and reflects the contents of the integrated zapping diodes. Following programming the data can be verified via these addresses. After the supply voltage is connected, the contents of the zapping diodes are copied to the RAM area 0x00..0x0D and 0x7D..0x7F. Then the settings can be overwritten via the serial interface. Overwriting is not possible if the CFGPROT bit is set.

With the profile ID, the data format can be requested for the following sensor data cycles in the module. A read operation at address 0x42 results in 0x2C, which is the equivalent to 12-bit single-cycle data. The address 0x43 contains the number of significant singleturn bits R_ST depending on the resolution. The registers 0x7D to 0x7F are reserved for the manufacturer and can be provided with an ID so that the manufacturer can identify its modules.

The port register at address 0x75 allows read and write access to the ports P0 to P3. The reset value is 0x00.

Px	Addr. 0x75; bit 3:0	0x0
0	low	
1	high	

Table 30: Port Value

DIRx	Addr. 0x75; bit 7:4	0x0
0	input	
1	output	

Table 31: Port Direction

The gain register at address 0x76 contains the actual value of the amplitude control. This value multiplied with GAING results in the complete gain.

GAIN(7:0)	Addr. 0x76; bit 7:0
0x00...0x08	1,098
...	$exp(\frac{ln(20)}{256} \cdot GAINF)$
0xF8...0xFF	18,213

Table 32: Hall signal amplification

The status register at address 0x77 provides information on the status of the module. The information resets after reading.

Internal Reset Function
A write access at RAM address 0x04..0x09 triggers an internal reset.

SERIAL INTERFACE: SSI protocol

In the SSI mode the absolute position is output with 13 bits according to the SSI standard. (The data is transmitted as Gray code with trailing zeros.)

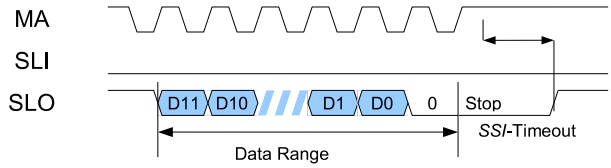


Figure 24: SSI protocol, data GRAY-coded

ENSSI	Addr. 0x05; bit 7
0	BiSS C
1	SSI

Table 33: Protocol version

Register transfer is not possible in SSI-Mode. The BiSS mode must be forced by applying V(VZAP) = V()ZAP before changing the value of bit ENSSI to avoid an aborted register communication.

ERROR HANDLING

Errors in the module are signaled via the error message output NERR. This open-drain output signals an error if the output is pulled against VND. If the error condition no longer exists, then the pin is released again after a waiting time of approximately 1 ms. If the integrated pull-up resistor is deactivated with DPU = 0x1, then an external resistor must be provided. With DPU = 0x0 it brings the pin up to the high level again.

DPU	Addr. 0x04; bit 6
0	Pull-up activated
1	Pull-up deactivated

Table 34: Activation of NERR pull-up

The status register provides information on the status of the module. There are 5 different errors that can be signaled. Following unsuccessful programming of the zapping diodes, the bit PROGERR is set. If an attempt is made to read the current position via the serial interface during the start-up phase, an error is signaled with ERRSDATA, as the actual position is not yet known. The ERRAMAX bit is output to signal that the amplitude is too high, while the ERRAMIN bit signals an amplitude which is too low, caused, for example, by too great a distance to the magnet. If the NERR pin is pulled against VND outside the module, this error is also signaled via the serial interface. The ERREXT bit is then equal to 0x1. The error bits are reset again after the status register is read out at the address 0x77. The error bit in the data word is then also read in the next cycle as 0x0.

OTP PROGRAMMING

CFGPROT	Addr. 0x05; bit 6
0	no protection
1	write/read protection

Table 35: Write/read protection of configuration

ENHC	Addr. 0x0F; bit 7
0	Default setting
1	ZAP diode testing: Use a higher current for reading the ZAP diodes memory (0x10-0x1F)

Table 36: Enable High Current

With CFGPROT = 0x0, the registers at the addresses 0x00..0x0F, 0x75 and 0x78..0x7F are readable and writeable. The addresses 0x10..0x1F, 0x42..0x43 and 0x76..0x77 are read-only. With CFGPROT = 0x1, all registers except the addresses 0x75 and 0x7C are write-protected; the addresses 0x42..0x42 and 0x75..0x7F are readable, while all others are read-protected.

An internal programming algorithm for the ZAP diodes is started by setting the bit PROGZAP. This process can only be successful if the voltage at VZAP is greater than 6.5 V and the test register TEST (2:0) is not set. Following programming, the register is reset internally again. In the process, the bit PROGOK is set in the status register (address 0x77) when programming is successful, and the bit PROGERR if it is not.

The ZAP memory can be tested by reading the register range 0x10-0x20. This test can be done with a higher readout current (bit ENHC = 0x1) to simulate deteriorated working conditions.

For reliable ROM writing, a low impedance connection path must be established for the VZAP blocking capacitor (about 100 nF) between pin VZAP and pin VNA2 to ensure stable VZAP voltage during programming. A further capacitor of 10 µF which may be located externally (e.g. on the programming board) is recommended for additional blocking purpose.

ORDERING INFORMATION

Type	Package	Order Designation
iC-MH16	QFN28	iC-MH16 QFN28-5x5

Please send your purchase orders to our order handling team:

Fax: +49 (0) 61 35 - 92 92 - 692
E-Mail: dispo@ichaus.com

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