

# iC-LFL1402

256x1 LINEAR IMAGE SENSOR

## FEATURES

- ◆ 256 active photo pixels of  $56\ \mu\text{m}$  at a gap and distortion free pitch of  $63.5\ \mu\text{m}$  (400 DPI)
- ◆ Integrating L-V conversion followed by a sample & hold circuit
- ◆ High sensitivity and uniformity over wavelength
- ◆ High clockrates of up to 5 MHz
- ◆ Only 256 clocks required for readout
- ◆ Shutter function enables flexible integration times
- ◆ Glitch-free analogue output
- ◆ Push-pull output amplifier
- ◆ 5 V single supply operation
- ◆ Can run off external bias to reduce power consumption
- ◆ Function equivalent to TSL1402 (serial mode)

## APPLICATIONS

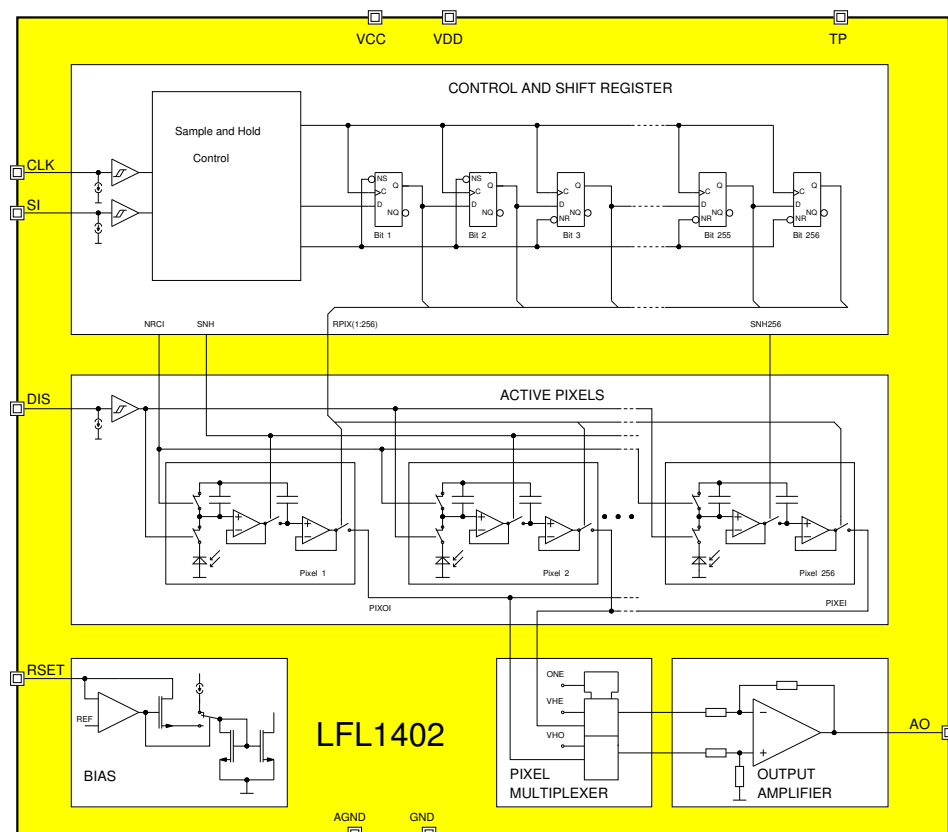
- ◆ Optical line sensors
- ◆ CCD substitute

## PACKAGES



OBGA™ LFL1C

## BLOCK DIAGRAM



# iC-LFL1402

256x1 LINEAR IMAGE SENSOR

preliminary



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## DESCRIPTION

iC-LFL1402 is an integrating light-to-voltage converter with a single line of 256 pixels pitched at  $63.5\mu\text{m}$  (center-to-center distance). Due to the monolithic integration there is no pixel-gap or pitch distortion whatsoever. Each pixel consists of a  $56.4\mu\text{m} \times 200\mu\text{m}$  photodiode, an integration capacitor and a sample and hold circuit.

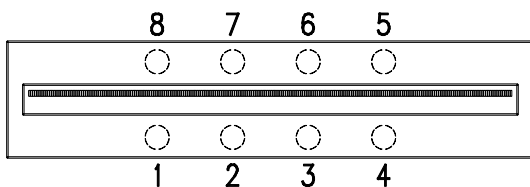
The integrated control logic makes operation very simple, with only a start and clock signal necessary. A third control input enables the integration period to be prematurely terminated at any time (electronic shutter).

When the start signal is given the hold mode is activated for all pixels simultaneously with the next rising clock edge; starting with pixel 1 the hold voltages are switched in sequence to the push-pull output amplifier. The second clock pulse deletes all integration capacitors and the integration period starts again in the background during the output phase. A run is complete after 256 clock pulses.

iC-LFL1402 is suitable for high clock rates of up to 5 MHz. If this is not required the supply current can be reduced via the external bias setting.

## PACKAGES OBGA™ LFL1C

### PIN CONFIGURATION OBGA™ LFL1C (top view)



### PIN FUNCTIONS

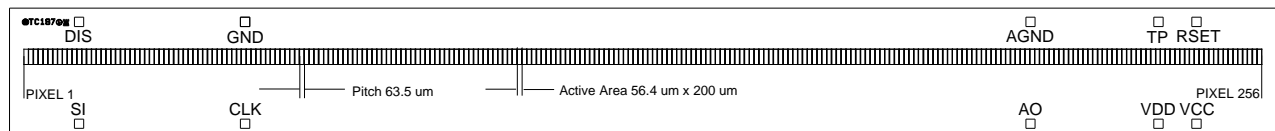
#### No. Name Function

- |   |      |  |
|---|------|--|
| 1 | SI   | Start Integration Input  |
| 2 | CLK  | Clock Input  |
| 3 | AO   | Analogue Output  |
| 4 | VCC  | +5 V Supply Voltage  |
| 5 | RSET | Bias Current (resistor from VCC to RSET; when connected to GND the internal bias setting is activated) |
| 6 | AGND | Analogue Ground  |
| 7 | GND  | Digital Ground   |
| 8 | DIS  | Disable Integration Input  |

## CHIP-LAYOUT

### iC-LFL1402

Chip size: 16.6 mm x 1.7 mm



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### ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Fig.	Limits		Unit
					Min.	Max.	
G001	VDD	Digital Supply Voltage			-0.3	6	V
G002	VCC	Analogue Supply Voltage			-0.3	6	V
G003	V()	Voltage at SI, CLK, DIS, RSET, TP, AO			-0.3	VCC + 0.3	V
G004	I()	Current in RSET, TP, AO			-10	10	mA
G005	Vd()	ESD Susceptibility at all pins	MIL-STD-883, Method 3015, HBM 100pF/1.5kΩ			2	kV
G006	Tj	Operating Junction Temperature			-40	125	°C
G007	Ts	Storage Temperature Range	see package specification OBGA™ LFL1C				

### THERMAL DATA

Operating Conditions: VCC = VDD = 5 V ±10%

Item No.	Symbol	Parameter	Conditions	Fig.	Limits			Unit
					Min.	Typ.	Max.	
T01	Ta	Operating Ambient Temperature Range	see package specification OBGA™ LFL1C					

All voltages are referenced to ground unless otherwise stated.

All currents into the device pins are positive; all currents out of the device pins are negative.



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## OPTICAL CHARACTERISTICS: Diagrams

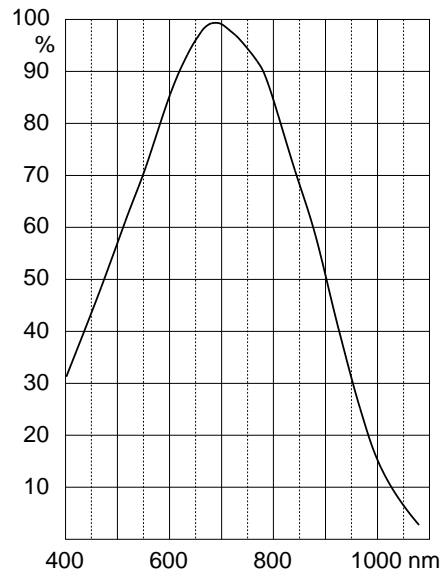


Figure 1: Relative spectral sensitivity

## OPERATING REQUIREMENTS: Logic

Operating Conditions:  $V_{CC} = V_{DD} = 5\text{ V} \pm 10\%$ ,  $T_j = -25 \dots 85\text{ }^\circ\text{C}$   
input levels  $lo = 0 \dots 0.45\text{ V}$ ,  $hi = 2.4\text{ V} \dots V_{CC}$ , see Fig. 2 for reference levels

Item No.	Symbol	Parameter	Conditions	Fig.	Min. / Max.		Unit
					Min.	Max.	
I001	tset	Setup Time: SI stable before CLK lo $\rightarrow$ hi		3	50		ns
I002	thold	Hold Time: SI stable after CLK lo $\rightarrow$ hi		3	50		ns

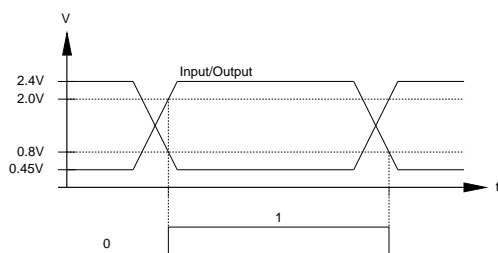


Figure 2: Reference levels

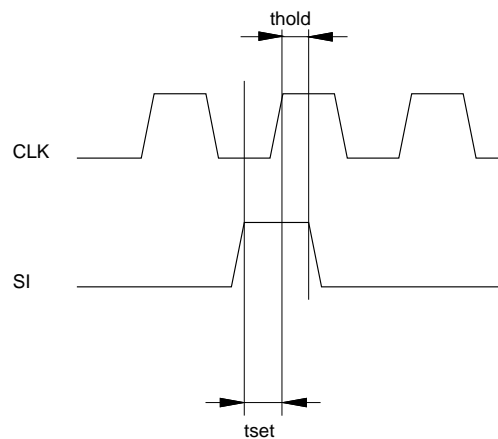


Figure 3: Timing diagram

**DESCRIPTION OF FUNCTIONS**

**Normal operation**

Following an internal power-on reset the integration and hold capacitors are discharged and the sample and hold circuit is set to sample mode. A high signal at SI and a rising edge at CLK triggers a readout cycle and with it a new integration cycle.

In this process the hold capacitors of pixels 1 to 255 are switched to hold mode immediately (SNH = 1),

with pixel 256 (SNH256 = 1) following suit one clock pulse later. This special procedure allows all pixels to be read out with just 256 clock pulses. The integration capacitors are discharged by a one clock long reset signal (NRCI = 0) which occurs between the 2<sup>nd</sup> and 3<sup>rd</sup> falling edge of the readout clock pulse (cf. Figure 4). After the 255 pixels have been read out these are again set to sample mode (SNH = 0), likewise for pixel 256 one clock pulse later (SNH256 = 0).

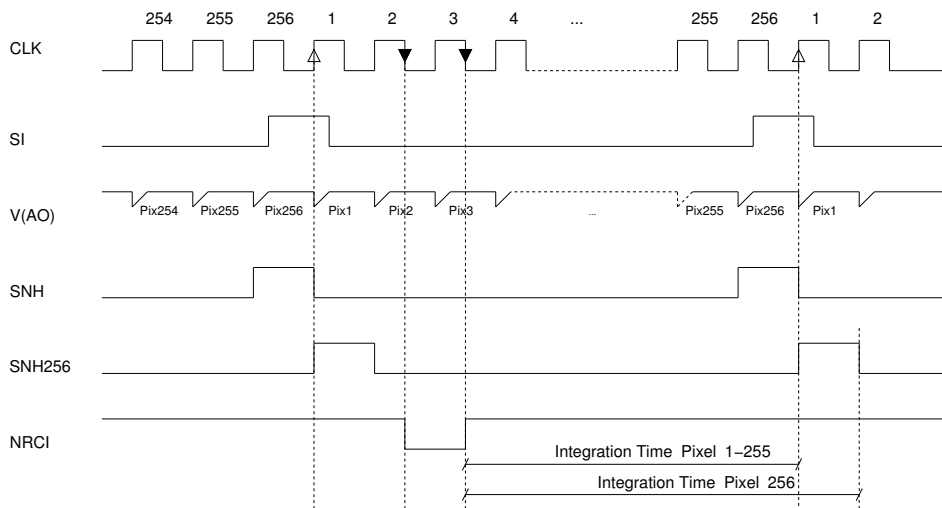


Figure 4: Readout cycle and integration sequence

If prior to the 256<sup>th</sup> clock pulse a high signal occurs at SI the present readout is halted and immediately reinitiated with pixel 1. In this instance the hold ca-

pacitors retain their old value i.e. hold mode prevails (SNH/SNH256 = 0).

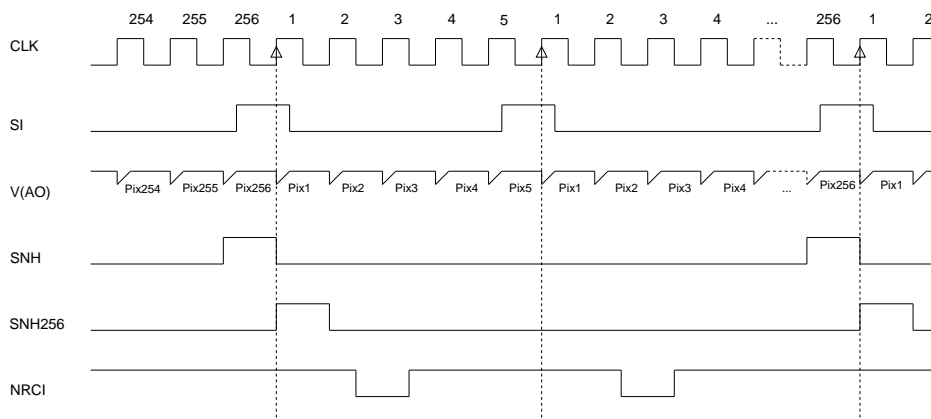


Figure 5: Restarting a readout cycle

With more than 256 clock pulses until the next SI signal, pixel 1 is output without entering hold mode; the

output voltage tracks the voltage of the pixel 1 integration capacitor.

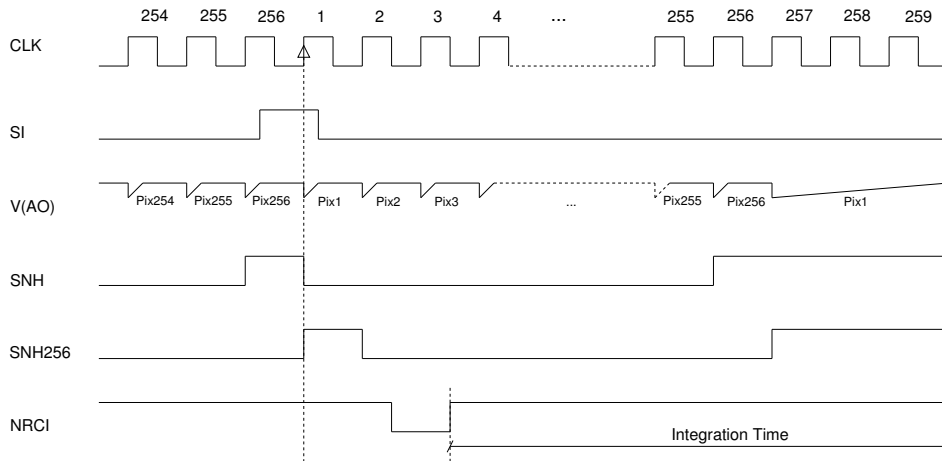


Figure 6: Clock pulse continued without giving a new integration start signal

**Operation with the shutter function**

Integration can be stopped at any time via pin DIS, i.e. the photodiodes are disconnected from their corresponding integration capacitor when DIS is high and

the current integration capacitor voltages are maintained. If this pin is open or switched to GND the pixel photocurrents are summed up by the integration capacitors until the next successive SI signal follows.

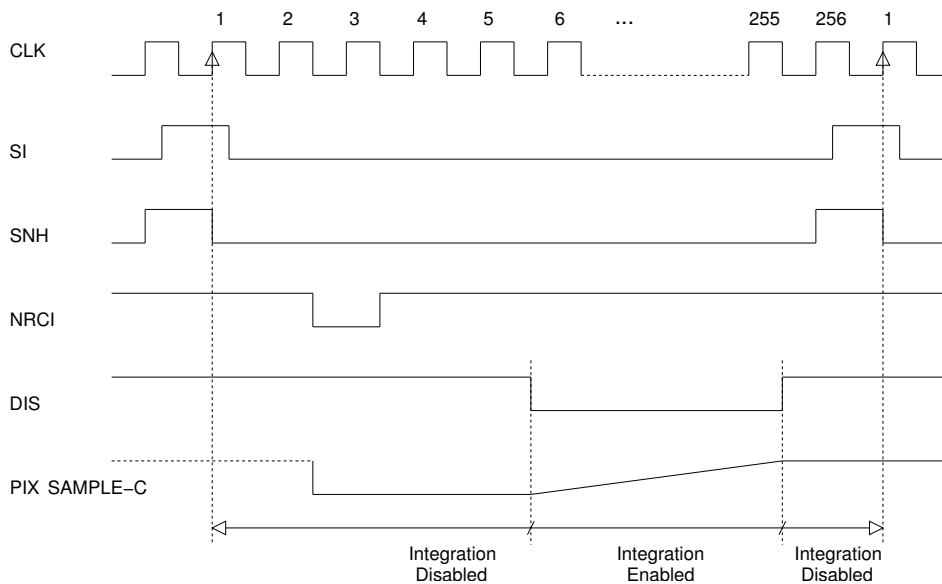


Figure 7: Defining the integration time via shutter input DIS

**External bias current setting**

In order to reduce the power consumption of the device an external reference current can be supplied to pin RSET which reduces the maximum readout frequency,

however. To this end a resistor must be connected from VCC to RSET. If this pin is not used, it should be connected to GND.

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## ORDERING INFORMATION

Type	Package	Order Designation
iC-LFL1402	OBGA™ LFL1C -	iC-LFL OBGA LFL1C iC-LFL Chip

For information about prices, terms of delivery, other packaging options etc. please contact:

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