iC-MSA SIN/COS SIGNAL CONDITIONER with AGC and 1Vpp DRIVER

preliminary

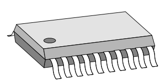
FEATURES

- PGA inputs for differential and single-ended sensor signals up to 20 kHz
- Selectable adaptation to voltage or current signals
- Flexible signal assignment due to input multiplexers
- Sine/Cosine signal conditioning for offset, amplitude and phase
- Separate index signal conditioning
- Short-circuit-proof and reverse polarity tolerant output drivers (1 Vpp to 100 Ω)
- Stabilized output signal levels due to automatic gain control
- Signal and system monitoring with configurable alarm output
- Supply voltage monitoring with integrated switches for reversed-polarity-safe systems
- Excessive temperature protection with sensor calibration
- I²C multi-master interface
- Supply from 4.3 to 5 V, operation within -40 °C to +115 °C
- Verifyable chip release code
- Pin compatible with iC-MSB

APPLICATIONS

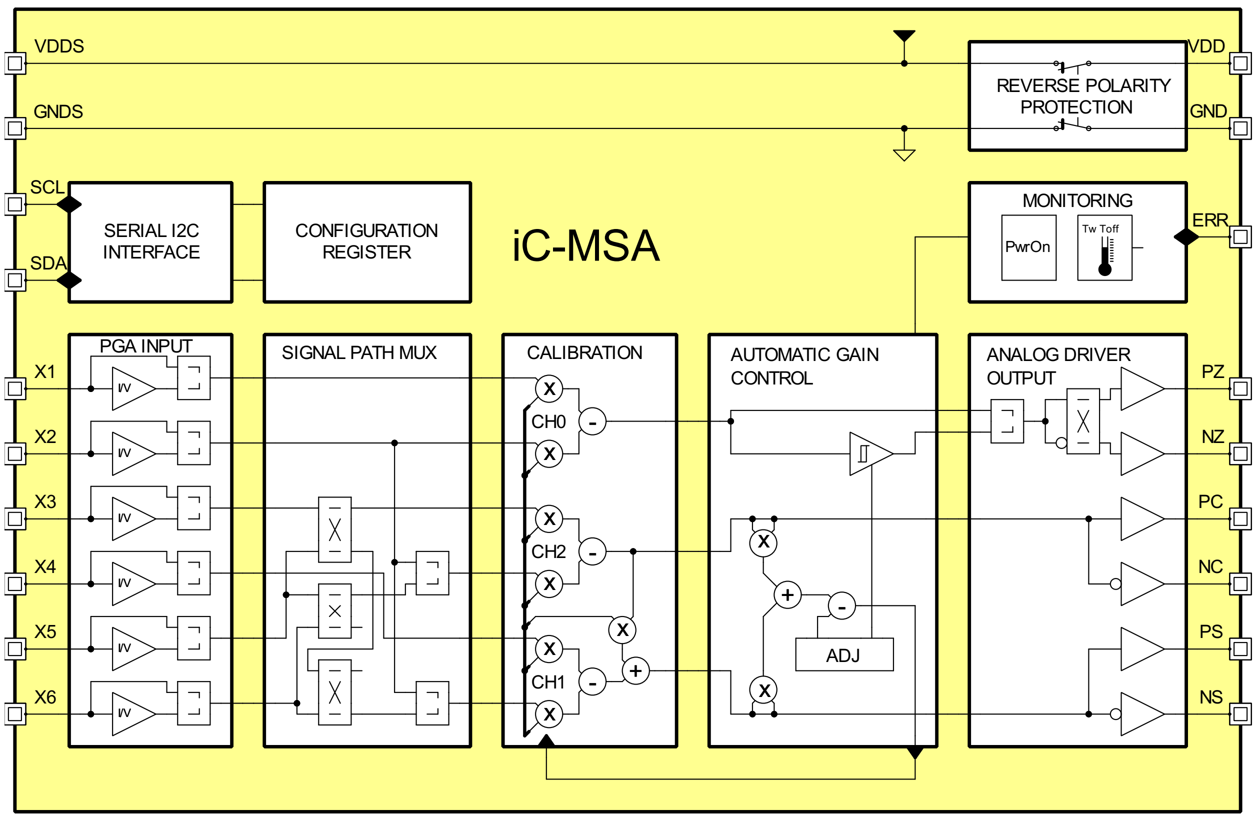
- Programmable sensor interface for optical and magnetic position sensors
- Linear gauges and incremental encoders
- Linear scales

PACKAGES



TSSOP20-TP

BLOCK DIAGRAM



DESCRIPTION

iC-MSA is a signal conditioner with line drivers for sine/cosine sensors which are used to determine positions in linear and angular encoders, for example.

Programmable instrumentation amplifiers with selectable gain levels permit differential or referenced input signals; at the same time the modes of operation differentiate between high and low input impedance. This adaptation of the iC to voltage or current signals enables MR sensor bridges or photosensors to be directly connected up to the device.

The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated accurately and also any phase error between the sine and cosine signals to be corrected. Separate zero signal conditioning settings can be made for the gain and offset; data is then output either as an analog or a differential square-wave signal (low/high level analogous to the sine/cosine amplitude).

For the stabilization of the output levels a signal is generated from the conditioned and calibrated input signals which controls the gain of all channels. Temperature and aging effects can be compensated for and the set signal amplitude is maintained with absolute accuracy. At the same time the control circuitry monitors both whether the sensor is functioning correctly and whether it is properly connected; signal loss due to wire breakage, short circuiting, dirt or aging, for example, is recognized when control thresholds are reached and indicated at alarm output ERR.

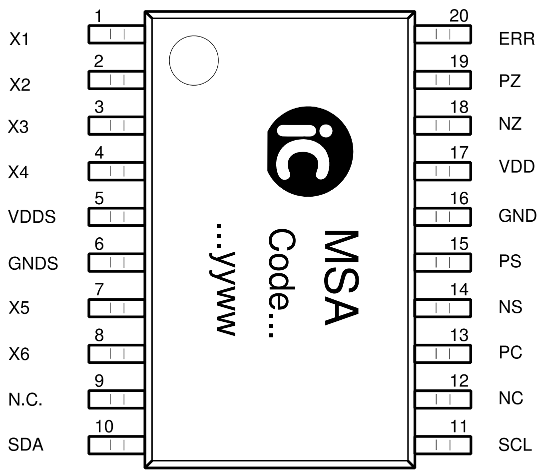
iC-MSA is protected against a reversed power supply voltage; the integrated voltage switch for loads of up to 20 mA extends this protection to cover the overall system. The analog output drivers are directly cable-compatible and tolerant to false wiring; if supply voltage is connected up to these pins, the device is not destroyed.

The device configuration and calibration parameters are CRC protected and stored in an external EEPROM; they are loaded automatically via the I2C interface once the supply voltage has been connected up.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION TSSOP20-TP



PIN FUNCTIONS

No.	Name	Function
1	X1	Signal Input 1 (Index +)
2	X2	Signal Input 2 (Index -)
3	X3	Signal Input 3
4	X4	Signal Input 4
5	VDDS[1)]	Switched Supply Output and Internal Analog Supply Voltage (reverse-polarity-proof, load 20 mA max.)
6	GNDS[1)]	Switched Ground (reverse-polarity-proof)
7	X5	Signal Input 5
8	X6	Signal Input 6
9	N.C.	Not Connected
10	SDA	Serial Configuration Interface, data line
11	SCL	Serial Configuration Interface, clock line
12	NC	Neg. Cosine Output
13	PC	Pos. Cosine Output
14	NS	Neg. Sine Output
15	PS	Pos. Sine Output
16	GND	Ground
17	VDD	+4.3 V to +5.5 V Supply Voltage
18	NZ	Neg. Index Output
19	PZ	Pos. Index Output
20	ERR	Error Signal (In/Out), Test Mode Trigger Input
	TP[2)]	Thermal Pad (TSSOP20-TP)

1) It is advicable to connect a bypass capacitor of at least 100 nF close to the chip's analog supply terminals.
2) To improve heat dissipation the *thermal pad* of the package (bottom side) should be joined to an extended copper area which must have GNDS potential.

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, GND, PC, NC, PS, NS, PZ, NZ		-6	6	V
G002	V()	Voltage at ERR		-6	8	V
G003	V()	Pin-To-Pin Voltage between VDD, GND, PC, NC, PS, NS, PZ, NZ, ERR			6	V
G004	V()	Voltage at X1...X6, SCL, SDA		-0.3	VDDS + 0.3	V
G005	I(VDD)	Current in VDD		-100	100	mA
G006	I()	Current in VDDS, GNDS		-50	50	mA
G007	I()	Current in X1...X6, SCL, SDA, ERR, PC, NC, PS, NS, PZ, NZ		-20	20	mA
G008	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G009	Ptot	Permissible Power Dissipation	TSSOP20-TP		400	mW
G010	Tj	Junction Temperature		-40	150	°C
G011	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

VDD = 4.3...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	TSSOP20-TP	-40		115	°C
T02	Rthja	Thermal Resistance Chip to Ambient	TSSOP20-TP surface mounted to PCB according to JEDEC 51		35		K/W

All voltages are referenced to Pin GNDS unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage	Load current I(VDDS) < -10 mA	4.3 4.5		5.5 5.5	V V
002	I(VDD)	Supply Current in VDD	Tj = 27 °C, no load		25	50	mA
003	I(VDDS)	Permissible Load Current VDDS		-20		0	mA
004	Vcz()hi	Clamp Voltage hi at all pins				11	V
005	Vc()hi	Clamp Voltage hi at inputs SCL, SDA	Vc()hi = V() − V(VDDS), I() = 1 mA	0.4		1.5	V
006	Vc()hi	Clamp Voltage hi at inputs X1...X6	Vc()hi = V() − V(VDDS), I() = 4 mA	0.3		1.2	V
007	Vc()lo	Clamp Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
008	Irev(VDD)	Reverse-Polarity Current VDD vs. GND	V(VDD) = −5.5 V...−4.3 V	-1		1	mA
Signal Conditioning, Inputs X3...X6							
101	Vin()sig	Permissible Input Voltage Range	RIN12(3:0) = 0x01 RIN12(3:0) = 0x09	0.75 0		VDDS − 1.5 VDDS	V V
102	Iin()sig	Permissible Input Current Range	RIN12(0) = 0, BIAS12 = 0 RIN12(0) = 0, BIAS12 = 1	-300 10		-10 300	µA µA
103	Iin()	Input Current	RIN12(3:0) = 0x01	-10		10	µA
104	Rin()	Input Resistance vs. VREFin	Tj = 27 °C; RIN12(3:0) = 0x09 RIN12(3:0) = 0x00 RIN12(3:0) = 0x02 RIN12(3:0) = 0x04 RIN12(3:0) = 0x06	 16 1.1 1.6 2.2 3.2	 20 1.6 2.3 3.2 4.6	 24 2.1 3.0 4.2 6.0	 kΩ kΩ kΩ kΩ kΩ
105	TCRin()	Temperature Coefficient Rin			0.15		%/K
106	VREFin12	Reference Voltage	RIN12(0) = 0, BIAS12 = 1 RIN12(0) = 0, BIAS12 = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
107	G12	Gain Factors	GC2 = 0x80; RIN12(3:0) = 0x01, GR12 and AGCGF1 = min. RIN12(3:0) = 0x01, GR12 and AGCGF1 = max. RIN12(3:0) = 0x09, GR12 and AGCGF1 = min. RIN12(3:0) = 0x09, GR12 and AGCGF1 = max.		 0.8 116 0.2 29		
108	ΔGdiff	Differential Gain Accuracy	calibration range 11 bit	-0.5		0.5	LSB
109	ΔGabs	Absolute Gain Accuracy	calibration range 11 bit, guaranteed monotony	-1		1	LSB
110	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(CHPx) - V(CHNx), RIN12(3) = 0 RIN12(3) = 1	 10 40		 500 2000	 mVpp mVpp
111	Vin()os	Input Offset Voltage	refered to side of input	0	20		µV
112	VOScal	Offset Calibration Range	referenced to the selected source (VOS12); ORx = 00 ORx = 01 ORx = 10 ORx = 11		 ±100 ±200 ±600 ±1200		 %V() %V() %V() %V()
113	ΔVOSdiff	Differential Linearity Error of Offset Correction	calibration range 11 bit	-0.5		0.5	LSB
114	ΔVOSint	Integral Linearity Error of Offset Correction	calibration range 11 bit	-1		1	LSB
115	PHIkorr	Phase Error Calibration Range	CH1 versus CH2		±10.4		°
116	ΔPHIdiff	Differential Linearity Error of Phase Calibration	calibration range 10 bit	-0.5		0.5	LSB
117	ΔPHIint	Integral Linearity Error of Phase Calibration	calibration range 10 bit	-1		1	LSB
119	fin()max	Permissible Input Frequency		20			kHz

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
120	fhc()	Input Amplifier Cut-off Frequency (-3dB)		100			kHz
Signal Conditioning, Inputs X1, X2							
201	Vin()sig	Permissible Input Voltage Range	RIN0(3:0) = 0x01 RIN0(3:0) = 0x09	0.75 0		VDDS – 1.5 VDDS	V V
202	Iin()sig	Permissible Input Current Range	RIN0(0) = 0, BIAS0 = 0 RIN0(0) = 0, BIAS0 = 1	-300 10		-10 300	µA µA
203	Iin()	Input Current	RIN0(3:0) = 0x01	-10		10	µA
204	Vout(X2)	Output Voltage at X2	BIASEX = 10, I(X2) = 0, referenced to VREFin12	95	100	105	%
205	Vin(X2)	Permissible Input Voltage at	BIASEX = 11	0.5		VDDS – 2	V
206	Rin(X2)	Input Resistance at X2	BIASEX = 11, RIN0(3:0) = 0x01, RIN12(3:0) = 0x01	20	28	35	kΩ
207	Rin()	Input Resistance vs. VREFin	Tj = 27 °C; RIN0(3:0) = 0x09 RIN0(3:0) = 0x00 RIN0(3:0) = 0x02 RIN0(3:0) = 0x04 RIN0(3:0) = 0x06	 16 1.1 1.6 2.2 3.2	 20 1.6 2.3 3.2 4.6	 24 2.1 3.0 4.2 6.0	 kΩ kΩ kΩ kΩ kΩ
208	TCRin()	Temperature Coefficient Rin			0.15		%/K
209	VREFin0	Reference Voltage	RIN0(0) = 0, BIAS0 = 1 RIN0(0) = 0, BIAS0 = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
210	G0	Gain Factors	GC0 = 0x80; RIN0(3:0) = 0x01, GR0 and AGCGF1 = min. RIN0(3:0) = 0x01, GR0 and AGCGF1 = max. RIN0(3:0) = 0x09, GR0 and AGCGF1 = min. RIN0(3:0) = 0x09, GR0 and AGCGF1 = max.		 0.8 116 0.2 29		
211	ΔGdiff	Differential Gain Accuracy	calibration range 5 bit	-0.5		0.5	LSB
212	ΔGabs	Absolute Gain Accuracy	calibration range 5 bit, guaranteed monotony	-1		1	LSB
213	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(CHP0) - V(CHN0), RIN0(3:0) = 0x01 RIN0(3:0) = 0x09	 10 40		 500 2000	 mVpp mVpp
214	Vin()os	Input Offset Voltage	referred to side of input	0	75		µV
215	VOScal	Offset Calibration Range	referenced to the selected source (REFVOS); OR0 = 00 OR0 = 01 OR0 = 10 OR0 = 11		 ±100 ±200 ±600 ±1200		 %V() %V() %V() %V()
216	ΔVOSdiff	Differential Linearity Error of Offset Correction	calibration range 6 bit	-0.5		0.5	LSB
217	ΔVOSint	Integral Linearity Error of Offset Correction	calibration range 6 bit	-1		1	LSB
Signal Filter							
301	fg	Cut-off Frequency				4000	kHz
302	phi	Phase Shift	fin 500 kHz for sine/cosine			10	°
Index Pulse Comparator Output PZ, NZ							
401	Vpk()	Output Amplitude With Automatic Gain Control	EAZ = 1, AGCOFF = 0, ADJ = 0x32	225	250	275	mV
402	SR()	Output Slew Rate	EAZ = 1		1		V/µs
Line Driver Outputs PS, NS, PC, NC, PZ, NZ							
501	Vpk()max	Permissible Output Amplitude	VDD = 4.5 V, DC level = VDD / 2, RL = 50 Ω vs. VDD / 2			300	mV
502	Vpk()	Output Amplitude With Automatic Gain Control	AGCOFF = 0, ADJ (5:0) = 0x32	225	250	275	mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
503	fg	Cut-off Frequency	CL = 250 pF	500			kHz
504	Vos	Offset Voltage			±200		µV
505	Isc()	Short-circuit Current	pin shorten to VDD or GND	10	30	50	mA
506	Ilk()	Tristate Leakage Current	tristate or reversed supply	-1		1	µA
Automatic Signal Gain Controller							
601	tset()	Automatic Gain Settling Time	square control active, AGCGF1: 0x40 → 0x80		2		ms
602	Gt()min	Control Range Monitoring 1: lower limit	CH1 gain/GR12, AGCGF1 = 0x10		1.2		
603	Gt()max	Control Range Monitoring 2: upper limit	CH1 gain/GR12, AGCGF1 = 0xF0		16.6		
604	Vt()min	Signal Level Monitoring 1: lower limit	referenced to Vscq()		40		%Vpp
605	Vt()max	Signal Level Monitoring 2: upper limit	referenced to Vscq()		130		%Vpp
Test Current ERR							
701	I(ERR)	Permissible Test Current	test mode activated	0		1	mA
Bias Current Source and Reference Voltages							
801	IBN()	Bias Current Source	MODE(3:0) = 0x01, I(NC) vs. VDDS	180	200	220	µA
802	VPAH	Reference Voltage VPAH	referenced to GND	45	50	55	%VDD
803	V05	Reference Voltage V05		450	500	550	mV
804	V025	Reference Voltage V025			50		%V05
Power-Down-Reset							
901	VDDon	Turn-on Threshold (power-on release)	increasing voltage at VDD vs. GND	3.7	4	4.3	V
902	VDDoff	Turn-off Threshold (power-down reset)	decreasing voltage at VDD vs. GND	3.2	3.5	3.8	V
903	VDDhys	Threshold Hysteresis	VDDhys = VDDon − VDDoff	0.3			V
Clock Oscillator							
A01	fclk()	Internal Clock Frequency	MODE(3:0) = 0x0A, fclk(NS)	120	160	200	kHz
Error Signal Input/Output, Pin ERR							
B01	Vs()lo	Saturation Voltage lo	vs. GND, I() = 4 mA			0.4	V
B02	Isc()	Short-circuit Current lo	vs. GND; V(ERR) ≤ VDD V(ERR) > VTMon	4 2			mA mA
B03	Vt()hi	Input Threshold Voltage hi	vs. GND			2	V
B04	Vt()lo	Input Threshold Voltage lo	vs. GND	0.8			V
B05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	300	500		mV
B06	Ipu()	Input Pull-up Current	V() = 0...VDD − 1 V, EPU = 1	-400	-300	-200	µA
B07	Rpu()	Input Pull-Up Resistor	EPU = 0		500		kΩ
B08	Vpu()	Pull-up Voltage	Vpu() = VDD - V(), I() = -5 µA, EPU = 1			0.4	V
B09	VTMon	Test Mode Activation Threshold	increasing voltage at ERR			VDD + 1.5	V
B10	VTMoff	Test Mode Disabling Threshold	decreasing voltage at ERR	VDD + 0.5			V
B11	VTMhys	Test Mode Hysteresis	VTMhys = VTMon − VTMoff	0.15	0.3		V
B12	Ilk()	Leakage Current	tristate or reversed supply voltage	-1	-10	-50	µA
Supply Switch and Reverse Polarity Protection VDDS, GNDS							
C01	Vs()	Saturation Voltage VDDS vs. VDD	Vs(VDDS) = VDD − V(VDDS) I(VDDS) = -10 mA...0 mA I(VDDS) = -20 mA...-10 mA			 150 250	 mV mV
C02	Vs()	Saturation Voltage GNDS vs. GND	Vs(GNDS) = V(GNDS) − GND I(GNDS) = 0 mA...10 mA I(GNDS) = 10 mA...20 mA			 150 250	 mV mV
C03	C()	Backup Capacitor Analog Supply VDDS vs. GNDS		100			nF

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Serial Configuration Interface SCL, SDA							
D01	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
D02	Isc()	Short-circuit Current lo		4		80	mA
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt()lo	Input Threshold Voltage lo		0.8			V
D05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	300	500		mV
D06	Ipu()	Input Pull-up Current	V() = 0...VDDS − 1 V	-600	-300	-60	µA
D07	Vpu()	Input Pull-up Voltage	Vpu() = VDDS − V(), I() = -5 µA			0.4	V
D08	fclk(SCL)	Clock Frequency at SCL	ENFAST = 0 ENFAST = 1	60 240	80 320	100 400	kHz kHz
D09	tbusy()cfg	Duration of Startup Configuration	IBN not calibated, EEPROM access without read failure, time to outputs operational; ENFAST = 0 ENFAST = 1		 40 25	 55 35	 ms ms
D10	tbusy()err	End Of I2C Communication; Time Until I2C Slave Is Enabled	IBN not calibrated; V(SDA) = 0 V V(SCL) = 0 V or arbitration lost no EEPROM CRC ERROR		 4 indef. 45 95	 12 135 285	 ms ms ms ms
D11	td()	Start Of Master Activity On I2C Protocol Error	SCL without clock signal: V(SCL) = constant; IBN not calibrated IBN calibrated to 200 µA	 25 64	 80 80	 240 120	 µs µs
D12	td()i2c	Delay for I2C-Slave-Mode Enable	no EEPROM, V(SDA) = 0 V		4	6.2	ms
Temperature Monitoring							
E01	VTs	Temperature Sensor Voltage	VTs() = VDDS − V(PS), Tj = 27 °C, Calibration Mode 3, no load	600	650	700	mV
E02	TCs	Temp. Co. of Temperature Sensor Voltage			-1.8		mV/K
E03	VTth	Temperature Warning Activation Threshold	VTth() = VDDS − V(NS), Tj = 27 °C, Calibration Mode 3, no load; CFGTA(3:0) = 0x00 CFGTA(3:0) = 0x0F	 260 470	 310 550	 360 630	 mV mV
E04	TCth	Temp. Co. Temperature Warning Activation Threshold			0.06		%/K
E05	Thys	Temperature Warning Hysteresis		4	12	20	°C
E06	ΔT	Relative Shutdown Temperature	ΔT = Toff − Twarn	4	12	20	°C

PROGRAMMING

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Interface								
0x40	ENFAST	DEVID(6:0)						
Calibration								
0x41	CFGIBN(3:0)				CFGTA(3:0)			
Operation Modes								
0x42	NTRI	1	0	–	MODE(3:0)			
Input Configuration and Signal Path Multiplexer								
0x43	EAZ	0	0	0	INVZ	INMODE	MUXIN(1:0)	
0x44	0	0	0	1	0	0	0	0
Signal Level Controller								
0x45	AGCOFF	0	ADJ(5:0)					
Signal Conditioning CH1, CH2								
0x46	0	0	0	0	0	GR12(2:0)		
0x47	0	0	0	0	1	0	0	0
0x48	OR1(0)	0	1	0	0	0	0	0
0x49	OF1(6:0)							OR1(1)
0x4A	OF2(1:0)		OR2(1:0)		OF1(10:7)			
0x4B	OF2(9:2)							
0x4C	PH12(6:0)							OF2(10)
0x4D	BIASEX(1:0)		BYP	1	1	PH12(9:7)		
0x4E	ENF	BIAS12	VOS12(1:0)		RIN12(3:0)			
0x4F	GC2(7:0)							
Signal Conditioning CH0								
0x50	GC0(7:0)							
0x51	-					GR0(2:0)		
0x52	OF0(5:0)						OR0(1:0)	
0x53	0	BIAS0	VOS0(1:0)		RIN0(3:0)			
Error Monitoring and Alarm Output								
0x54	–	EMASKA(6:0)						
0x55	TMODE(1:0)		EMTD(2:0)			EPH	–	–
0x56	–	EMASKO(6:0)						
0x57	EMASKE(3:0)				ENSL	EPU	–	–
0x58	–	PDMODE	–	–	–	EMASKE(6:4)		
0x59	EEPROM: not defined / RAM: AGCGF1(10:3) (read-only)							
0x5A	not defined							
OEM Data								
0x5B.. 0x5E	OEM Data							
Check Sum / Chip Release								
0x5F	EEPROM: CHKSUM(7:0) / ROM: CHPREL(7:0)							

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Error Register								
0x60	–	ERR1(6:0)						
0x61	ERR2(5:0)						–	–
0x62	ERR3(3:0)				–	–	–	ERR2(6)
0x63	–	–	–	–	–	ERR3(6:4)		
Notes	Register entries specified 0 or 1 mean a mandatory programming.							

Table 4: Register layout

SERIAL CONFIGURATION INTERFACE (EEPROM)

The serial configuration interface consists of the two pins SCL and SDA and enables read and write access to an EEPROM with I²C interface. The readout speed can be adjusted using register bit ENFAST.

ENFAST	Adr 0x40, bit 7
Code	Function
0	Regular clock rate, f(SCL) approx. 80 kHz
1	High clock rate, f(SCL) approx. 320 kHz
Notes	For in-circuit programming bus lines SCL and SDA require pull-up resistors. For line capacitances to 170 pF, adequate values are: 4.7 kΩ with clock frequency 80 kHz 2 kΩ with clock frequency 320 kHz The pull-up resistors may not be less than 1.5 kΩ. To separate the signals a ground line between SCL and SDA is recommended. iC-MSA requires a supply voltage during EEPROM programming (5 V to VDD).

Table 5: Config. Interface Clock Frequency

Once the supply has been switched on (power down reset) the iC-MSA outputs are high impedance (tristate) until a valid configuration is read out from the EEPROM using device ID 0x50.

Bit errors in the 0x40 to 0x5E memory section are pinpointed by the CRC deposited in register CHKSUM(7:0) (address 0x5F; the CRC polynomial used is "1 0001 1101").

Should no valid configuration data being available (incorrect CRC value or EEPROM missing), the readin process is repeated; the system aborts following a fourth faulty attempt and iC-MSA switches to I²C slave mode.

For devices loading valid configuration data from the EEPROM, the register bit ENSL decides for enabling the I²C slave function.

ENSL	Adr 0x17, bit 3
Code	Function
0	Normal operation
1	I²C Slave Mode Enable (Device ID 0x57)

Table 6: Config. Interface Mode

The device ID for the EEPROM can be entered in register DEVID(6:0) (address 0x40), from which iC-MSA will take its configuration after exiting test mode (see page 17). The DEVID(6:0) stored therein is then accepted.

Example of CRC Calculation Routine

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<31; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

EEPROM Selection

The following minimal requirements must be fulfilled:

- Operation from 3.3 to 5 V, I²C interface
- Minimal 1024 bit, 128x8 (address range used is 0x40 to 0x7F)
- Support of *Page Write* with *Pages* of at least 4 bytes. Otherwise error events can not be saved to the EEPROM (EMASKE(9:0) = 0x000).
- Device ID 0x50 "101 0000", no occupation of 0x57 (A2...A0 = 0). Otherwise iC-MSA is not accessible in I²C slave mode via 0x57 (ENSL = 0).

Recommended devices: Atmel AT24C01B, ST M24C01W, ST M24C02 (2K), ROHM BR24L01A-W, BR24L02-W

I²C Slave Mode (ENSL = 1)

In this mode iC-MSA behaves like an I²C slave with the device ID 0x57 and the configuration interface permits write and read accesses to iC-MSA's internal registers.

For chip release verification purposes an identification value is stored under ROM address 0x5F; a write access to this address is not permitted.

CHPREL	Adr 0x5F, bit 7:0 (ROM)
Code	Chip Release
0x10	iC-MSA

Table 7: Chip Release

NTRI	Adr 0x42, bit 7
Code	Function
0	Output drivers disabled
1	Setting the operating mode, output drivers active
Notes	NTRI is evaluated only during I²C slave mode.

Table 8: Tristate Function And Op. Mode Change

Register	Read access in I²C slave mode (ENSL = 1)
Address	Content
0x00-0x03	Current error memory
0x04-0x3F	Not available
0x40-0x58	Configuration: register addresses 0x40-0x58
0x59	AGCGF1(10:3)
0x5A	Not available
0x5B-0x5E	OEM data: register addresses 0x5B-0x5E
0x5F	Chip release (ROM)
0x60-0x63	Configuration: register addresses 0x60-0x63
0x64-0x77	Not available
0x78	Configuration: register address 0x58
0x79-0x7A	Not available
0x7B-0x7E	OEM data: register addresses 0x5B-0x5E
0x7F	Chip release (ROM)

Table 9: RAM Read Access

Register	Write access in I²C slave mode (ENSL = 1)
Address	Access and conditions
0x40	Changes possible, no restrictions
0x41	Changes possible (wrong entries for CFGIBN can limit functions)
0x42	Bit 7 = 0 (NTRI): changes to bits (6:0) permitted A change of operating mode follows only on writing Bit 7 = 1 (NTRI); when doing so changes to bits (6:0) are not permitted.
0x43-0x56	Changes possible, no restrictions
0x57	Bit 3 = 1 (ENSL): changes to bits (7:4) and (2:0) permitted
0x58	Changes possible, no restrictions
0x59-0x5A	Not available
0x5B-0x5E	Changes possible, no restrictions
others	No changes permitted

Table 10: RAM Write Access

BIAS SOURCE AND TEMPERATURE SENSOR CALIBRATION

Bias Source Calibration

The calibration of the bias current source in operation mode *Calibration 1* (Tab. 13) is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. SCL clock frequency). For setup purposes the IBN value is measured using a 10 kΩ resistor by pin VDDS connected to pin NC. The setpoint is 200 µA which is equivalent to a measurement voltage of 2 V.

CFGIBN	Adr 0x41, bit 7:4		
Code k	$IBN \sim \frac{31}{39-k}$	Code k	$IBN \sim \frac{31}{39-k}$
0x0	79 %	0x8	100 %
0x1	81 %	0x9	103 %
0x2	84 %	0xA	107 %
0x3	86 %	0xB	111 %
0x4	88 %	0xC	115 %
0x5	91 %	0xD	119 %
0x6	94 %	0xE	124 %
0x7	97 %	0xF	129 %

Table 11: Bias Current Source Calibration

Temperature Sensor

The temperature monitor is calibrated in operating mode *Calibration Mode 3*.

To set the required warning temperature T_2 the temperature sensor voltage VTs at which the warning is generated is first determined. To this end a voltage ramp from VDDS towards GNDS is applied to pin PS until pin ERR triggers an error message (for EMASKA = 0x20 and EMTD = 0x00).

Example: $VTs(T_1)$ is ca. 650 mV, measured from VDDS versus PS, with T_1 = 25 °C;

The necessary activation threshold voltage $VTth(T_1)$ is then calculated. The required warning temperature T_2, temperature coefficients TCs and TCth (see Electrical Characteristics, Section E) and measurement value $VTs(T_1)$ are entered into this calculation:

$$VTth(T_1) = \frac{VTs(T_1) + TCs \cdot (T_2 - T_1)}{1 + TCth \cdot (T_2 - T_1)}$$

Example: For $T_2 = T_1 + 100\,K$, $VTth(T_1)$ must be programmed to 443 mV.

Activation threshold voltage $VTth(T_1)$ is provided for a high impedance measurement (10 MΩ) at output pin NS (measurement versus VDDS) and must be set by programming CFGTA(3:0) to the calculated value.

Example: Altering $VTth(T_1)$ from 310 mV (measured with CFGTA(3:0)= 0x0) to 443 mV is equivalent to 143 %, the closest value for CFGTA is 0x9;

CFGTA	Adr 0x41, bit 3:0		
Code k	$VTth \sim \frac{65+3k}{65}$	Code k	$VTth \sim \frac{65+3k}{65}$
0x0	100 %	0x8	140 %
0x1	105 %	0x9	145 %
0x2	110 %	0xA	150 %
0x3	115 %	0xB	155 %
0x4	120 %	0xC	160 %
0x5	125 %	0xD	165 %
0x6	130 %	0xE	170 %
0x7	135 %	0xF	175 %
Notes	With CFGTA = 0xF Toff is 80 °C typ., with CFGTA = 0x0 Toff is 155 °C typ.		

Table 12: Calibration of Temperature Monitoring

OPERATING MODES

In order to calibrate iC-MSA, compensate for the input signals and test iC-MSA the mode of operation must be changed. The output function changes according to the various operating modes; the line drivers and protection against reverse polarity facility are only active in normal mode.

MODE(3:0)		Addr. 0x42; bit 3:0						
BYP		Addr. 0x4D; bit 5						
Code	Operating Mode	Pin PS	Pin NS	Pin PC	Pin NC	Pin PZ	Pin NZ	Pin ERR
0x00	Normal operation	PS	NS	PC	NC	PZ	NZ	ERR
0x01	Calibration 1	TANA0(2)	VREFI0	VREFI12	IBN	PZI	NZI	ERR
0x02	Calibration 2	PCH1	NCH1	PCH2	NCH2	—	—	—
0x03	iC-Haus Test 1	VPAH	VPD	—	CGUCK	IPF	V05	IERR
0x04	iC-Haus Test 2	PS_out	NS_out	PC_out	NC_out	PZ_out	NZ_out	IERR
0x05	iC-Haus Test 3	PS_out	NS_out	PC_out	NC_out	PZ_out	NZ_out	ERR
0x06	iC-Haus Test 4, BYP = 0 iC-Haus Test 4, BYP = 1	TANA12(0) X4	TANA12(1) X6	TANA12(2) X3	TANA12(3) X5	TANA12(4) X1	TANA12(5) X2	IERR
0x07	Calibration 3	VTs	VTth	—	—	—	—	ERR
0x08	Saturation low	SCL, SDA and ERR low						
0x09	—	—	—	—	—	—	—	—
0x0A	iC-Haus Test 5	—	—	TP	CLK6	—	—	—
0x0B	—	—	—	—	—	—	—	—
0x0C	—	—	—	—	—	—	—	—
0x0D	—	—	—	—	—	—	—	—
0x0E	IDDQ-Test	All PU/PD resistors, oscillator and supply voltage deactivated						
0x0F	—	—	—	—	—	—	—	—

Table 13: Selection of Operating Modes

Calibration Op. Modes

In *Calibration Mode 1* the user can measure the BIAS current (IBN), input amplifier reference potential VREFI and the analog signals from channel 0 following signal conditioning (PCH0 and NCH0).
In *Calibration Mode 2* the conditioned signals from channels 1 and 2 are output (PCH1, NCH1, PCH2 and NCH2).
In *Calibration Mode 3* the internal temperature monitoring signals are provided.

Special Device Test Functions

IDDQ-Test, *Saturation Low*, *Saturation High*, and *Test 1 to 5* are test modes for iC-Haus device tests. With an activated bypass (BYP = 1), mode *iC-Haus Test 4* permits the direct feedthrough of X1 - X6 input signals to the output pins; in this instance the output impedance is high-ohmic. Furthermore, if the input voltage divider is selected (by RINx = 1- -1), it reduces the signal amplitudes to approx. 7/8.

Signal Filter

iC-MSA has a noise limiting signal filter to filter the conditioned analog signals. This can be activated using ENF.

ENF	Adr 0x4E, bit 7
Code	Function
0	Noise limiter deactivated
1	Noise limiter activated

Table 14: Signal Filtering

TEST MODE

iC-MSA switches to test mode if a voltage larger than VTMon is applied to pin ERR (precondition: TMODE(0) = 1). In response iC-MSA transmits its configuration settings as current-modulated data using I/O pin ERR after re-reading the EEPROM. If the voltage at pin ERR falls below VTMoff test mode is terminated and data transmission aborted.

The clock rate for the data output is determined by ENFAST. Two clock rates can be selected: 780 ns for ENFAST = 1 or 3.125 µs for ENFAST = 0 (see Elec. Char. D08 for clock frequency and tolerances).

Data is output in Manchester code via two clock pulses per bit. To this end the lowside current source switches between a Z state (OFF = 0 mA) and an L state (ON = 2 mA).

The bit information lies in the direction of the current source switch:
Zero bit: change of state Z → L (OFF to ON)
One bit: Change of state L → Z (ON to OFF)

Transmission consists of a start bit (a one bit), 8 data bits and a pause interval in Z state (the timing is identical with an EEPROM access via the I^2C interface).

Example: byte value = 1000 1010
Transmission including the start bit: 1 1000 1010
In Manchester code: LZ LZZL ZLZL LZZL LZZL

Decoding of the data stream:

ZZZZZZ LZ LZ ZL ZL ZL LZ ZL LZ ZL ZZZZZZ
Pause 1 1 0 0 0 1 0 1 0 Pause

If test mode is quit with TMODE = 0x00, iC-MSA continues operation without any interruption.
If test mode is quit with TMODE > 0x00, then iC-MSA again reads out its configuration from the EEPROM accessible at the device ID filed to DEVID(6:0) of address 0x40.
In TMODE = 0x03 the EEPROM is read completely; in all other cases only the address range 0x40 to 0x61 is read to keep the configuration time for device testing short.

TMODE	Addr 0x55, bit 7:6	
Code	Function during test mode	Function following test mode
00	Normal operation	Normal operation
01	Transmission of EEPROM data, address range 0x5B-0x7F and 0x00-0x3F	Repeated read out of EEPROM
10	Normal operation	Repeated read out of EEPROM
11	Transmission of EEPROM data, address range 0x40-0x7F and 0x00-0x3F	Repeated read out of EEPROM

Table 15: Test Mode Functions

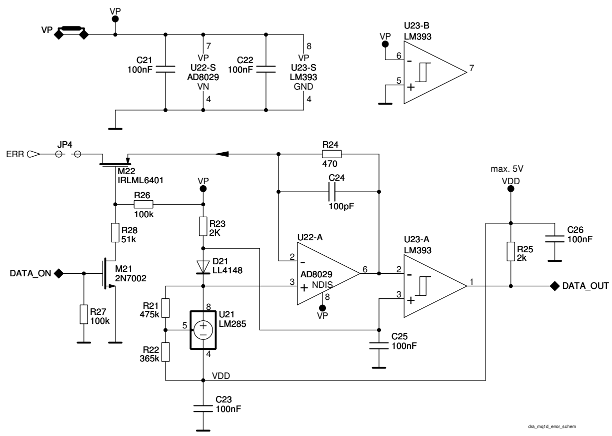


Figure 1: Example circuit for the decoding and conversion of the current-modulated signals to logic levels.

INPUT CONFIGURATIONS

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Referenced input signals can be processed as an option; in this mode input X2 acts as a reference. Both current and voltage signals can be processed as input signals, selected using RIN12(0) and RIN0(0).

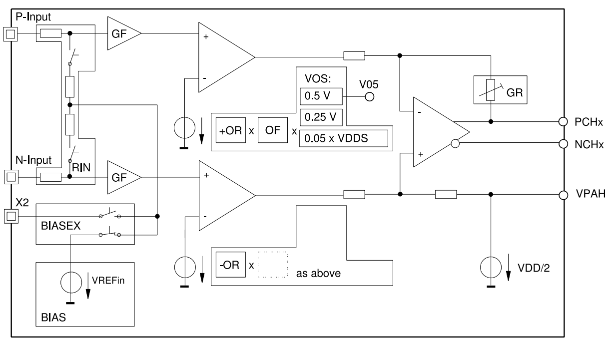


Figure 2: Signal conditioning input circuit.

Current Signals

In I Mode an input resistor Rin() becomes active at each input pin, converting the current signal into a voltage signal. Input resistance Rin() consists of a pad wiring resistor and resistor Rui() which is linked to the adjustable bias voltage source VREFin(). The following table shows the possible selections, with Rin() giving the typical resulting input resistance (see Electrical Characteristics for tolerances).

NB. The input circuit is not suitable for back-to-back photodiodes.

Voltage Signals

In V Mode an optional voltage divider can be selected which reduces unacceptably large input amplitudes to ca. 25%. The circuitry is equivalent to the resistor chain in I Mode; the pad wiring resistor is considerably larger here, however.

For sensors whose offset calibration is to be proportional to an external DC voltage source the reference source can be selected using BIASEX; for all other sensors BIASEX should be set to '00'.

INMODE	Addr 0x43, bit 2
Code	Function
0	Differential input signals
1	Single-ended input signals *
Note	* Input X2 is reference for all inputs.

Table 16: Input Signal Mode

RIN12	Addr 0x4E, bit 3:0		
RIN0	Addr 0x53, bit 3:0		
Code	Nominal Rin()	Intern Rui()	I/V Mode
–000	1.7 kΩ	1.6 kΩ	current input
–010	2.5 kΩ	2.3 kΩ	current input
–100	3.5 kΩ	3.2 kΩ	current input
–110	4.9 kΩ	4.6 kΩ	current input
1—1	20 kΩ	5 kΩ	voltage input 4:1*
0—1	high impedance	1 MΩ	voltage input 1:1
Notes	For single-ended signals identical settings of RIN0 and RIN12 are required. *) VREFin is the voltage divider's footpoint; input currents may be positive or negative (Vin > VREFin, or Vin < VREFin).		

Table 17: I/V Mode and Input Resistance

BIAS12	Addr 0x4E, bit 6
BIAS0	Addr 0x53, bit 6
Code	Function
0	VREFin = 2.5 V for low-side current sinks (e.g. photodiodes with common anode at GNDS)
1	VREFin = 1.5 V for high-side currrent-sources (e.g. photodiodes with common cathode at VDDS) for voltage sources versus ground (e.g. iC-SM2, Wheatstone sensor bridges) for voltage sources with low-side reference (e.g. iC-LSHB, when using BIASEX = 11)

Table 18: Reference Voltage

BIASEX	Addr 0x4D, bit 7:6	
Code	VREFin	Pin function of X2
00	internal	Input Index- (negative zero signal)
10	internal	Output of VREFin12*
11	external	Input for external reference**: V(X2) replaces VREFin
Notes	*) Do not load, buffering recommended **) See Elec. Char. Nos. 205 and 206	

Table 19: Input Reference Selection

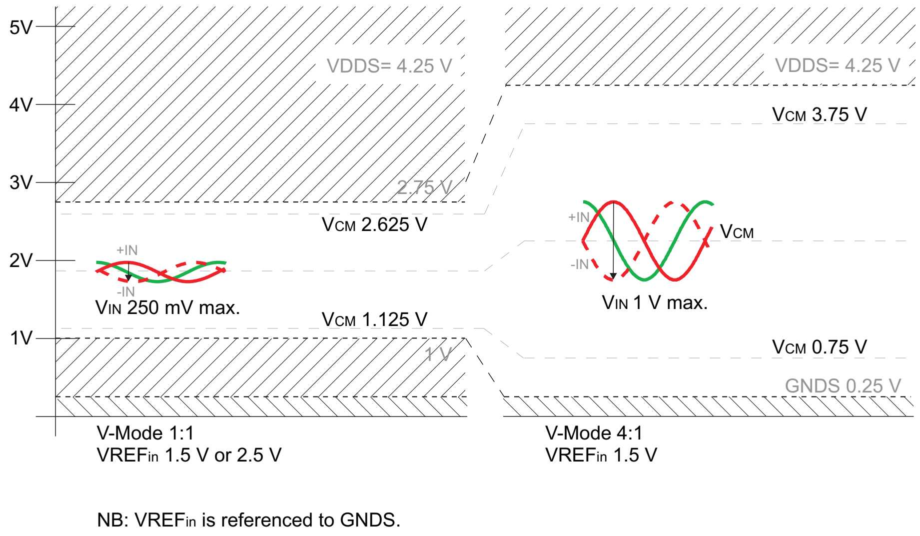


Figure 3: Permissible common mode range and maximum input signal for lowest gain (GR12 = 0x0, GF1, GF2 = 0x00); left side: voltage input 1:1, right side: voltage input 4:1.

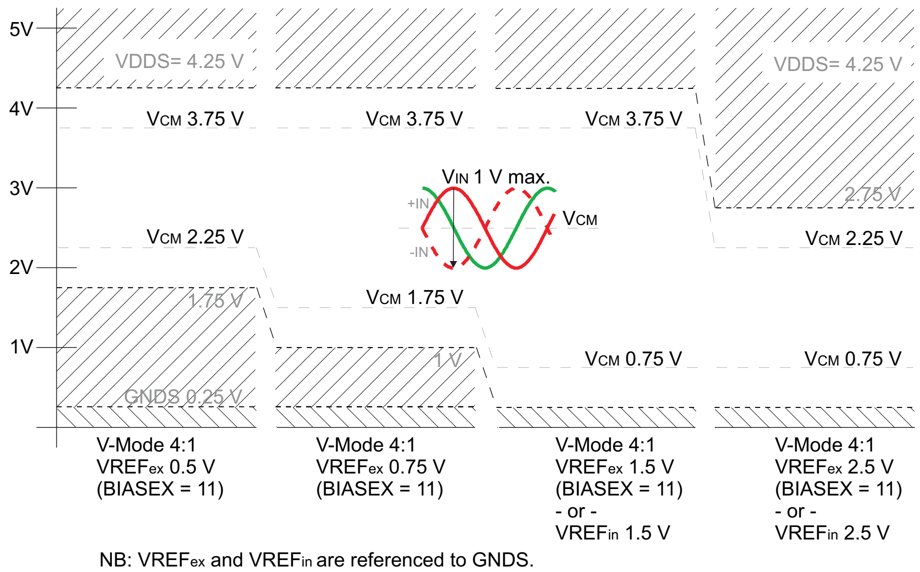


Figure 4: Permissible common mode range for voltage input 4:1 in dependancy to the reference voltage.

SIGNAL PATH MULTIPLEXING

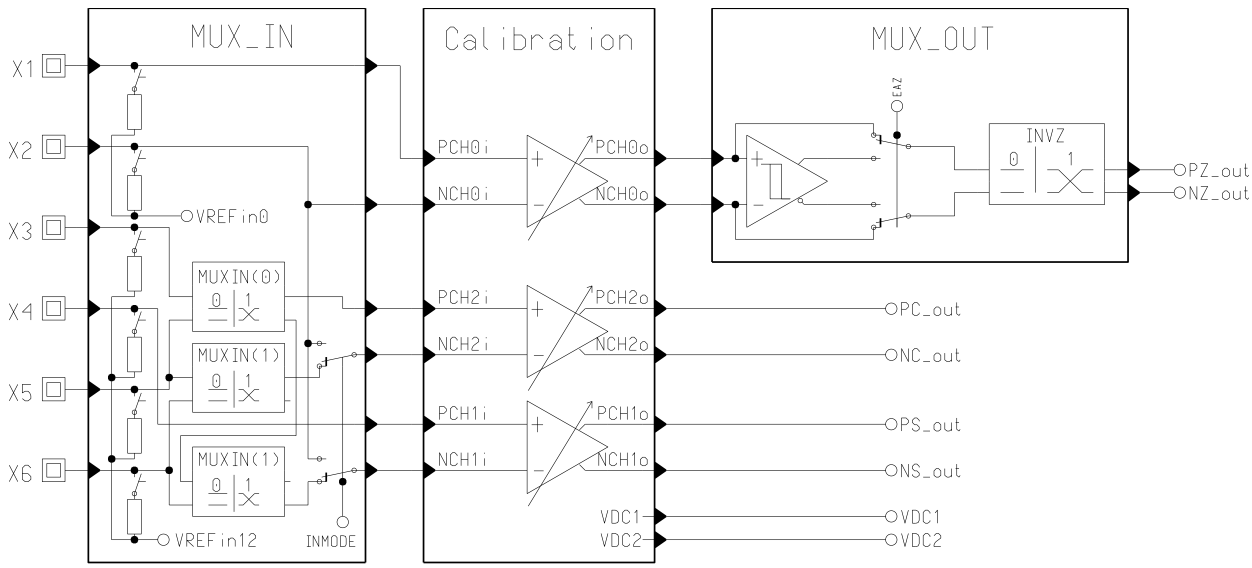


Figure 5: Multiplexer Schematics

The signals for index channel CH0 are connected up to pins X1 and X2. Pins X3 to X6 are allocated to internal channels CH1 and CH2 via MUXIN. INMODE can be activated for referenced input signals; this then selects X2 as the reference input.

MUXIN	Addr 0x43, bit 1:0			
Code	PCH1i	NCH1i	PCH2i	NCH2i
00	X4	X6	X3	X5
01	X4	X6	X5	X5
10	X4	X5	X3	X6
11	X4	X3	X5	X6

Table 20: Input Multiplexer for INMODE = 0

MUXIN	Addr 0x43, bit 1:0			
Code	PCH1i	NCH1i	PCH2i	NCH2i
-0	X4	X2	X3	X2
-1	X4	X2	X5	X2

Table 21: Input Multiplexer for INMODE = 1

EAZ permits the activation of an analog comparator for index channel CH0.

EAZ	Addr 0x43, bit 7
Code	Function
0	Comparator bypass
1	Comparator active

Table 22: Index Output

For output purposes INVZ allows the index signal phase to be inverted.

INVZ	Addr 0x43, bit 3	
Code	PZ_out	NZ_out
0	PCH0o	NCH0o
1	NCH0o	PCH0o

Table 23: Index Signal Inversion

SIGNAL CONDITIONING CH1, CH2

The voltage signals necessary for the conditioning of channels 1 and 2 can be measured in operation mode *Calibration 2*.

Gain Settings CH1, CH2

The gain is set in four stages:

1. The automatic gain control is shut down (set register AGCOFF to a value of 1).

2. The gain range is selected so that the differential signal amplitude of CH1 is closest to 1 Vpp (signal Px vs. Nx, see Figure below).

3. The automatic gain control is turned on (set register AGCOFF to a value of 0) and adjust ADJ to obtain a signal amplitude of 1 Vpp for CH1.

4. The CH2 signal amplitude can then be adjusted relative to the CH1 signal amplitude via gain correction ratio GC2.

AGC gain range reserve can be checked by the value of read-only register AGCGF1 which represents the 8 most significant bits of the current automatic gain setting for channel 1.
NB: automatic gain control is halted during AGCGF1 readout and will continue automatically afterwards.

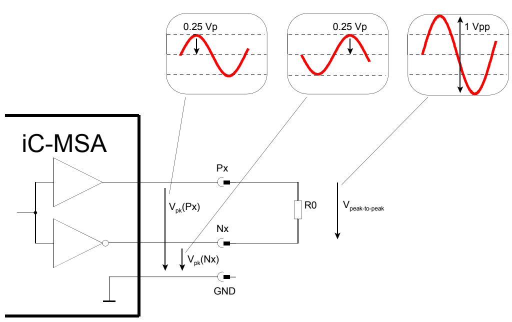


Figure 6: Definition of 1 Vpp signal. Termination R0 must be high-ohmic during all *Test* and *Calibration* modes.

GR12	Addr 0x46, bit 2:0	
Code	AGC on (AGCOFF = 0)	AGC off (AGCOFF = 1)
0x0	0.20 .. 2.77	0.75
0x1	0.34 .. 4.69	1.27
0x2	0.51 .. 7.03	1.89
0x3	0.71 .. 9.82	2.65
0x4	1.01 .. 13.8	3.73
0x5	1.28 .. 17.7	4.77
0x6	1.68 .. 23.2	6.24
0x7	2.11 .. 29.1	7.83

Table 24: Gain Range CH1, CH2 with voltage divider inputs (RIN12=0x9)

GR12	Addr 0x46, bit 2:0	
Code	AGC on (AGCOFF = 0)	AGC off (AGCOFF = 1)
0x0	0.80 .. 11.1	2.98
0x1	1.36 .. 18.8	5.06
0x2	2.04 .. 28.1	7.58
0x3	2.85 .. 39.3	10.6
0x4	4.02 .. 55.4	14.9
0x5	5.14 .. 70.8	19.1
0x6	6.73 .. 92.6	25.0
0x7	8.44 .. 116	31.3

Table 25: Gain Range CH1, CH2 (RIN12≠0x9)

GC2	Addr 0x4F, bit 7:0
Code	Ratio
0x00	0.8292
0x01	0.8304
...	$20^{\frac{GC2-128}{2047}}$
0x80	1.00
...	$20^{\frac{GC2-128}{2047}}$
0xFE	1.2025
0xFF	1.2043

Table 26: Gain Correction Ratio CH2/CH1

AGCGF1	Addr 0x59, bit 7:0
Value	AGC reserve
0xF0	alarm (±0.0 dB)
0x80	0.27 .. 3.7 (±11.4 dB)
0x5E...92	0.33 .. 3.0 (±9.5 dB)
0x4B...B4	0.50 .. 2.0 (±6.0 dB)
0x33...CD	0.67 .. 1.5 (±3.5 dB)
0x10	alarm (±0.0 dB)

Table 27: Minimum AGC Reserve (read only)

Offset Calibration CH1, CH2

In order to calibrate the offset the reference source must first be selected using VOS12. Two fixed voltages and one dependent source are available for this purpose.

VOS12	Addr 0x4E, bit 5:4
Code	Type of source
0x0	Feedback of sensor supply voltage: VDDS for supply-dependent differential voltage signals for Wheatstone sensor bridges
0x1, 0x2	Fixed reference: V05 of 500 mV, V025 of 250 mV for single-ended or differential signals (regulated sensor or waveform generator)
0x3	not permitted

Table 28: Offset Reference Source CH1, CH2

The calibration range for the CH1/CH2 offset is dependent on the selected VOS12 source and is set using OR1 and OR2. Both sine and cosine signals are then calibrated using factors OF1 and OF2. The calibration target is reached when the DC fraction of the differential signals PCHx versus NCHx is zero.

OR1 **OR2**	Addr 0x49, bit 0; Addr 0x48, bit 7 Addr 0x4A, bit 5:4
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 29: Offset Range CH1, CH2

OF1 **OF2**	Addr 0x4A, bit 3:0; Addr 0x49, bit 7:1 Addr 0x4C, bit 0; Addr 0x4B, bit 7:0; Addr 0x4A, bit 7:6		
Code	Factor	Code	Factor
0x000	0	0x400	0
0x001	+ 0.00098	0x401	– 0.00098
...	+ Code / 1023	...	– (Code - 1024) / 1023
0x3FF	+ 1	0x7FF	– 1

Table 30: Offset Factors CH1, CH2

Phase Correction CH1 vs. CH2

The phase shift between CH1 and CH2 can be adjusted using parameter PH12. Following phase calibration other calibration parameters may have to be adjusted again (those as gain ratio, intermediate potentials and offset voltages).

PH12	Addr 0x4D, bit 2:0; Addr 0x4C, bit 7:1		
Code	Correction angle	Code	Correction angle
0x000	0 °	0x200	0 °
0x001	+ 0.0204 °	0x201	– 0.0204 °
...	+ 10.42 ° · PH12 / 511	...	– 10.42 ° · (PH12 - 512) / 511
0x1FF	+ 10.42 °	0x3FF	– 10.42 °

Table 31: Phase Correction CH1 vs. CH2

SIGNAL CONDITIONING CH0

The voltage signals needed to calibrate channel 0 are available in *Calibration Mode 1*.

Gain Settings CH0

The CH0 gain is set in the following stages:

1. Adjust CH1 and CH2.

2. Set gain range GR0 to the same value as GR12.

3. GC0 then permits fine gain ratio adjustment relative to CH1.

GR0	Addr 0x51, bit 2:0	
Code	AGC on (AGCOFF = 0)	AGC off (AGCOFF = 1)
0x0	0.20 .. 2.77	0.75
0x1	0.34 .. 4.69	1.27
0x2	0.51 .. 7.03	1.89
0x3	0.71 .. 9.82	2.65
0x4	1.01 .. 13.8	3.73
0x5	1.28 .. 17.7	4.77
0x6	1.68 .. 23.2	6.24
0x7	2.11 .. 29.1	7.83

Table 32: Gain Range CH0 with voltage divider inputs (RIN0=0x9)

GR0	Addr 0x51, bit 2:0	
Code	AGC on (AGCOFF = 0)	AGC off (AGCOFF = 1)
0x0	0.80 .. 11.1	2.98
0x1	1.36 .. 18.8	5.06
0x2	2.04 .. 28.1	7.58
0x3	2.85 .. 39.3	10.6
0x4	4.02 .. 55.4	14.9
0x5	5.14 .. 70.8	19.1
0x6	6.73 .. 92.6	25.0
0x7	8.44 .. 116	31.3

Table 33: Gain Range CH0 (RIN0≠0x9)

GC0	Addr 0x50, bit 7:0
Code	Ratio
0x00	0.8292
0x01	0.8304
...	$20^{\frac{GC0-128}{2047}}$
0x80	1.00
...	$20^{\frac{GC0-128}{2047}}$
0xFE	1.2025
0xFF	1.2043

Table 34: Gain Correction Ratio CH0/CH1

Offset Calibration CH0

To calibrate the offset the source of supply must first be selected using VOS0 (see Offset Calibration CH1 and CH2 for further information).

VOS0	Addr 0x53, bit 5:4
Code	Source
0x0	0.05 · V(VDDS)
0x1	0.5 V
0x2	0.25 V
0x3	not permitted

Table 35: Offset Reference Source CH0

OR0	Addr 0x52, bit 1:0
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 36: Offset Range CH0

OF0	Addr 0x52, bit 7:2		
Code	Factor	Code	Factor
0x00	0	0x20	0
0x01	+ 0.0322	0x21	− 0.0322
...	+ OF0 /31	...	− (OF0 - 32) /31
0x1F	+ 1	0x3F	− 1

Table 37: Offset Factor CH0

AUTOMATIC SIGNAL GAIN CONTROL and SIGNAL MONITORING

Via its automatic gain control iC-MSA can keep the output signals for the ensuing sine-to-digital conversion constant regardless of changes in input signal level.

Both the controller operating range and input signal amplitude for the controller are monitored and can be enabled for error messaging.

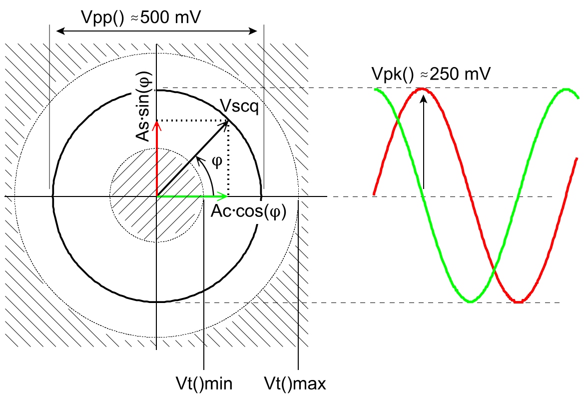


Figure 7: Signal level monitoring with square control (example for AGCOFF = 0, ADJ = 0x32; see Elec. Char. Nos.604 and 605 regarding Vt()min resp. Vt()max).

AGCOFF	Addr 0x45, bit 7
Code	Function
0	Sine/cosine square control
1	AGC turned off

Table 38: Controller Operating Mode

ADJ	Addr 0x45, bit 5:0
Code	**Square control** AGCOFF = 0
0x00	Vpp() ca. 300 mV (60 %)
0x01	Vpp() ca. 305 mV (61 %)
...	Vpp() $\approx 300\,mV\,\frac{77}{77-(0.625*Code)}$
0x32	Vpp() ca. 500 mV (98 %)
...	...
0x3F	Vpp() ca. 600 mV (120 %)

Table 39: Vpp Setpoint For Square Control

ERROR MONITORING AND ALARM OUTPUT

The following table gives the errors which can both be recognized by iC-MSA and enabled either for messaging, output shutdown or protocol in the EEPROM.

Mask EMASKA stipulates that errors should be signaled at pin ERR, mask EMASKO determines whether the line drivers are to be shutdown or not (with PDMODE defining reactivation) and mask EMASKE governs the storage of error events in the EEPROM.

EMASKA	Addr 0x54, bit 6:0
EMASKO	Addr 0x56, bit 6:0
EMASKE	Addr 0x58, bit 2:0; Addr 0x57, bit 7:4
Bit	Error Event
6*	Configuration error (SDA or SCL pin error, no Ack signal from EEPROM or invalid check sum); EMASKO(6) = 1 (ROM bit): The line drivers remain high impedance (tristate) when cycling power.
5	Excessive temperature warning
4	External system error
3	Control error 2: range at max. limit
2	Control error 1: range at min. limit
1	Signal error 2: clipping
0	Signal error 1: loss of signal (poor differential amplitude**, wrong s/c phase)
EMASKA	Error Mask Alarm Output ERR
1	Enable: event changes state of pin ERR (if EMASKO does not disable the output function).
0	Disable: event does not affect pin ERR.
EMASKO	Error Mask Driver Shutdown
1	Enable: event resets pin ACO to the 5 mA range, tristates the line driver outputs and pin ERR (i.e. low-active error messages can not be displayed)
0	Disable: output functions remain active
EMASKE	Error Mask EEPROM Savings
1	Enable: event will be latched
0	Disable: event will not be latched
Notes	*) Pin ERR can not pull low on configuration error, use high-active error logic instead (EPH = 1); **) Also due to excessive input signals or internal signal clipping.

Table 40: Error Masking

Alarm Output: I/O pin ERR

Pin ERR is operated by a current-limited open drain output driver and has an internal pull-up which can be shutdown. The ERR pin also acts as an input for external system error messaging and for switching iC-MSA to test mode for which a voltage of greater than VTMon must be applied. Interpretation of external system error messaging and the phase length of the message output can be set using EPH; the minimum signaling duration for internal errors is adjusted using EMTD.

EPH	Addr 0x55, bit 2	
Code	State on error	State w/o error
0	active low	high impedance, with input function for a low-active system error;
1	high impedance	active low

Table 41: I/O Logic, Alarm Output ERR

EMTD	Addr 0x55, bit 5:3		
Code	Indication Time	Code	Indication Time
0x0	0 ms	0x4	50 ms
0x1	12.5 ms	0x5	62.5 ms
0x2	25 ms	0x6	75 ms
0x3	37.5 ms	0x7	87.5 ms

Table 42: Min. Indication Time, Alarm Output ERR

EPU	Addr 0x57, bit 2
Code	Function
0	No internal pull-up
1	Internal 300 µA pull-up current source active

Table 43: Pull-Up Enable, Alarm Output ERR

Excessive Temperature Warning

Exceeding the temperature warning threshold T_w (corresponds to T_2, refer to Tempeprature Sensor, page 15) can be signaled at pin ERR or used to shut down the line drivers (via mask EMASKO). The temperature warning is cleared when the temperature falls below $T_w - T_{hys}$.

Notice: If the temperature shutdown threshold $T_{off} = T_w + \Delta T$ is exceeded, the line drivers are shut down independently of EMASKO. For ΔT refer to Elec. Char. E06.

Driver Shutdown

PDMODE	Addr 0x58, bit 6
Code	Function
0	Line driver active when no error persists
1	Line driver active after power-on

Table 44: Driver Activation

Error Protocol

Out of the errors pinpointed by EMASKE both the first (under ERR1) and last error (under ERR2) which occur after the iC-MSA is turned on are stored in the EEPROM.

The EEPROM also has a memory area in which all occurring errors can be stored (ERR3). Only the fact that an error has occurred can be recorded, with no information as to the time and frequency of that error given. The EEPROM memory can be used to statistically evaluate the causes of system failure, for example.

ERR1	Addr 0x60, bit 6:0
ERR2	Addr 0x62, bit 0; Addr 0x61, bit 7:2
ERR3	Addr 0x63, bit 2:0; Addr 0x62, bit 7:4
Bit	Error Event
6:0	Assignation according to EMASKE
Code	Function
0	No event
1	Registered error event

Table 45: Error Protocol

REVERSE POLARITY PROTECTION

The line drivers in iC-MSA are protected against reverse polarity and short-circuiting. A defective device cable or one wrongly connected cause damage neither to iC-MSA nor to the components protected against reverse polarity by VDDS and GNDS. The following pins are also reverse polarity protected: PC, NC, PS, NS, PZ, NZ, ERR, VDD, and GND (as long as GNDS is only loaded versus VDDS). The maximum voltage difference between the pins should not be greater than 6 V, the exception here being pin ERR.

APPLICATION HINTS

PLC Operation

There are PLCs with a remote sense supply which require longer for the voltage regulation to settle. At the same time the PLC inputs can have high-impedance resistances versus an internal, negative supply voltage which define the input potential for open inputs.

In this instance iC-MSA's reverse polarity protection feature can be activated as the outputs are tristate during the start phase and the resistances in the PLC determine the pin potential. During the start phase neither the supply VDD nor the output pins, which are also monitored, must fall to below ground potential (pin GND); otherwise the device is not configured and the outputs remain permanently set to tristate.

In order to ensure that iC-MSA starts with the PLCs mentioned above pull-up resistors can be used in the encoder. Values of 100 kΩ are usually sufficient; it is, however, recommended that PLC specifications be specifically referred to here.

Connecting MR sensor bridges for safety-related applications

For safety-related applications iC-MSA requires an external overvoltage protection of supply VDD (Zener diode with fuse, for instance) and external pull-down resistors at the inputs X3 to X6 towards GNDS (of up to 100 kΩ).

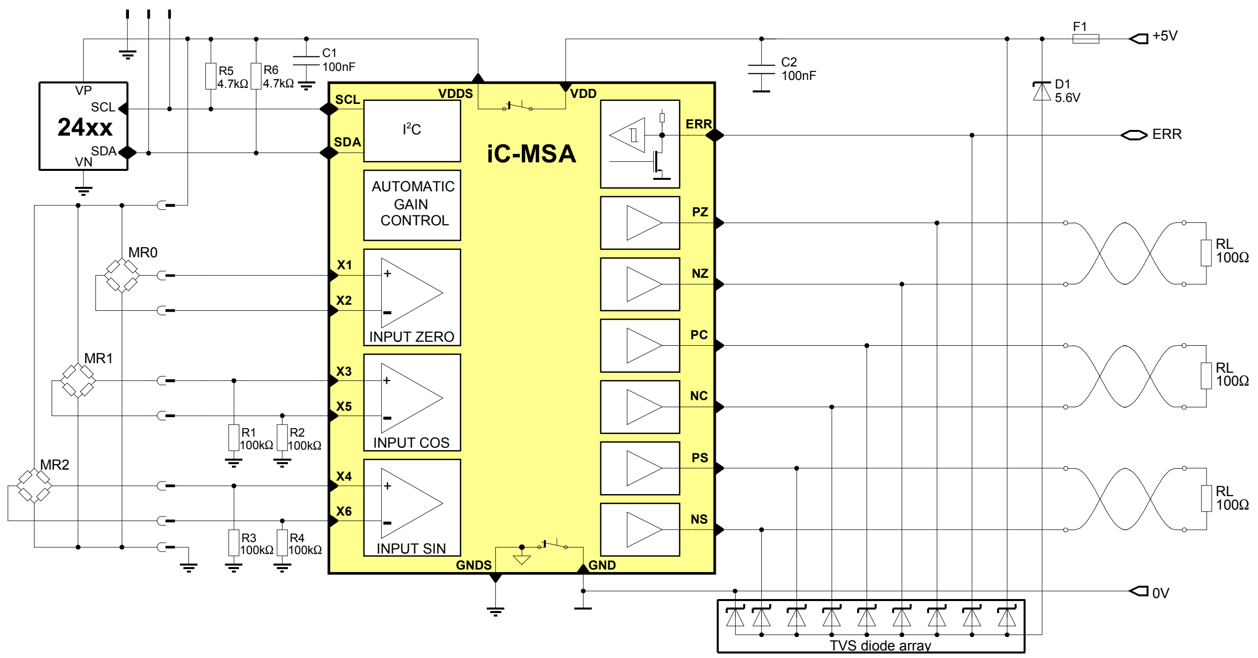


Figure 8: Example circuit for safety-related applications with iC-MSA.

Motor feedback encoder with iC-MSA, iC-MSB and single EEPROM

In this application iC-MSB is fed with typically 2048 CPR sine and cosine signals, and an index signal. A constant signal level is achieved by controlling the sensor's LED current. iC-MSA is utilized to provide C/D commutation signals, typically with 1 CPR, at a constant amplitude. At higher rotation speed the sine/cosine amplifier cut-off-frequency is exceeded and iC-MSB increases the LED current. In order to keep the low frequency signals of C/D constant, iC-MSA automatically reduces the gain.

iC-MSA and iC-MSB are multi-master I^{2}C capable and feature non-overlapping configuration register addresses. Thus, both devices can share a single EEPROM providing individual configuration data.

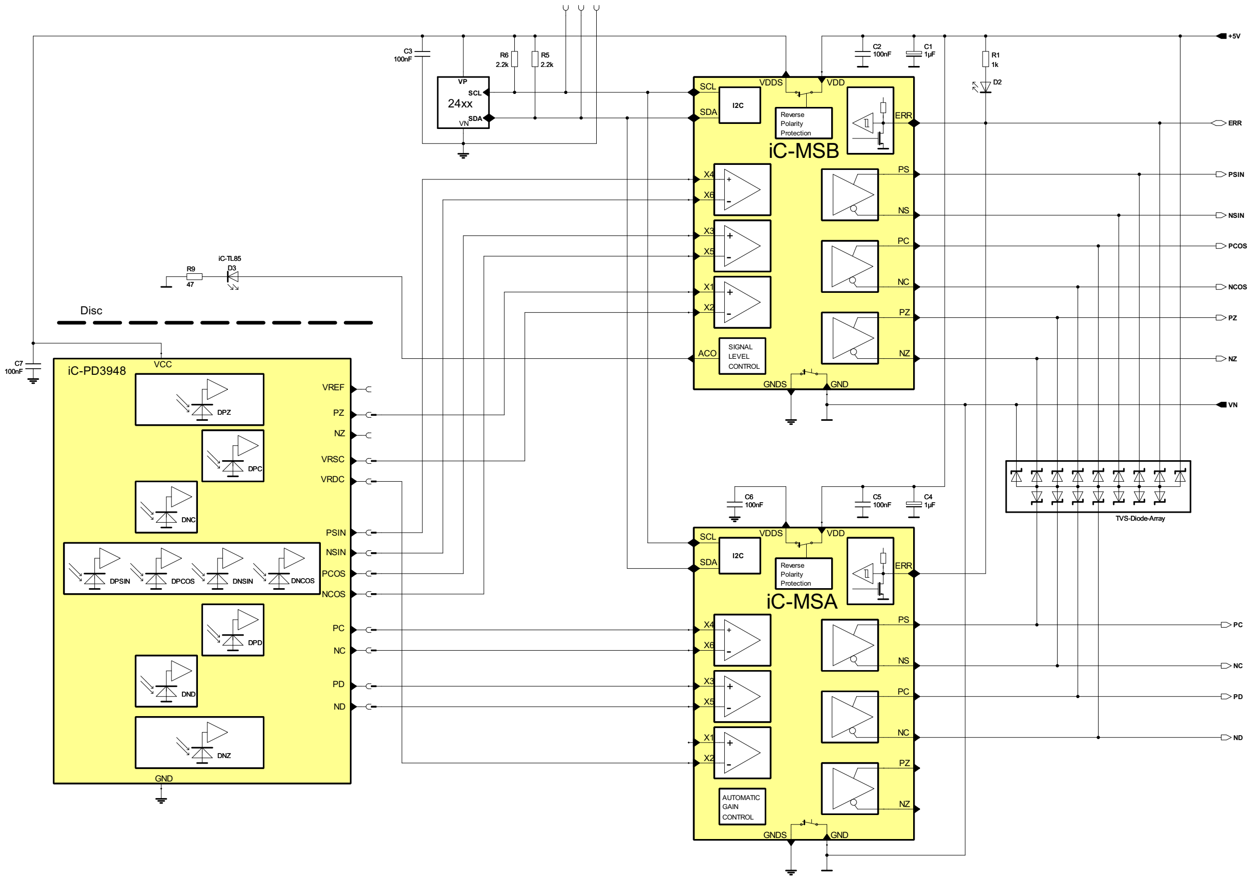


Figure 9: Example circuit with iC-MSA, iC-MSB and single EEPROM.

ORDERING INFORMATION

Type	Package	Order Designation
iC-MSA	TSSOP20 with thermal pad	iC-MSA TSSOP20-TP

For technical support, information about prices and terms of delivery please contact:

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