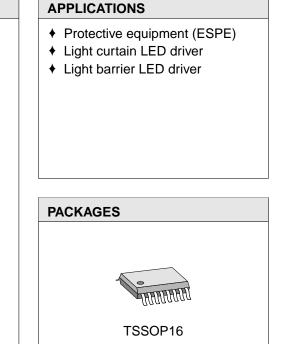
iC-NX 8-CHANNEL LIGHT-GRID PULSE DRIVER



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FEATURES

- ♦ 1 to 8 channels (hardware programmable)
- LED pulse current can be adjusted from 0.4 to 1.8 A via a single external low power resistor
- Positive pulse current temperature coefficient permits compensation of decreases in LED efficiency
- ♦ Short light pulses from 0.5 µs with steep edges
- Low standby current; device activated by input data
- Diagnostic message generated with LED interrupts
- ♦ LED short-circuit recognition
- ♦ Control logic with three-stage shift register
- Output buffer with 120 Ω line adaptation
- Supply voltage range of 4.75 to 6 V
- Thermal and low-voltage shutdown
- Integrated protection against ESD
- Configured for safety systems according to IEC 1496-1
- ♦ Optional extended temperature range of -20 to 85 °C



BLOCK DIAGRAM +4.75..6V O $\forall \checkmark \checkmark$ PROG LED1 LED4 . VDD LED2 LED3 LED5 . LED6 0-CHAN1 LOGIC INPU1 _ 1≤ FF2 CONTROL INPUT SHEN LED CURRENT SINK POWER DOWN TERMA OUTPUT BUFFER RESET SHUTDOWN BANDGAP iC–NX GND ISET RSET



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DESCRIPTION

iC-NX is an eight-fold LED pulse driver for light curtain systems and light barriers.

The device, which is controlled by a shift register, features an adjustable LED current sink with a set range of 0.4 to 1.8 A (at room temperature). The three stages of the shift register cell enable data to be safely transported, free of race conditions, in order to activate the pulse driver connected in a chain in a light curtain application.

The positive temperature coefficient of the LED current sink largely compensates for the decrease in LED efficiency with a rise in temperature. Active discharge provided by short-circuiting the junction capacitance of the LED enables steep light pulses to be generated. The duration of this short circuit is determined by a monoflop which keeps the discharge path of the LED at a low impedance. In the event of light pulses occurring in rapid succession the monoflop is automatically reset to prevent cross currents.

The current sink common to all eight channels prepares for a light pulse when DIN and subsequently one of the internal data inputs DIi (i = 1...8) reads a high signal (NENABLE = Io). With the rising edge of CLK the first flip-flop in the active channel takes on the value of DIi and switches the current sink to output LEDi. The LED current sink is disconnected from the LEDi output with the rising edge of the next clock pulse. The duration of the LED current pulse is thus determined by the time difference between two rising CLK edges and should be no less than 0.5 µs.

The next channel in the chain is activated when at the falling edge of the second clock pulse the shift register transfers the high to output DOi. This must be enabled by SHEN being high; if this is not the case, a clock-synchronised reset of the entire chain is triggered.

iC-NX signals a broken LED connection or insuf-

ficient LED current by manipulating the input current at enable input SHEN which acts as a bidirectional diagnostic interface. When the device is activated (NENABLE = lo) the input resistance is usually 2.5 k Ω . The resistor is switched to GND when SHEN is high and to VDD when SHEN is low.

Should the set LED current not reach its specified value between two clock pulses a current comparator switches the input resistor off at SHEN. In the event of a fault a gap in input current is thus produced at the enable input which can be analysed externally.

Short circuits at the LED outputs are also verified; these directly alter data transfer within the shift register. An LEDON signal cannot be generated for LED pins which short circuit with the supply line; the data shift is blocked, causing the entire shift register to record zeros. A short circuit from output to output, however, fills the shift register step by step and several LEDs are supplied with partial current. When the next device in the chain is activated the doubled power consumption can be recognised by the system control via the supply line.

iC-NX can be programmed to bridge any channels with the exception of channel 1. To this end the unused LED pins (pins without an LED) are connected to pin PROG. The corresponding registers are removed from the chain by a bypass and are no longer relevant to the device's functions.

In the event of excessive temperature or low voltage the shift register is reset and the LED current sink turned off. Driver and logic outputs are currentlimited and short-circuit-proof, as the device is powered down with excessive temperature. Integrated protective diodes prevent destruction by ESD.

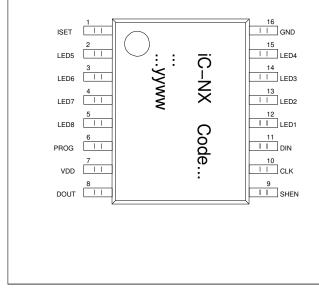
iC-NX adheres to safety requirements according to IEC 1496-1. An optional extended temperature range of -20 to 85 °C is also available.



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PACKAGES TSSOP16 to JEDEC standard

PIN CONFIGURATION TSSOP16 4.4 mm (top view)



PIN FUNCTIONS No. Name Function

1 ISET Current Adjust, attachment RSET 2 LED5 Pulse Output, LED5 Cathode 3 LED6 Pulse Output, LED6 Cathode 4 LED7 Pulse Output, LED7 Cathode 5 LED8 Pulse Output, LED8 Cathode 6 PROG Channel Bypass Programming +4.75 to 6 V Supply Voltage 7 VDD 8 DOUT Data Output 9 SHEN Shift Enable Input, low active 10 CLK **Clock Input** 11 DIN Data Input 12 LED1 Pulse Output, LED1 Cathode 13 LED2 Pulse Output, LED2 Cathode 14 LED3 Pulse Output, LED3 Cathode 15 LED4 Pulse Output, LED4 Cathode 16 GND Ground



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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

ltem	Symbol	Parameter	Conditions	Fig.			Unit
No.	-				Min.	Max.	
G001	VDD	Supply Voltage			-0.5	6.2	V
G002	V()	Voltage at Inputs DIN, CLK, SHEN			-0.5	VDD + 0.5	V
G003	V()	Voltage at DOUT, ISET, LED			-0.5	VDD + 0.5	V
G004	Vd()	ESD Susceptibility at VDD, ISET and all digital In- and Outputs	MIL-STD-883, HBM 100 pF discharged through 1.5 k Ω			2	kV
G005	Vd(LED)	ESD Susceptibility at LED	with standard circuitry, HBM 100 pF discharged through 1.5 $k\Omega$	5		2	kV
G006	Tj	Junction Temperature			-40	150	°C
G007	Ts	Storage Temperature			-40	150	°C
G008	TL	Lead Temperature	soldering 10 s max.			260	°C

THERMAL DATA

Operating Conditions: VDD = 4.75...6.0 V

Item	Symbol	Parameter	ameter Conditions Fig.			Unit		
No.	-			-	Min.	Тур.	Max.	
T01		Operating Ambient Temperature Range (extended temperature range of -20 to 85 °C on request)			0		70	°C
T02	Rthja	Thermal Resistance Junction to Ambient	surface mounted without special cooling areas				120	k/W



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ELECTRICAL CHARACTERISTICS

tem No.	Symbol	Parameter	Conditions	Tj ℃	Fig.	Min.	Тур.	Max.	Unit
Total	Device			1	1				
001	VDD	Permissible Supply Voltage range				4.75		6	V
002	I(VDD)	Supply Current in VDD (LED current source not active, static)	NENABLE = hi, DIN = lo, CLK, SHEN = hi or lo, logic levels: lo = 00.45 V, hi = VDD - 0.45 VVDD					480	μA
003	I(VDD)	Supply Current in VDD (LED current source active)	NENABLE = Io, SEND18 = 0, RSET $\ge 1.8 \text{ k}\Omega$	-20 27 85 Toff				8 8 9 1	mA mA mA mA
004	I(VDD)	Supply Current in VDD (LEDi turned on)	NENABLE = lo, SENDi = 1, RSET ≥ 1.8 kΩ	-20 27 85 Toff				25 25 25 1	mA mA mA mA
005	I(PROG)	Supply Current in RROG	V(PROG) > 2 V	27		5			mA
006	VDDon	Turn-on Threshold VDD (Power-on Release)						3.75	V
007	VDDoff	Undervoltage threshold at VDD (Power-down Reset)	decreasing voltage VDD	85		2.2 2.1		3.75	V V
800	VDDhys	Hysteresis	VDDhys = VDDon - VDDoff				250		mV
009	Vc()hi	Clamp voltage hi at DIN, CLK, SHEN, DOUT, ISET, PROG	Vc()hi = V() - VDD; I() = 1 mA			0.4		1.25	V
010	Vc()hi	Clamp voltage hi LED	Vc()hi = V() - VDD; I() = 10 mA			0.4		1.25	V
011	Vc()lo	Clamp voltage lo at DIN, CLK, SHEN, DOUT, ISET, PROG, LED	VDD = 0 V, I() = -10 mA, other pins open			-1.25		-0.4	V
012	Toff	Shutdown temperature				110		150	°C
LED C	urrent Sink	<u>د</u>							
101	V(ISET)	Reference voltage at ISET		-20 27 85 Toff			1.27 1.50 1.79 0		V V V V
102	TC(ISET)	Temperature Coefficient of Reference Voltage at ISET		27		0.30	0.33	0.36	%/K
103	CR()	Current Ratio I(LED)/-I(ISET)					1200		
104	I(LED)	LED Pulse Current	duty cycle I(LED)	-20 27 85 Toff		1.15 1.46 1.66	1.53 1.80 2.15 0	1.90 2.14 2.69	A A A A
105	I(LED)	LED Pulse Current	duty cycle I(LED)	-20 27 85 Toff		0.65 0.82 0.93	0.85 1.00 1.2 0	1.06 1.18 1.48	A A A A
106	I(LED)	LED Pulse Current	duty cycle I(LED)	-20 27 85 Toff		0.26 0.33 0.37	0.34 0.40 0.48 0	0.44 0.48 0.61	A A A A
107	tr(LED)	LED Current Rise Time			3			150	ns
108	tf(LED)	LED Current Fall Time			3			150	ns
109	tdis(LED)	LED Discharge Duration	NENABLE = hi, switch Sdis closed					6	μs
110	lr(LED)	LED Discharge Current	V(VDD/LED) = 1.5 V				200		mA
111	R(LED)	Pull-up Resistor at LED				2	4	7	kΩ
112	Vt(LED)hi	LED Voltage Monitoring Threshold	Vt(LED)hi = VDD - V(LED)			0.5		1.0	V
113	IOK	LED Current Monitoring Threshold	lset = CR() x I(ISET)			1		70	%lse



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ELECTRICAL CHARACTERISTICS

ltem No.	Symbol	Parameter	Conditions	Tj ℃	Fig.	Min.	Тур.	Max.	Unit
Contr	ol Inputs D	N, CLK, SHEN							
201	Vt()hi	Threshold Voltage hi						67	%VDD
202	Vt()lo	Threshold Voltage lo				22			%VDD
203	Vhys()	Input Hysteresis				400			mV
204	lpd()	Pull-Down Current	V() = VDD			3	6	15	μA
205	R(SHEN)	SHEN Pull-up/down Resistance				1.7	2.5	3.6	kΩ
206	tp(SHEN)	SHEN Resistance Switch-Delay					150		ns
Outpu	t Buffer DC	UT							
301	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(DOUT), I() = -4 mA					0.4	V
302	Vs()lo	Saturation Voltage lo	I() = 4 mA					0.4	V
303	lsc()hi	Short-Circuit Current hi	V() = 0 V			-100	-40	-20	mA
304	lsc()lo	Short-Circuit Current lo	V() = VDD			20	40	100	mA
305	Rout()	Output Resistance	VDD = 5.0 V, V() = 2.5 V			80	120	190	Ω
306	tr()	Rise Time	$CL() \leq 50 pF$				20	60	ns
307	tf()	Fall Time	$CL() \leq 50 pF$				20	60	ns
Switc	hing Chara	cteristics							
401	tphl(CLK- LED)	LED-Pulse Turn-on Delay	DIN = hi, CLK lo \rightarrow hi until l(LED) = 10 % of set value		4			100	ns
402	tplh(CLK- LED)	LED-Pulse Turn-off Delay	DIN = Io, CLK Io \rightarrow hi until I(LED) = 90 % of set value		4			80	ns
403	tplh(CLK- DOUT)	DOUT Switch Delay hi	$\mbox{CL(DOUT)}\leqslant 50\mbox{pF, CLK}$ hi \rightarrow lo		2		25	60	ns
404	tphl(CLK- DOUT)	DOUT Switch Delay lo	CL(DOUT) \leqslant 50 pF, CLK hi \rightarrow lo		2		25	60	ns

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OPERATING REQUIREMENTS: Logic

Operating Conditions: VDD = 4.75...6.0 V, Ta = 0...70 °C, CL() = 50 pF, input levels lo = 0...0.45 V, hi = VDD - 0.45...VDD, see Fig. 1 for reference levels and waveforms

ltem	Symbol	Parameter	Conditions	Fig.			Unit
No.	-				Min.	Max.	
1001	ten	Activation Time (standby to operation): DIN lo \rightarrow hi before CLK lo \rightarrow hi		4	5		μs
1002	tset	Setup time: DIN stable before CLK lo \rightarrow hi		2	50		ns
1003	thold	Hold Time: DIN stable after CLK lo \rightarrow hi		2	50		ns
1004	tw	LED Pulse time: 1^{st} to 2^{nd} CLK lo \rightarrow hi		4	0.5		μs

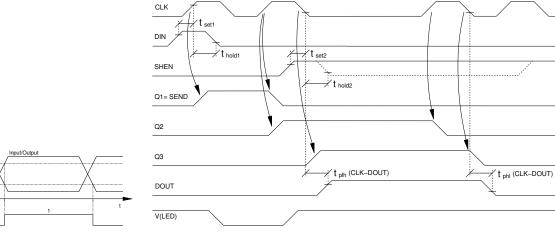


Figure 1: Reference levels

VDD - 0.45 V

Vt()h

Vt()lo 0.45 V

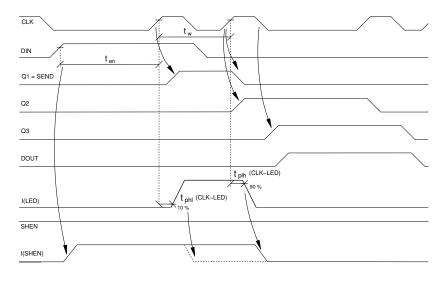


Figure 2: Timing characteristics

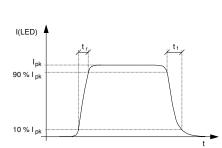


Figure 3: LED current pulse

Figure 4: LED current pulse definition by clock signal (dashed line denotes I(SHEN) in case of an interrupted LED path)



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APPLICATION HINTS

Light curtains

The circuit in Figure 5 shows several iC-NXs connected as a light curtain, where consecutive LEDs emit clock-driven light pulses. In this example iCa drives eight LEDs, with the hardware of the following device (iCb) specifically programmed to drive just four. A unique high signal at DINa is shifted from right to left with the shared pulse at CLK.

When discussing the function of iC-NX it is assumed that all of the flip-flops in iCa to iCx have been reset, such as is the case, for example, after the supply voltage has been switched on. When the signal at DINa is high iCa's current sink is activated and first switched to LED1 with the rising CLK edge. When DINa is low the next rising CLK edge resets the first flip-flop FF1 (see the block diagram on page 1) in iCa, turns off LED1 and deactivates the current sink in iCa. At the same time FF1 sends the stored information to FF2. FF3 accepts this information via the trailing CLK edge (provided that SHEN is high) and reactivates the current sink in the next channel in iCa via DO1.

The pulse diagram in Figure 6 is also valid for the subsequent channels and/or components in the chain, i.e. the iCs configured as a light curtain make up a clockdriven shift register which passes on the input information. With the ninth clock pulse the second device shown in the chain (iCb) is activated for four pulses as programmed.

The layout of the PCB must ensure that the wire resistance of the supply lines and the voltage drop which occur during operation along the entire length of the light curtain are sufficiently small. High, short-term pulse currents are provided by back-up capacitors Ca to Cx; these should have a low inductance due to the high increase rate of the current. With suitable capacitors the voltage drop caused by a light pulse can be less than 1 V, i.e. Ca to Cx is 1 μ F for a light pulse of 1 A x 1 μ s, for example. In practice the actual voltage drop at the iC is considerably less during a pulse as charge from the back-up capacitors of neighboring iCs also flows into the active device.

Low-inductance capacitance can be achieved more economically by placing several capacitors of low capacitance in parallel as opposed to using special lowinductance devices. Leads to the LED anodes and to iC-NX's ground pin should be as short as possible.

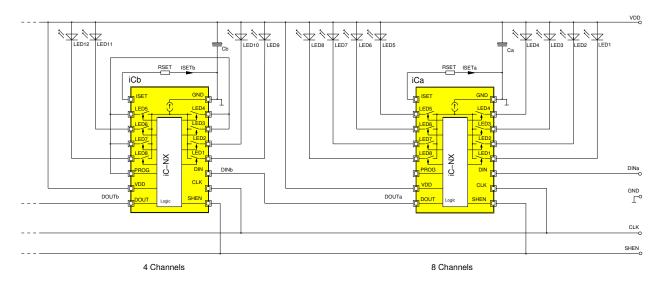


Figure 5: Schematic of a chain configuration



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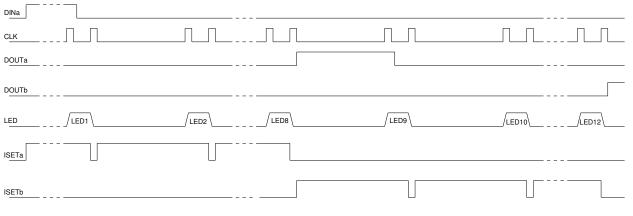


Figure 6: Signals of the chain configuration of Figure 5

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8-CHANNEL LIGHT-GRID PULSE DRIVER

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ORDERING INFORMATION

Туре	Package	Order Designation
iC-NX	TSSOP16 4.4 mm	iC-NX TSSOP16

For information about prices, terms of delivery, other packaging options etc. please contact:

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