Critical Conduction Mode PFC IC
FA5695N / FA5696N

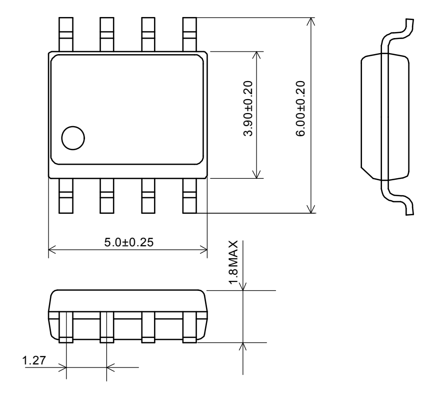
Datasheet

1. Overview

FA5695/FA5696 is power-factor correction converter IC operating in critical conduction mode. It realizes low power consumption by using high voltage CMOS process. It is equipped with many fault protection functions such as FB short-circuit detection circuit which stops the operation when abnormal output voltage is detected.

2. Features

- Very Low Standby Power by disusing Input Voltage Detection Resistors
- High-precision over current protection : 0.6V±5%
- Improved power efficiency at light load due to Maximum Frequency Limitation
- No Audible Noise at Startup
  Soft-Startup and Soft-OVP functions
- Low current consumption by CMOS process
  Start-up : 80μA(max.), Operating : 2mA(typ.)
- Enabled to drive power MOSFET directly
  Output peak current, source : 1000mA, sink : 1000mA
- Protects the output electrolytic capacitor by the double OVP function, even if a fault happen in the output detection.
- Open/short protection at feedback (FB) pin
- Under-voltage Lockout:
  FA5695 : 13V ON / 9V OFF FA5696 : 9.6V ON / 9V OFF
- Restart timer
- Standby function
- 8-pin package (SOP)

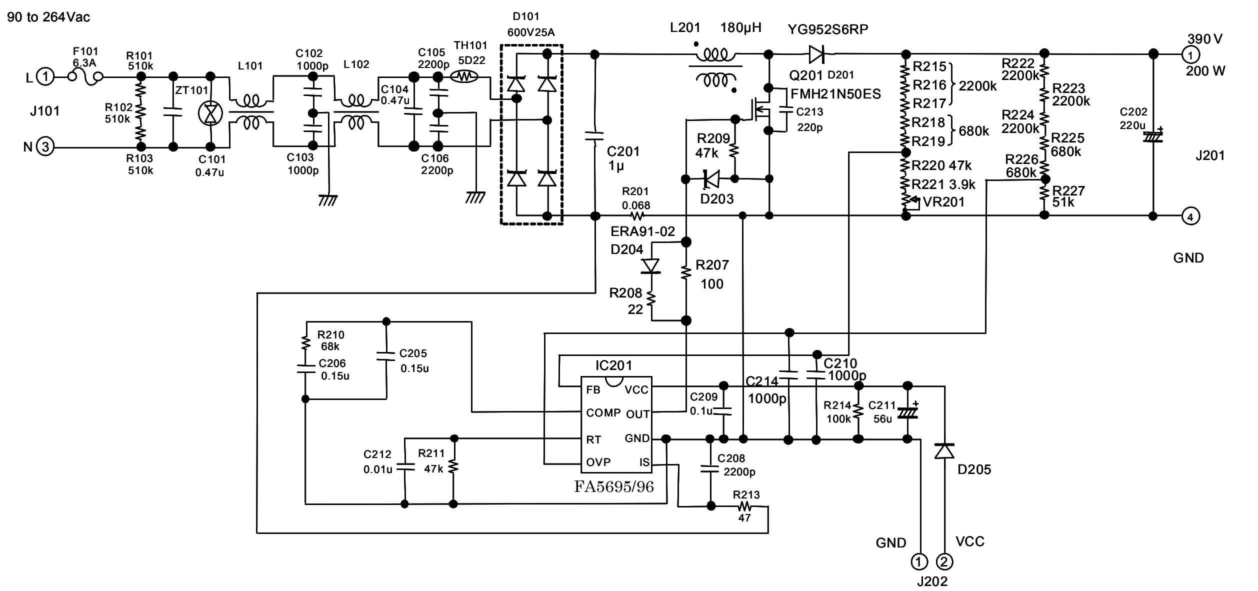


Package：SOP-8

3. Function list by types

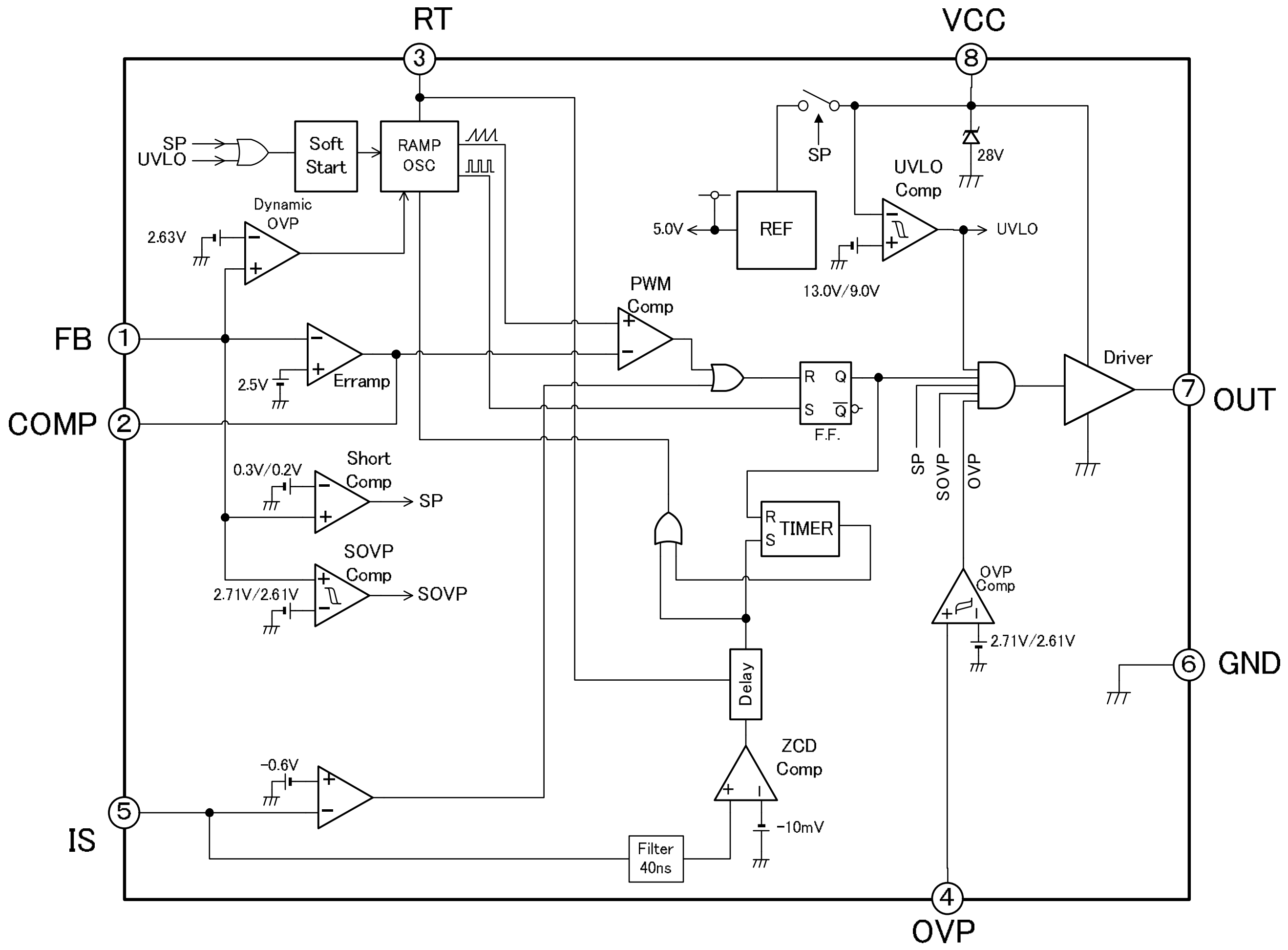
Type	Startup Threshold	Double OVP function
FA5695N	13V(typ.)	○
FA5696N	9.6V(typ.)	○

4. Application circuit example



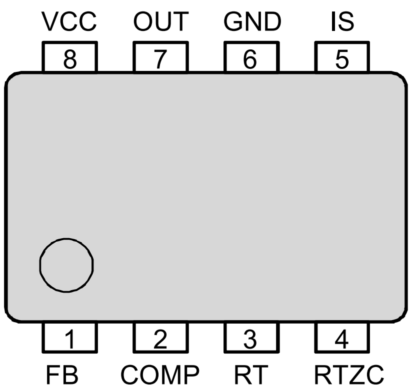
5. Block diagram

FA5695N / FA5696N



6. Functional description of pins

Pin No.	Pin name	Pin Function
1	FB	Feedback Voltage Input *1
2	COMP	Compensation *1
3	RT	Set Maximum on time *1
4	OVP	Over voltage detection *1
5	IS	Current Sense Input *1
6	GND	Ground
7	OUT	Output
8	VCC	Power Supply *1



Notes)
*1 connect the capacitor.

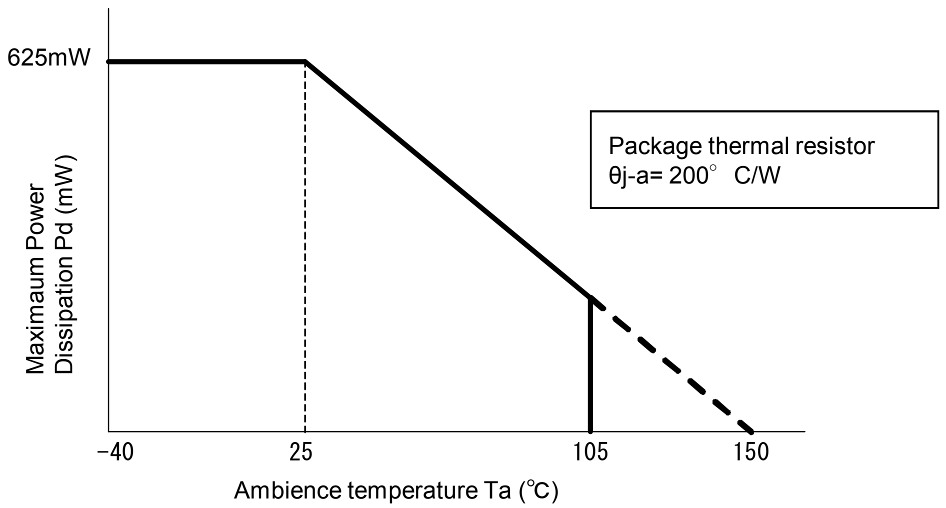
7. Rating & characteristics

Stress exceeding absolute maximum ratings may malfunction or damage the device.
“-” shows source and “+” shows sink in current descriptions.

(1) Absolute maximum ratings

Item	Symbol	Value	Unit
Total power supply and zener current	Ivcc+Iz	15	mA
Supply Voltage	Vcc	28	V
Output Current	Io	-500 to 1000	mA
Input voltage (FB,COMP,RT,OVP)	Vinfb,Vincomp, Vinrt,Vinovp	-0.3 to 5	V
Input voltage (IS)	Vinis	-5 to 0.3	V
Input current (FB, COMP, RT, OVP, IS)	Iinfb,Iincomp, Iinrt,Iinovp	-100 to 100	uA
Power dissipation	Pd	625	mW
Operating Junction Temperature	Tj	-40 to 150	℃
Storage Temperature	Tstg	-40 to 150	℃

※Maximum dissipation curve



(2) Recommended operating conditions

Item	Symbol	MIN	TYP	MAX	Unit
Supply Voltage	Vcc	10	12	26	V
VCC pin electrolyte capacitor	Cvcce	10	-	-	uF
VCC pin ceramic capacitor	Cvccc	0.1	-	-	uF
RT pin resistance	Rrt	20	82	150	kΩ
FB, OVP pin resistance	Rfb, Rovp	-	-	8	MΩ
IS pin filter resistance	Risf	-	-	100	Ω
Operating ambient temperature	Ta	-40	-	+105	℃

(3) DC electrical characteristics

The characteristics in this section are those in conditions as follows unless otherwise specified. The voltages described in the conditions are DC input, not AC input.

Tj=25℃, VCC=12V, VFB=1.0V, VCOMP=5V, VOVP=0V, VIS=100mV, OUT=OPEN, Rrt=82KΩ

Notes) (1) The item which indicated "*1" are not 100% tested and guaranteed by design.
(2) "－" means that it is not guaranteed.
(3) "-" shows source current and "+" shows sink current in output characteristics.

ERROR AMPLIFIER (FB Pin, COMP Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Voltage Feedback Input Threshold	Vfb		2.465	2.500	2.535	V
Line Regulation	Regline	Vcc=10V to 26V	-20	-10	-	mV
Temperature stability *1	VdT	Tj=-30℃ to 85℃	-	±0.5	-	mV/℃
Transconductance	Gm	VFB(DC)=2.25V, 2.75V VCOMP(DC)=2.5V Gm=Icomp_2.75-Icomp_2.25/(2.75-2.25)	50	75	100	μmho
Output current at startup	Icompso_st	Source:V(FB)=1.0V	-60	-40	-20	uA
FB pin threshold voltage when source current up	Vfb_Icomp so_p	V(FB) decrease	0.925 ∗Vfb	0.945 ∗Vfb	0.965 ∗Vfb	V
Output Current	Icompso	Source:V(FB)=1.0V V(COMP)=2.5V	-80	-60	-40	μA
	Icompsi	Sink:V(FB)=4.0V V(COMP)=2.5V	30	50	70	

RAMP OSCILLATOR (RT Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum on range	Tonmax	V(FB)=Vfb	24	30	36	us
Maximum on range (Soft start)	Tonmax _ss	V(FB)=1.0V	18	24	30	us
Maximum on time hysteresis width	Tonmax_hys	Tonmax – Tonmax_ss	4	6	8	us
Maximum oscillating frequency1	Fmax1	V(COMP)=Vthcomp +0.1V	340	400	460	kHz
Maximum oscillating frequency2 *1	Fmax2	V(COMP)=Vthcomp+0.01V	450	530	610	kHz
RT output voltage	Vrt		0.90	1.15	1.40	V

PWM COMPARATER (COMP Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
COMP threshold voltage	Vthcomp	V(COMP) decrease	0.6	0.7	0.8	V

SOFT START (FB Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
End voltage of soft-start	Vthsoft	V(FB) increase Ton=Tonmax∗0.9	0.905 ∗Vfb	0.94 ∗Vfb	0.975 ∗Vfb	V

OVERVOLTAGE COMPARATER (FB Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Static OVP threshold voltage	Vsovph	V(FB) increase	1.060 ×Vfb	1.080 ×Vfb	1.095 ×Vfb	V
	Vsovpl	V(FB) decrease	1.020 ×Vfb	1.040 ×Vfb	1.060 ×Vfb	V
	Vsovphys	Vsovph-Vsovpl	0.030 ×Vfb	0.040 ×Vfb	0.060 ×Vfb	V
Dynamic OVP threshold voltage	Vdovp	V(FB) increase Ton=Tonmax∗0.7	1.025 ×Vfb	1.050 ×Vfb	1.075 ×Vfb	V

OVERVOLTAGE COMPARATER (OVP Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
OVP threshold voltage for stop switching at OUT pin	Vovph	V(OVP) increase, Switching at OUT pin stop	1.060 ×Vfb	1.080 ×Vfb	1.095 ×Vfb	V
	Vovpl	V(OVP) decrease, Switching at OUT pin start	1.020 ×Vfb	1.040 ×Vfb	1.060 ×Vfb	V
	Vovphys	Vovph - Vovpl	0.030 ×Vfb	0.040 ×Vfb	0.060 ×Vfb	V

FB SHORT COMPARATOR (FB Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input threshold voltage	Vthfbh	VFB(DC) increase, Switching at OUT pin start	0.10	0.30	0.50	V
	Vthfbl	VFB(DC) decrease, Switching at OUT pin start	0.10	0.20	0.50	V
	Vthfb_hys	Vthfbh - Vthfbl	0.02	0.05	0.10	V

CURRENT SENSE COMPARATOR (IS Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
IS threshold voltage	Vthis	V(IS) pulse : High = 100mV, Low decrease, dV/dT = ±40V/us	-0.62	-0.60	-0.58	V
IS threshold voltage temperature characteristics *1	Vthisdt	Tj = -30℃ to +85℃	-1.5	-	1.5	%
Output delay	Tphl	V(IS) pulse : High = 100mV, Low = -100mV, dV/dT = -40V/us, OUT open	30	200	500	ns
Zero current detection voltage	Vzcd	V(ZCD) increase	-15.0	-10.0	-5.0	mV
Zero current detection delay	Tzcd	V(IS) pulse : High = 100mV, Low = -100mV, dV/dT = +40V/us, OUT open,	0.3	0.9	1.5	us

Driver output (OUT Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage (L)	Vol	Isink=200mA	0.5	1.2	3.3	V
Output voltage (H) *1	Voh	Isouce=200mA	7.8	8.4	9.5	V
Output rise time	Tr	CL=1.0nF	20	50	120	ns
Output fall time	Tf	CL=1.0nF	10	25	100	ns

Restart timer

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Restart timer delay *1	Tdly	VFB(Pulse), High = 2.4V, Low = 0V, dV / dT = +40V / μs Switching at OUT pin start	10	30	50	μs

Under voltage lock out (VCC Pin)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Startup threshold voltage	Von	VCC increase	FA5695N	11.5	13	14	V
			FA5696N	8.6	9.6	10.6	V
Shutdown threshold voltage	Voff	VCC decrease		8	9	10	V
UVLO hysteresis width	Vhysvcc	Von – Voff	FA5695N	3.0	4.0	5.0	V
			FA5696N	0.3	0.6	0.9	V

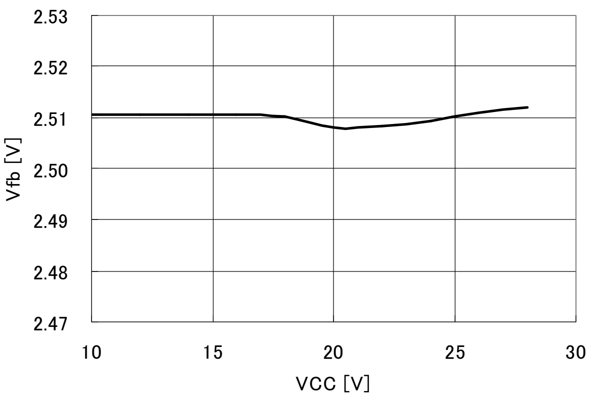
Power supply current (VCC Pin)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Startup power supply current	Istart	VCC = Von-0.1V	1	-	80	μA
Operating power supply current	Icc	Vcc=12V, CL=OPEN	0.3	1.5	3.0	mA
Dynamic operating power supply current	Iop	CL=1.0nF	0.5	2.0	4.0	mA
Stand-by current	Istb	V(FB)=0V, V(COMP)=0V	3	30	60	uA

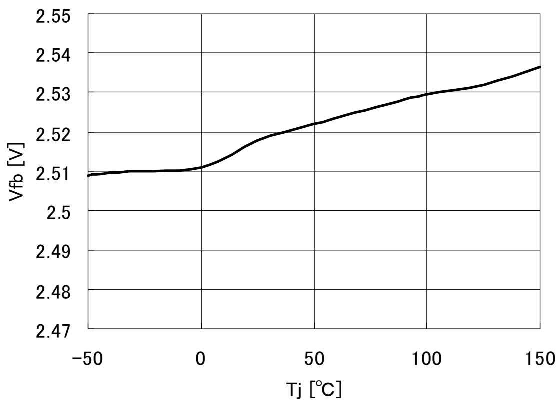
8. Characteristic curve

The characteristics in this section are those in conditions as follows unless otherwise specified.
Tj=25℃, VCC=12V, V(FB)=1.0V, V(COMP)=5V, V(IS)=100mV, OUT open, Rrt=82KΩ
Notes)
(1) ”-” shows source current and “+” shows sink current.
(2) The data listed here show the typical characteristics of an IC and it does not guarantee the characteristic.

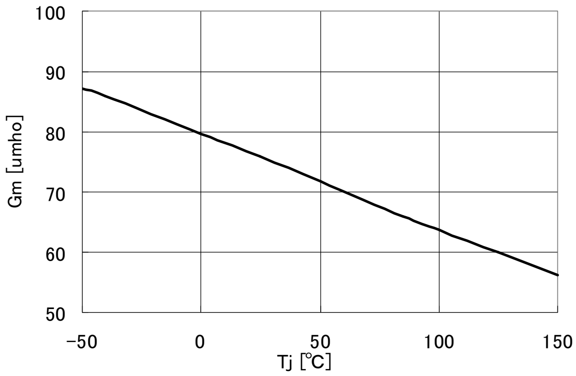
Error amplifier voltage feedback input threshold(Vfb) vs. supply voltage(Vcc)



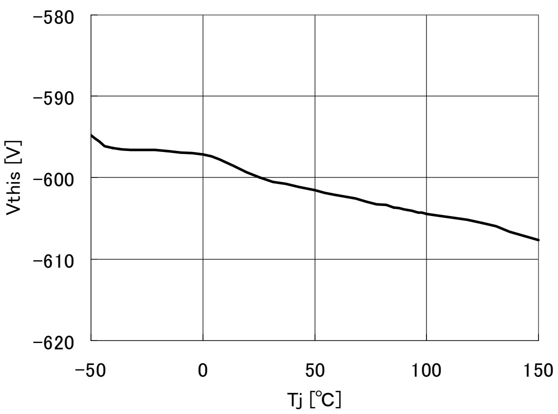
Error amplifier voltage feedback input threshold(Vfb) vs. junction temperature(Tj)



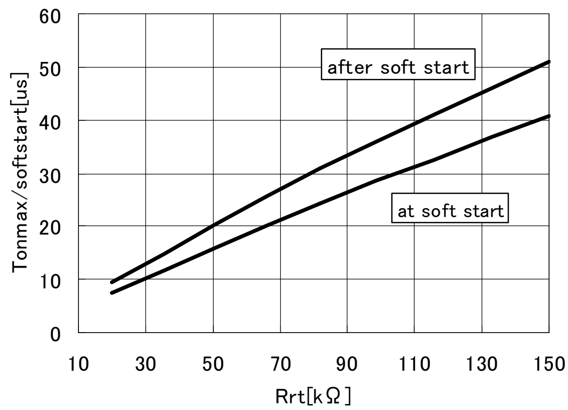
Error amplifier transconductance(Gm) vs. junction temperature(Tj)



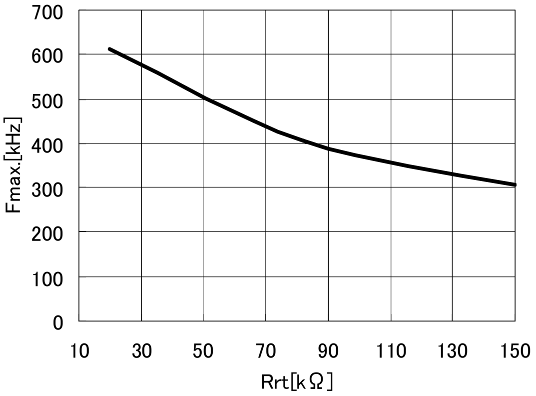
Current sense comparator maximum threshold(Vthis) vs. supply voltage(Vcc)



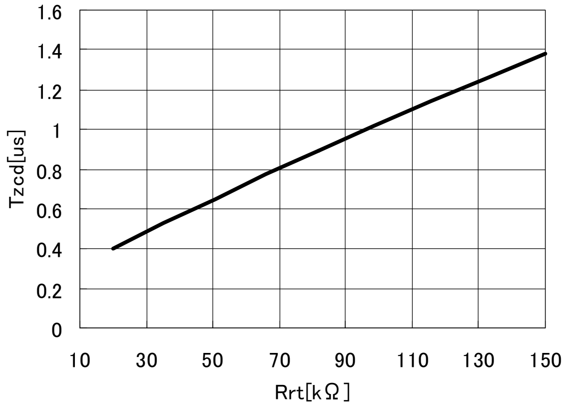
Maximum on-range(Tonmax) vs. RT resistance(Rrt)



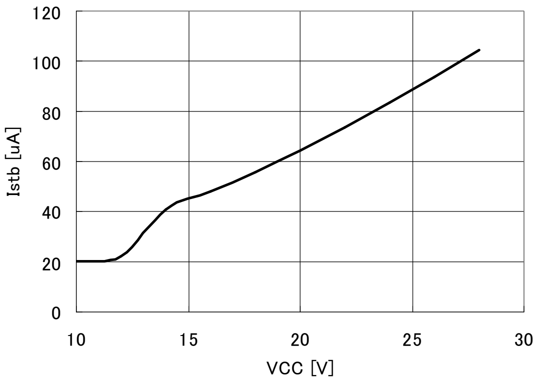
Maximum oscillating frequency(Fmax) vs.
RT resistance(Rrt)



Zero current detection delay(Tzcd) vs.
RT resistance(Rrt)



Standby current(Istb) vs.
supply voltage(Vcc)



9. Outline of circuit operation

This IC is a power-factor correction converter utilizing a boosting chopper, operating in critical mode. Hereinafter is outline of the operation consisting of switching operation and power-factor correction operation using the circuit diagram shown in Fig. 1.

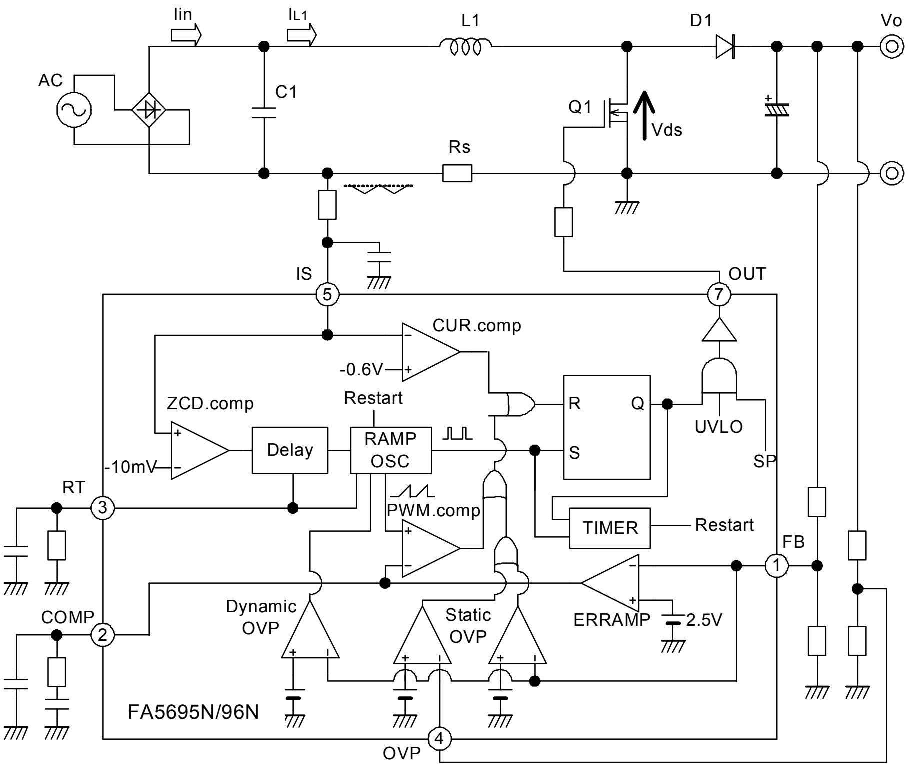


Fig.1 Block diagram of operating circuit

(1) Switching operation

This IC performs the switching operation in the critical mode applying self-oscillation without using an oscillator. Fig.2 shows the outline of waveforms of the switching operation in steady state. The operation is as follows.

【t1】Q1 turns on, the current through inductor (L1) rises from zero. At the timing of Q1 on, Vramp; output of ramp generator states to rise.

【t2】Vramp and Vcomp; output of the error amplifier are compared by the PWM comparator, and when Vramp>Vcomp, Q1 turns off and the output of the ramp generator drops.
When Q1 turns off, the voltage across L1 inverts and the current through L1 decreases while the current is supplied to the output side through D1.

【t3】The current through L1 is detected by IS pin, and when the current becomes zero, the output of the current detection comparator becomes High to turn on Q1 after delay given by the delay circuit, thus moving to the next switching cycle (t1).

By repeating the operations of t1 ~ t3, the switching in critical mode is continued.

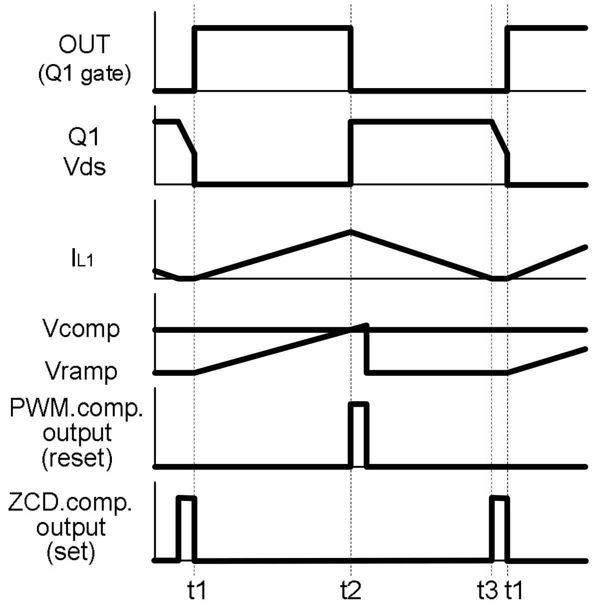


Fig. 2 Switching Operation, Waveforms

With the power-factor correction circuit in the critical mode, the switching frequency is always changing due to instantaneous values of the AC input voltage. The switching frequency also changes when the input voltage or load changes.

(2)Power-factor correction operation

As explained in the switching operation, the current flowing through the inductor repeats in triangular waveforms.
The mean value (IL1(mean)) of the triangular wave current becomes 1/2 of the peak value (IL1(peak)). (Fig. 3)

By controlling to make outline linking the peak of the inductor current to sine wave and removing switching ripple current, the smoothed current flowing from the AC input power source has sine wave shape.

FA5695 / FA5696 uses fixed on time control shown in Fig. 4. This control determines the on time of the output of IC (gate drive signal for Power Mos) with combination of the error amplifier output and saw tooth wave. While the load is constant, the output of the error amplifier is constant, and on time also stays constant. Since an inclination of inductor current depends on input voltage (an inclination of inductor current is proportional to input voltage) and on time is constant, the outline linking the peak of the inductor current becomes same AC waveform as the input voltage, which enables power-factor correction operation.

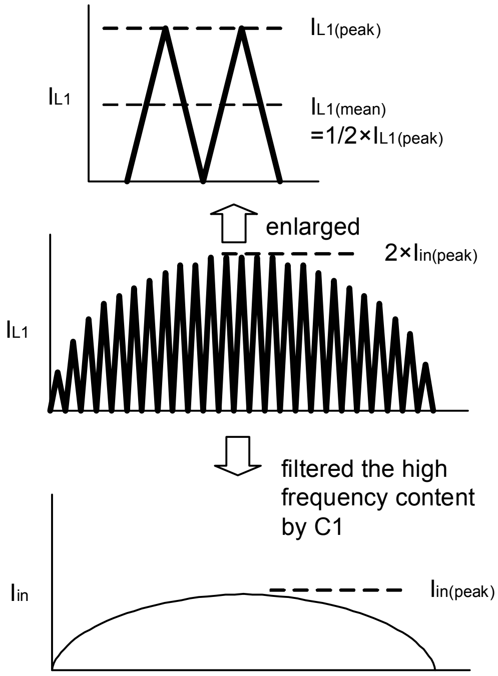


Fig.3：Power-factor correction operation waveforms

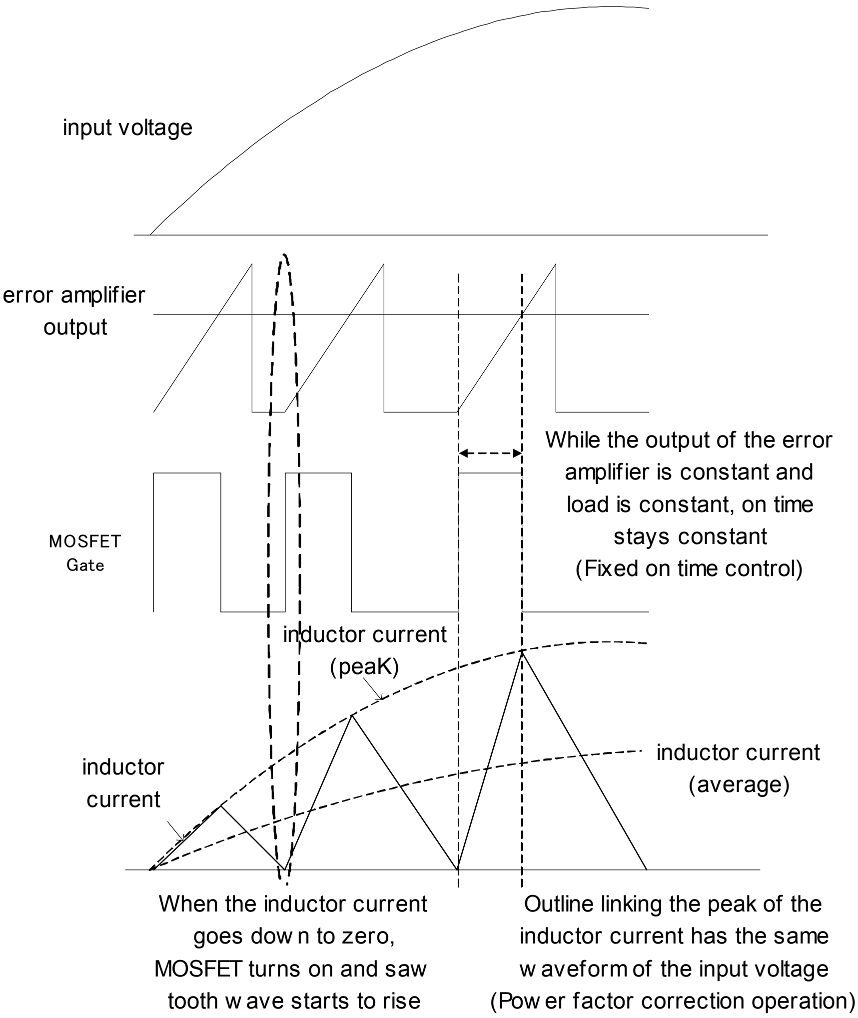


Fig.4：Fixed on time control

10. Description of each circuit block

(1) Error amplifier circuit

The error amplifier is to make the output voltage constant with feedback control. For this IC, a transconductance type is used for the error amplifier.
The non-inverting input pin is connected to internal reference voltage of 2.5V (typ.).
The inverting input pin is fed with output voltage of the power-factor correction converter, and normally use divided voltage with resistors. To the inverting input, internal constant current source of 1.8μA is connected for FB open detection function.
The output of the error amplifier (COMP) is connected to the PWM comparator and controls the on time of the OUT output.
The output voltage of PFC contains much of ripple of frequency 2 times AC power line (50 or 60Hz). When this ripple component becomes largely appears in the output of the error amplifier, the power-factor correction converter does not stably operate. In order to obtain the stable operation, connect capacitors and a resistor between pin No.2 (COMP pin) and GND as shown in Fig.5.

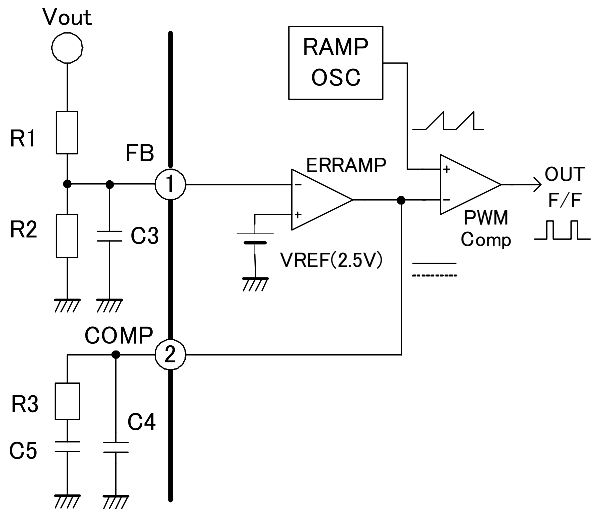


Fig.5 Error amplifier circuit

(2)Soft start circuit

FA5695N/96N is equipped with soft start function to suppress rushing startup and overshoot of output voltage when starting.
The soft start circuit works after UVLO and standby is released and before the soft start cancellation voltage is exceeded. In the meantime, the soft start function restricts the startup speed of the output voltage by limiting the maximum on time to about 80% when the FB pin voltage is lower than the reference voltage. (Fig. 6) The on time limited by the soft start is cancelled when the FB pin voltage becomes higher than the soft start cancellation voltage.

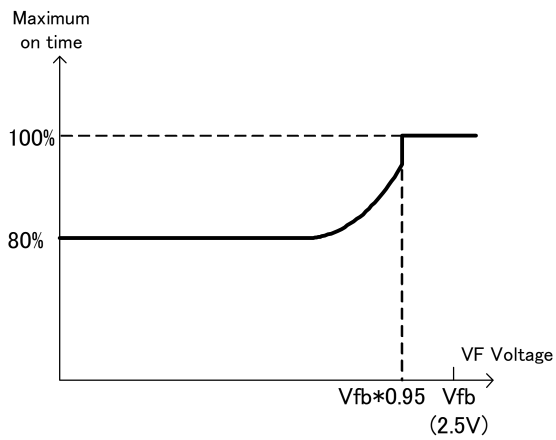


Fig.6 Maximum on time at soft start

(2) Overvoltage protection circuit (OVP)

This circuit is to limit the voltage when the output voltage of the power-factor correction converter exceeds the set value.
When this IC starts up or load changes sharply, the output voltage of the converter may exceed the set value. In such a case, this protection circuit works to control the output voltage.
FA5695/96 has 2 of OVP function as shown below.

It controls the ON width linearly when the output exceeds the reference voltage.
Dynamic OVP - - - Built-in FB pin

It stops the output pulse when the output exceeds 1.08 times of reference voltage.
Static OVP - - - Built-in FB pin and OVP pin

The operation of FB pin which has two functions above is described below.
FB pin voltage is usually 2.5V as same as the reference voltage. When the startup or a sudden change of load, FB pin voltage rises and will exceed 2.5V. In this case, a function which limits ON width depending on FB pin voltage becomes active. (Dynamic OVP) If FB pin voltage rises more and exceeds a reference voltage of comparator (Vfb*1.08), another function becomes active and stops the output pulse during exceeding the reference. (Fig.7)
When FB pin voltage decreases to 1.040 times of reference voltage or lower, IC outputs pulses again.

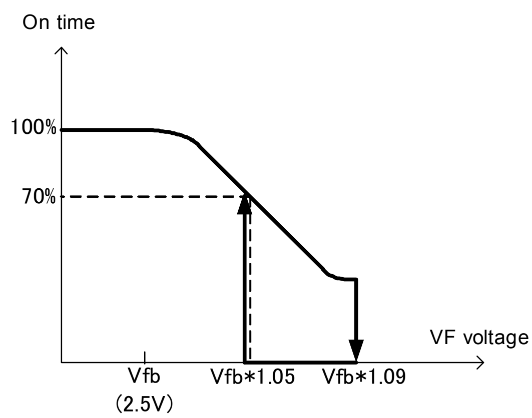


Fig.7 On time at overvoltage

(4) FB short-circuit/open detection circuit (standby circuit)

In the PFC circuit of booster type, if feedback voltage is not properly provided to the FB pin due to short-circuit or open-circuit around R1, R2, the error amplifier cannot control the constant voltage and the output voltage abnormally rises. In such a case, the overvoltage protection circuit also cannot operate because the detection of the output voltage is abnormal.
To avoid such situation, this IC is equipped with FB short-circuit detection circuit.
This circuit is composed of the reference voltage of 0.3V (typ.) and comparator (SP), and when the input voltage of the FB pin becomes 0.3V or lower due to such trouble as short-circuit of R2 or opening of R1, the output of the comparator (SP) inverts to stop the output of the IC and the IC stops operation resulting in standby state.
Once the voltage of the FB pin decreases to almost zero and the output of the IC stops, and then when the voltage of the FB pin returns to 0.3V or higher, the IC resumes from the standby state and the OUT pulse restarts.

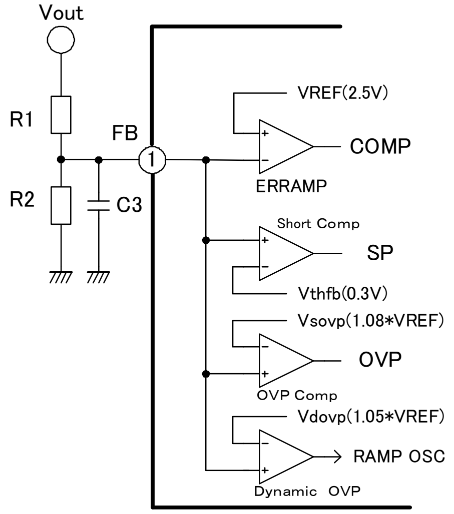


Fig.8 FB pin circuit

(5) Ramp oscillating circuit

The ramp oscillating circuit receives signal from the zero current detection circuit or restart circuit, and outputs the set signal of F/F for OUT output and saw tooth wave signal for deciding the duty of the PWM comparator.

(5-1) Maximum frequency limiting

The switching frequency of PFC in the critical mode has characteristic to rise at light load.
FA5695N/96N has the maximum frequency limiting function to improve the efficiency at light load and limits the switching frequency to Fmax (Hz). (Fig. 9)
The maximum frequency Fmax depends on the resistance connected between the RT pin and GND.
When the switching frequency is lower than Fmax, the zero level of the inductor current is detected and MOSFET is turned on after the zero current detection delay Tzcd to adjust turning on take place at the bottom of Vds wave, as shown in Fig. 11.
In case of light load where the switching frequency is limited to Fmax, the zero level of the inductor current is detected and no turn-on occurs after the zero current detection delay, but turn-on occurs at the cycle of 1/Fmax, as shown in Fig. 12.

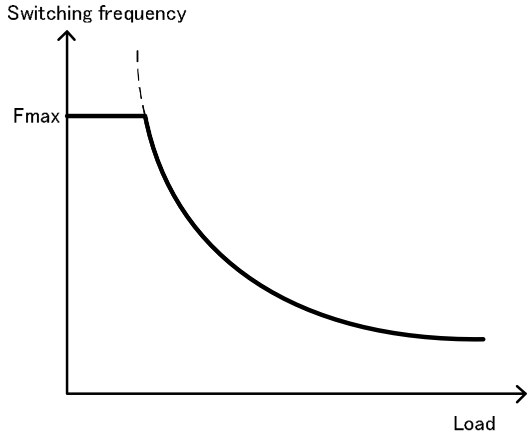


Fig.9 maximum frequency limiting

(6) Current detection circuit

The current detection circuit is composed of zero current detection and overcurrent detection. (Fig. 10)

(6-1) Zero current detection circuit

This IC performs the switching operation by self-oscillation in critical mode instead of the oscillator with the fixed frequency. The zero current detection circuit ZCD. Comp detects that the inductor current becomes zero to perform the critical mode operation.
With the zero current detection, the voltage across the current detection resistor Rs connected to the GND line is fed to the IS pin, and it is compared by the zero current detection comparator, and when it becomes -4mV or more, the inductor current is regarded as zero level.
When the zero level is detected, the delay Tzcd is generated by the zero cross delay detection circuit, and then set the F/F for OUT to make MOSFET turn on.

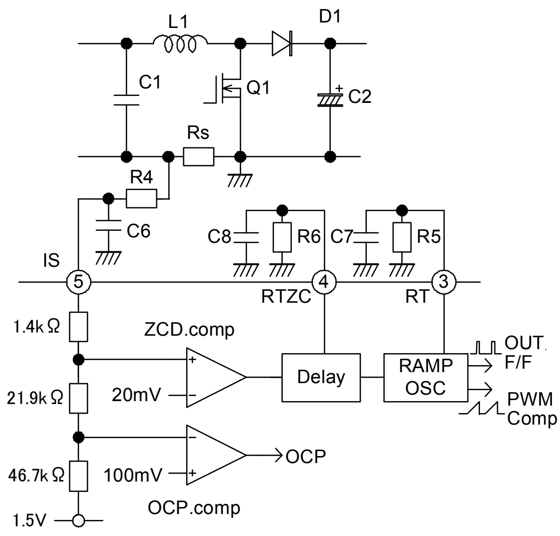


Fig.10 Current detection circuit

(6-2) Overcurrent detection protective circuit

The overcurrent detection protective circuit detects the inductor current and protects MOSFET by turning off the OUT output when it becomes higher than a set current level. With the overcurrent detection, the voltage across the current detection resistance Rs connected to the GND is fed to the IS pin, and when the IS pin voltage compared by the overcurrent detection comparator becomes lower than -0.6V, it is regarded as overcurrent state.
When the overcurrent is detected, the F/F for OUT output is reset to make MOSFET turn off.

(7) Zero cross delay time setting circuit

Vds between the drain and the sources of the MOSFET starts oscillating through resonance of L1 and the parasitic capacitor component on the circuit just before the MOSFET turns on.
When the proper value of Rt, the turn on timing of MOSFET can be adjusted at the bottom of the voltage oscillation. This makes it possible to minimize the switching loss and the surge current generated at the turn-on. (Fig. 13)
When the Rt is smaller, the turn-on timing becomes earlier, and vice versa. (Fig. 14)
Since the optimum value of this Rt changes depending on the circuit and input/output conditions, tuning up is required so as to achieve an optimum state while evaluating the operation with actual circuit.

(8) Restart timer

This IC utilizes self oscillation instead of the oscillator with fixed frequency, and in the steady operation, it turns on MOSFET with a signal from the zero current detector.
But in start up or light load condition, a trigger signal is required for starting up or stable operation.
This IC is provided with a restart timer, and when the output of IC continues turn off for 20µs or more, the trigger signal is automatically generated.
This signal can realize stable operation even when starting up or the load is light.

(9) Under Voltage Lock out (UVLO)

UVLO is equipped to prevent circuit malfunction when supply voltage drops.
When the supply voltage rises from zero, the operation starts at 13V (typ.) for FA5695 and 9.6V (typ.) for FA5696.
When the supply voltage decreases after the operation starts, either part number stops the operation at 9V (typ.).
When UVLO is on and IC stops operation the OUT pin becomes LOW and cuts off the output. The current consumption of the IC decreases to 80µA or less.

(10) Output circuit

The output portion is of push-pull circuit and can directly drive the MOSFET. The peak current of the output portion is 1.0A maximum for sink and 1.0A maximum for source.

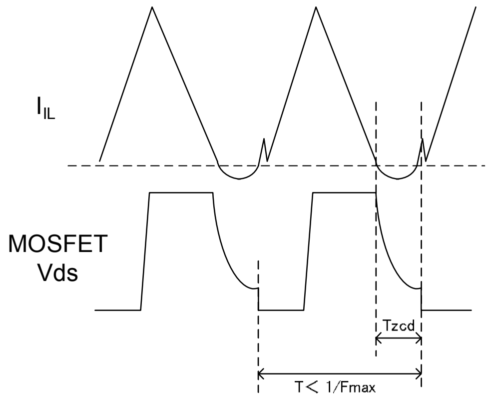


Fig.11 Waveforms when the switching frequency is lower than the maximum frequency Fmax

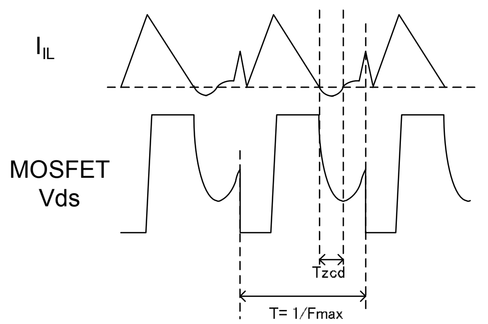


Fig.12 Waveforms when the switching frequency is limited to the maximum frequency Fmax

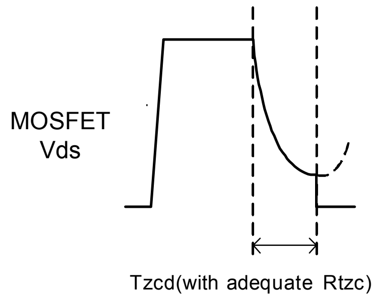


Fig.13 Vds waveform at turn on (with adequate Rtzc)

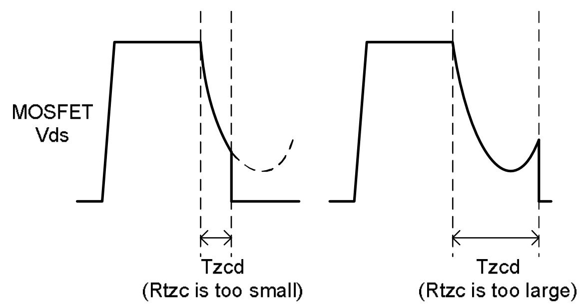


Fig.14 Vds waveform at turn on (with inadequate Rtzc)

11. How to use each pin and advice for designing

(1) Pin No.1 (FB pin)

Functions

(i) Input of feedback signal of output voltage setting
(ii) Detect short-circuit of FB pin
(iii) Detect output overvoltage

How to use

(i) Feedback signal input
- Connection method
  Connect the node between voltage dividing resistors for setting output voltage.
- Operation
  The output voltage Vout of PFC is controlled so that FB voltage matches the internal reference voltage (2.5V).

$$Vout = \frac{VREF}{R2} \times R1 + VREF$$

VREF : Reference voltage =2.5V(typ)

To prevent malfunction due to noise, capacitor C3 of 100pF to 3300pF should be connected between the FB pin and GND.

(ii) FB pin short-circuit detection
- Connection method
  Same as for the (i) Feedback signal input
- Operation
  When the input voltage of the FB pin becomes 0.3V or lower due to short-circuit of R2, the output of the comparator (SP) inverts to stop the output of the IC.

(iii) Output overvoltage detection
- Connection method
  Same as for the (i) Feedback signal input
- Operation
  Normally the voltage of the FB pin is 2.5V almost same as the reference voltage of the error amplifier. When the output voltage rises for some reason and the voltage of the FB pin reaches the comparator reference voltage (1.08*VREF), the output of the comparator (OVP) inverts to stop the OUT pulse. If the output voltage returns to the normal value, the OUT pulse resumes.

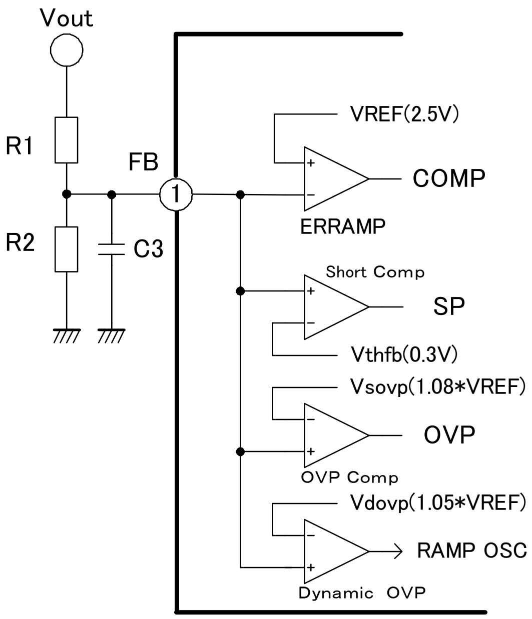


Fig.15 FB pin circuit

(2) Pin No.2 (COMP pin)

Functions

(i) Phase compensation of internal ERRAMP output

How to use

(i) Phase compensation of internal ERRAMP output
- Connection method
  Connect C, R between COMP pin and GND as shown in Fig. 16.

- Operation
  Connecting C, R to the COMP pin suppress ripple component at 2 times the frequency of the AC line that appears in the FB output.

(Reference)
Example of application circuit: C4=0.15uF
C5=0.15uF
R3=68kΩ

The above is a reference example, and it should be decided by sufficiently verifying with actual application circuit.

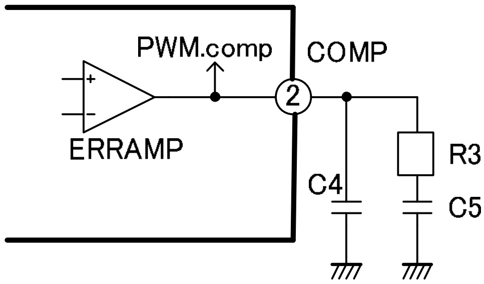


Fig.16 COMP pin circuit

(3) Pin No.3 (RT pin)

Functions

(i) Set maximum on time
(ii) Set maximum oscillation frequency
(iii) Set delay time for zero current detection

How to use

(i) Set maximum on time

In the PFC circuit of booster type, on time Ton in each switching cycle with input and output conditions is theoretically expressed by the following formula.

$$Ton = \frac{2 \times Lp \times Po}{Vac^2 \times \eta}$$

Input Voltage (Vrms) : Vac
Inductor (H) : Lp
Maximum Output Power (W) : Po
Efficiency : η

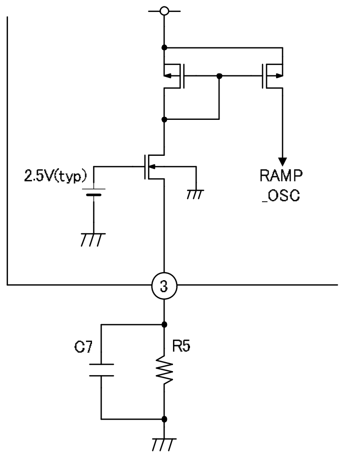


Fig.17 RT pin circuit

The maximum on time Tonmax must be set equal to or more than the on time at minimum input voltage Vac (min) at which the on time is maximum. In soft start, the maximum on time is limited to 80%, and therefore, the maximum on time should be set as shown by the following formula.

$$Tonmax > \frac{2 \times Lp \times Po}{Vac(min)^2 \times \eta \times 0.8}$$

(ii) Set maximum oscillation frequency

To improve the efficiency at light load, FA5695N/96N limits switching frequency at light load to Fmax(Hz). The maximum frequency Fmax depends on the resistance connected between RT pin and GND.

- Connection method

Connect R5 between RT pin and GND as shown in Fig. 17.
For the resistance dependency of the maximum on time and maximum oscillation frequency, see Chapter 8. Characteristic Curve.
The current sourced from the RT pin changes depending on the resistance connected. When R5 is relatively large, for example, 82kΩ, the current is about 10uA. When the current is relatively small, it is recommended to connect a capacitor of about 0.01μF in parallel to the resistor to stabilize the RT voltage, as shown in Fig. 17.

(4) Pin No.4 (OVP pin)

Functions

(i)Set detection level of OVP

It sets a voltage which detects an over voltage of output and which stop switching operation.
For avoiding malfunction by noise, the recommended resistance of the detection circuit is 10Mohm or smaller.

$$R8 = \frac{Vstop \times R9}{Vref(ovp) \times 1.095}$$

Vstop: Overvoltage detection voltage,
Vref: OVP Reference voltage =2.5V)
1.095: Vovp Max(1.095xVref)

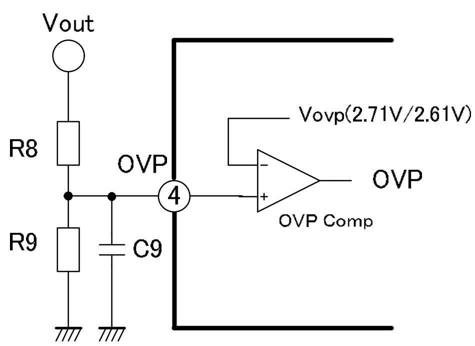


Fig.18 OVP pin circuit

(5) Pin No.5 (IS pin)

Functions

(i) Detect zero current through the inductor
(ii) Detect overcurrent and turn off OUT output

How to use

The maximum threshold voltage Vthcsh of the IS pin is -0.58V(max).
The current detection resistance Rs is set so that necessary current can be supplied for this Vthcsh.
With maximum output Po (W) and minimum input voltage Vac (min), the maximum value of peak current (ILP (max)) through the inductor can be approximately expressed by the following formula.

$$I_{LP(max)} = \frac{2\times\sqrt{2}\times Po}{\eta\times Vac_{(min)}}$$

Therefore, the value of Rs (Ω) is determined as follows.

$$Rs < \frac{-V_{thIS}}{I_{LP(max)}} = \frac{0.58}{I_{LP(max)}}$$

- Connection method

Connect the current detection resistor Rs between the source pin (GND) of MOSFET and the minus lead of the input capacitor (C1). The voltage across Rs is fed to the IC as the current/voltage conversion signal.(Fig.19)

- Operation

(i) Detect zero current through the inductor

The internal reference voltage and the internally divided voltage of the IS pin are inputted to the ZCD comparator, and when the IS pin voltage becomes larger than -10mV, the comparator output inverts and turns on the OUT output.

(ii) Detect overcurrent and turn off OUT output

When the IS pin voltage becomes smaller than -0.6V, the comparator output signal inverts and turns off the OUT output.

【Additional explanation】

When MOSFET turns on, the gate driving current of MOSFET and surge current due to discharging the parasitic capacitors run to the current detection resistance Rs. Large surge current may cause malfunction following disturbed input current waveform. Depending on the amperage of the surge current or timing, whisker-like pulse may be mixed in the turn-on portion of the OUT pulse of the IC. Normally, therefore, a CR filter is connected as shown in Fig.19. The cutoff frequency of this CR filter must be set sufficiently higher than the switching frequency so that it will not affect the normal operation.
It is recommended to set this cutoff frequency to about 1 to 2 MHz.

$$\frac{1}{2\times\pi\times C6\times R4} \fallingdotseq 1\text{ to }2\ [\text{MHz}]$$

Since the threshold level is made through resistance dividing voltage as shown in Fig.19, the input resistor R4 is recommended to be not higher than 100Ω.The voltage rating of the IS pin is -5V.

In case of an ordinary boosting circuit, rush current to charge the output smoothing capacitor C2 runs at the moment the ac input voltage is connected. This current may become far larger in comparison with the input current during normal operation. As a result, far larger voltage may also be applied to the IS pin than the ordinary case.

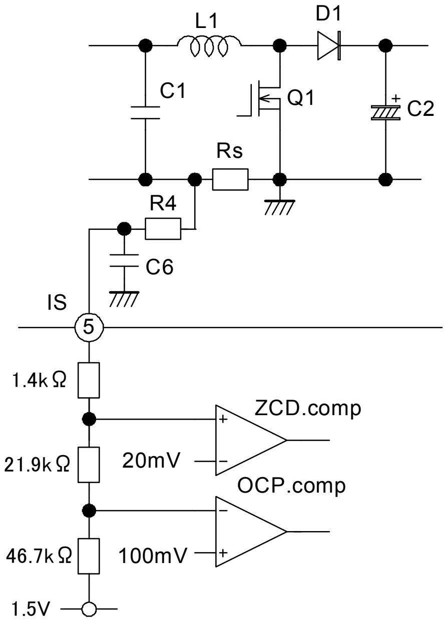


Fig.19 IS pin circuit

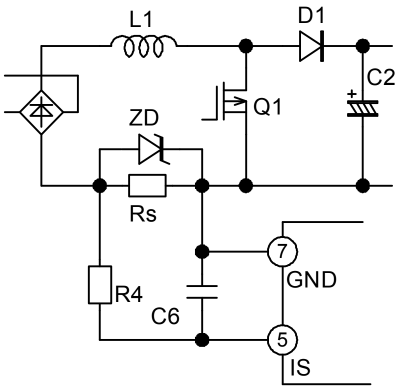


Fig.20 IS pin protection circuit (1)

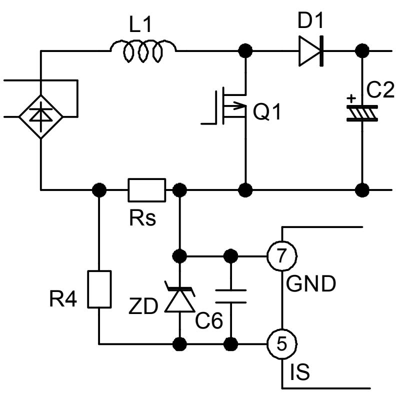


Fig.21 IS pin protection circuit (2)

In order to avoid damage, protective circuit must be taken in design so that voltage higher than -5V, absolute maximum rating, will not be applied to the IS pin even when such AC input voltage is connected. If voltage higher than the rating is predicted to be applied to the IS pin, use rush preventive circuit suppress rushing current or place Zener diode shown in Fig. 20 and Fig. 21.

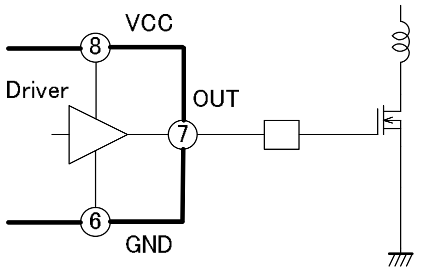


Fig.22 OUT pin circuit (1)

(6) Pin No.6 (GND pin)

Function

This voltage of GND pin is the reference for each portion of whole circuits.

(7) Pin No.7 (OUTpin)

Function

This drives MOSFET.

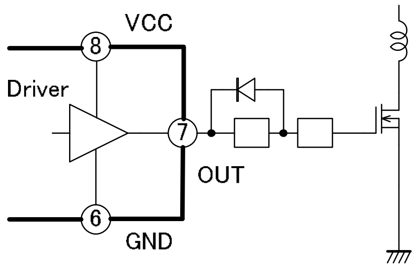


Fig.23 OUT pin circuit (2)

How to use

- Connection method

Connect it to the gate terminal of MOSFET through resistance.(Fig.22)

- Operation

During the period when turn on MOSFET, the output state is high, and the output voltage is almost VCC.
During the period when turn off MOSFET, the output state is low, and the output voltage is almost 0V.

- Additional explanation

The gate resistor is connected to limit the current of the OUT pin and prevent oscillation of the gate terminal voltage. The rating of the output current is 0.5A for source and 1A for sink.
Using the connections shown in Fig.23 and Fig.24, it is possible to independently set the gate driving current of turning on and off MOSFET.

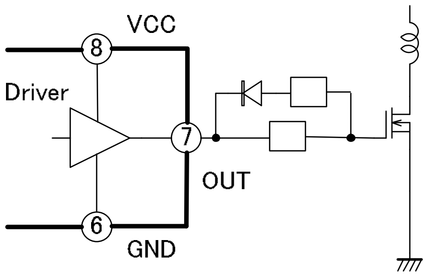


Fig.24 OUT pin circuit (3)

(8) Pin No. 8 (VCC pin)

Function

(i) Supply the power of IC.

How to use

(i) Supply the power of IC.

- Connection method

Connect the start up resistor R7 between VCC pin and Voltage line after rectifying from AC line, which supplies power before IC starts switching operation.
In general application, the power is provided from the auxiliary winding of the transformer through D2 during operation.
In some application, DC power supply can be connected.

- Operation

In the application with out DC power supply to feed VCC pin, the current through start up resistor R7 charges the smoothing capacitors C5 and C9, and when VCC voltage rises to the on threshold voltage of UVLO, the IC starts operating. Before starting operation, it is necessary to supply current higher than 80uA (max), the startup current of the IC. During steady operation, the VCC is supplied from the auxiliary winding of the inductor. (Fig. 27)

When the supply voltage rises from zero, the operation starts at 13V (typ.) for FA5695 and 9.6V (typ.) for FA5696.
If the supply voltage decreases after the operation starts, the operation stops at 9V (typ.) by UVLO for both ICs. After IC stops operation due to UVLO, the OUT pin is Low state to cut off the output.

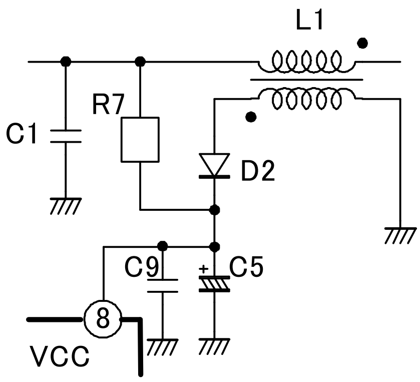


Fig.25 VCC pin circuit (1)

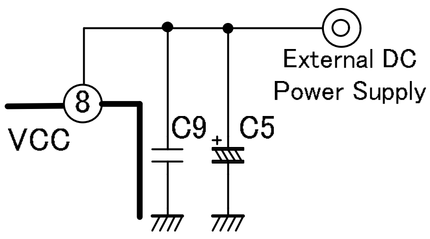


Fig.26 VCC pin circuit (2)

- Additional explanation

UVLO is preventive function to keep the circuit from malfunction when the supply voltage decreases.

With the start up resistor R7, it is necessary to supply current of 80μA or higher, the startup current, until start operating, and the following formula must be satisfied.

$$R7 < \frac{\sqrt{2} \times Vac(min) - Von(max)}{80 \times 10^{-6}}$$

Von(max): Low voltage ON threshold voltage of UVLO
FA5695 14V(max)
FA5696 10.6V(max)

The value of R7 expressed with the formula is, however, at least necessary and minimum condition to start the IC, and actually it should be decided considering the starting up time required for each application circuit.

This starting up time must be examined by measuring in actual circuit operation.

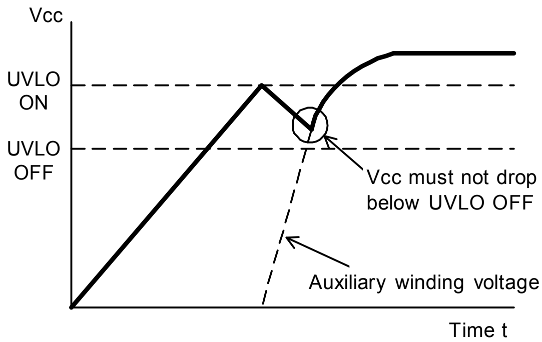


Fig.27 Vcc voltage at startup

During the steady operation, Vcc is supplied from the auxiliary winding of the transformer. But there is some time delay until the auxiliary winding voltage sufficiently rises after the IC starts switching operation. To prevent Vcc from decreasing to the off threshold voltage of UVLO, it is necessary to decide the capacitance of the C5 connected to Vcc. Since this time delay differs depending on the circuit, it should be decided after checking with actual circuit

It is also recommended to place the ceramic capacitor C9 (about 0.1uF) to remove switching noise.

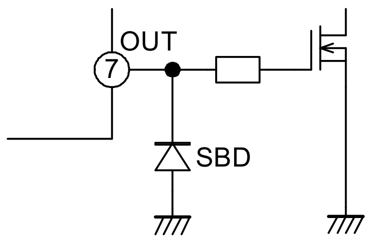


Fig.28 Protection circuit of OUT pin against the negative voltage

(9) Minus voltage of each pin

In some cases, the voltage oscillation of Vds just before MOSFET turns on is applied to the OUT pin through parasitic capacitors, etc. and minus voltage may be added to the OUT pin. If this minus voltage is large, the parasitic element inside the IC is activated, and the IC may malfunction.

If this minus voltage is expected to exceed -0.3V, Schottky barrier diode should be connected between the OUT pin and GND. With the forward voltage of the Schottky barrier diode, the minus voltage can be clamped.

For other pins as well, care should be taken so that minus voltage will not be applied in the same way.

12. Advice for design

(1) Advice in pattern designing

Main circuit MOSFET, inductor, diodes, etc. perform switching under high voltage and large current. If wiring of IC or signals inputted to IC gets too near such main circuit parts, they may operate erratically upon being affected by noise generated there.

Attention must be paid particularly in following cases (examples of faulty cases).

・IC is arranged under inductor or other main circuit parts, or immediately behind main circuit parts on double sided circuit board (Fig. 29)

・IC is arranged close to inductor, MOSFET or diode (Fig. 30)

・Signal wiring is placed under inductor or near MOSFET or diode (Fig. 31)

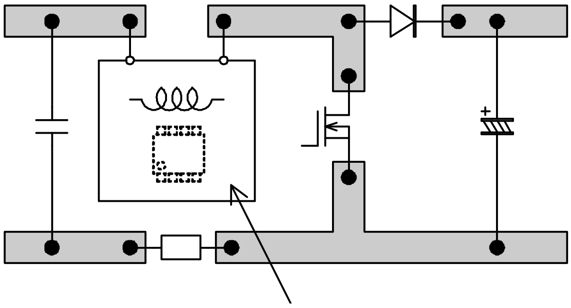


Fig.29 Bad example (1)

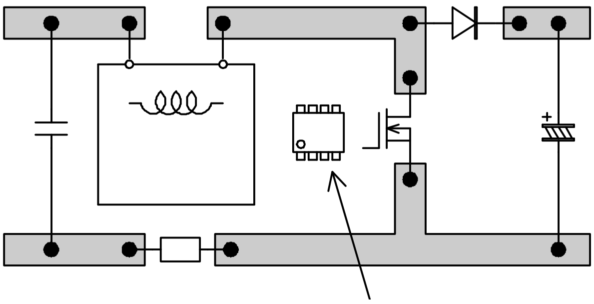


Fig.30 Bad example (2)

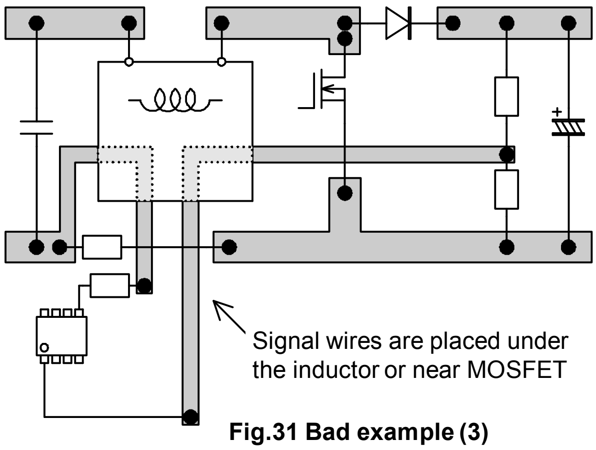


Fig.31 Bad example (3)

(2)Example of GND wiring around IC

Notes)

Wiring is exemplified for you to understand how to connect the GND line.
Noise and incidental erratic operations differ from one instrument to another. Adopting any wiring exemplified in Fig. 32 will not necessarily guarantee normal operations of your instruments.

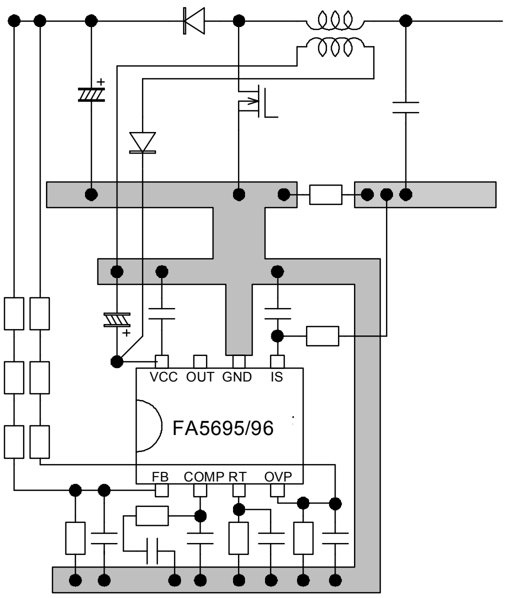


Fig.32 Good example of GND wiring around IC

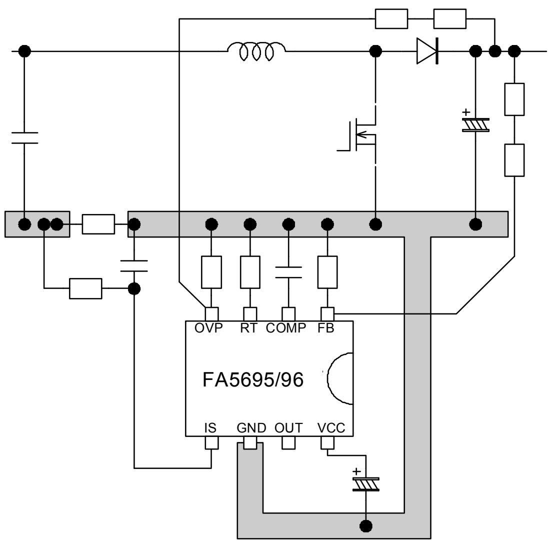
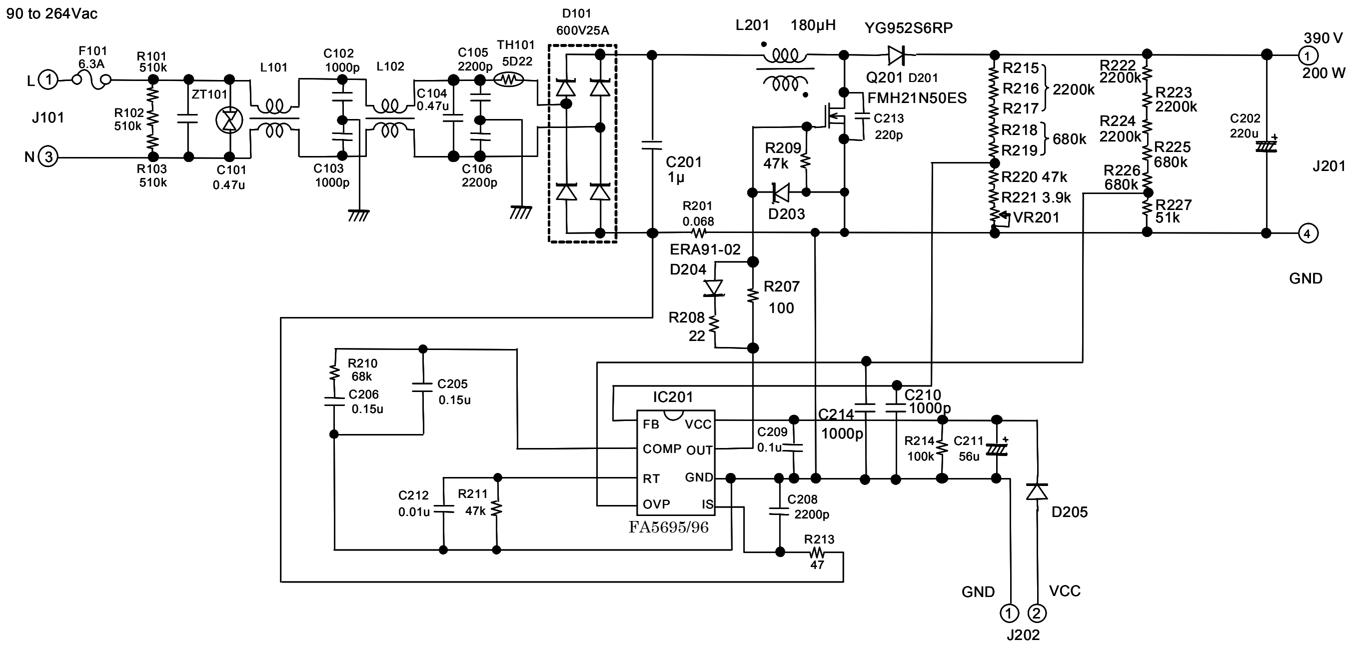


Fig.33 Bad example of GND wiring around IC
(GND is common to signal line parts and main circuit)

13. Example of application circuit (390V / 0.5A output)



Note) This application circuit is a reference material for describing typical usage of this IC,
and does not guarantee the operation or characteristics of the IC.

Notice

1. The contents of this note (Product Specification, Characteristics, Data, Materials, and Structure etc.) were prepared in Sep 2016.The contents will subject to change without notice due to product specification change or some other reasons. In case of using the products stated in this document, the latest product specification shall be provided and the data shall be checked.

2. The application examples in this note show the typical examples of using Fuji products and this note shall neither assure to enforce the industrial property including some other rights nor grant the license.

3. Fuji Electric Co.,Ltd. is always enhancing the product quality and reliability. However, semiconductor products may get out of order in a certain probability.Measures for ensuring safety, such as redundant design, spreading fire protection design, malfunction protection design shall be taken, so that Fuji Electric semiconductor product may not cause physical injury, property damage by fire and social damage as a result.

4. Products described in this note are manufactured and intended to be used in the following electronic devices and electric devices in which ordinary reliability is required:
   - Computer - OA equipment - Communication equipment (Pin) - Measuring equipment
   - Machine tool - Audio Visual equipment - Home appliance - Personal equipment
   - Industrial robot etc.

5. Customers who are going to use our products in the following high reliable equipments shall contact us surely and obtain our consent in advance. In case when our products are used in the following equipment, suitable measures for keeping safety such as a back-up-system for malfunction of the equipment shall be taken even if Fuji Electric semiconductor products break down:
   - Transportation equipment (in-vehicle, in-ship, railways, etc.) - Communication equipment for trunk line
   - Traffic signal equipment - Gas leak detector and gas shutoff equipment
   - Disaster prevention/Security equipment - Various equipment for the safety.

6. Products described in this note shall not be used in the following equipments that require extremely high reliability:
   - Space equipment - Aircraft equipment - Atomic energy control equipment
   - Undersea communication equipment - Medical equipment.

7. When reprinting or copying all or a part of this note, our company’s acceptance in writing shall be obtained.

8. If obscure parts are found in the contents of this note, contact Fuji Electric Co.,Ltd. or a sales agent before using our products. Fuji Electric Co.,Ltd. and its sales agents shall not be liable for any damage that is caused by a customer who does not follow the instructions in this cautionary statement.

- The contents will subject to change without notice due to product specification change etc.
- Application examples and component in this sheet is for the purpose of assisting in the design. Therefore, This sheet has not been made in consideration of the margin.
- Before using, Please design in consideration of the parts variation and use condition.