Critical Conduction Mode PFC IC
FA5601N

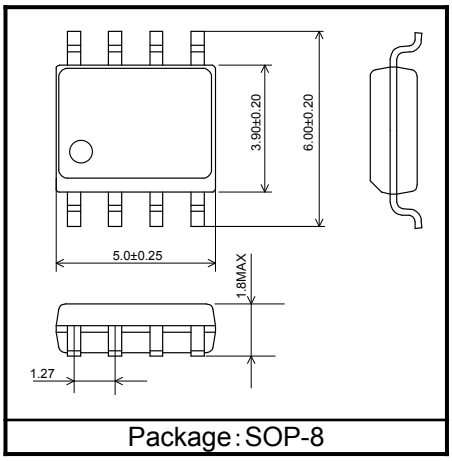
Datasheet

1. Overview

FA5601 is power-factor correction converter IC operating in critical conduction mode. It realizes low power consumption by using high voltage CMOS process. It is equipped with many fault protection functions such as FB short-circuit detection circuit which stops the operation when abnormal output voltage is detected.

2. Features

- Very Low Standby Power by disusing Input Voltage Detection Resistors
- High-precision over current protection: 0.65V±5%
- Improved power efficiency at light load due to Maximum Frequency Limitation
- No Audible Noise at Startup by dynamic OVP circuit
- Low current consumption by CMOS process
  Start-up : 80μA(max.), Operating : 2mA(typ.)
- Enabled to drive power MOSFET directly
  Output peak current, source : 0.5A, sink : 1A
- Open/short protection at feedback (FB) pin
- Under-voltage Lockout
  FA5601: 13V ON / 9V OFF
- Restart timer
- Standby function
- 8-pin package: SOP-8

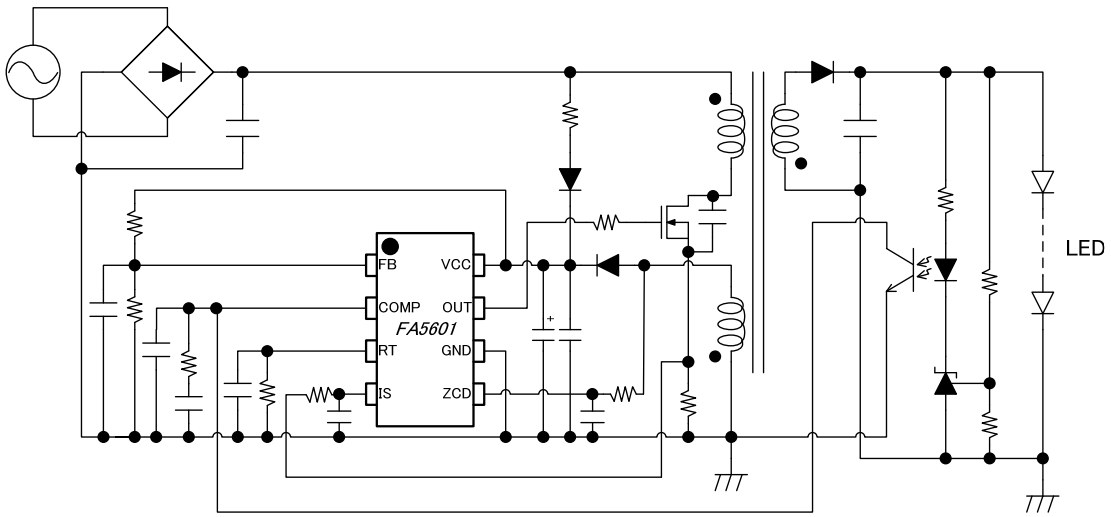


Package : SOP-8

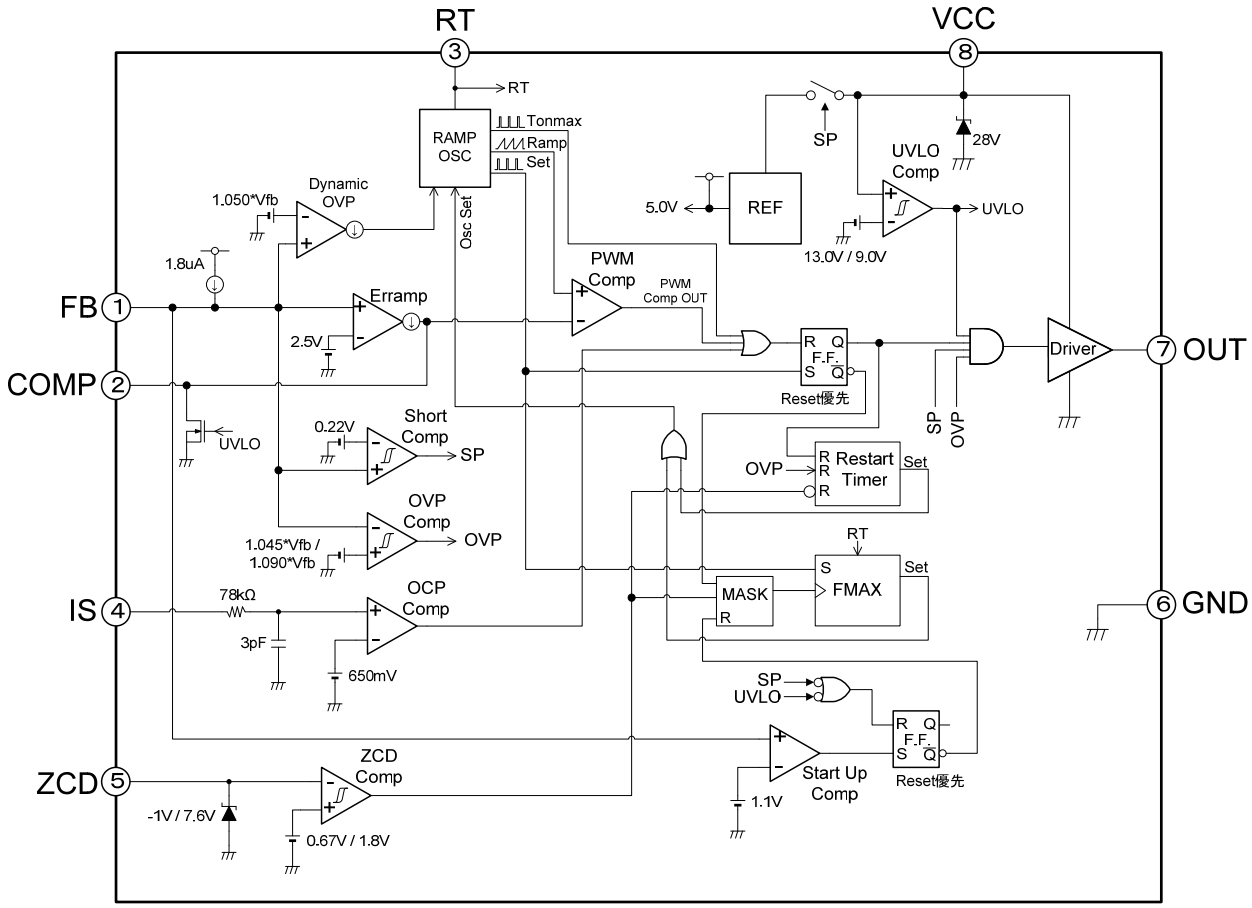
3. Function list by types

Type	Startup Threshold	Package
FA5601N	13V(typ.)	SOP-8

4. Application circuit example

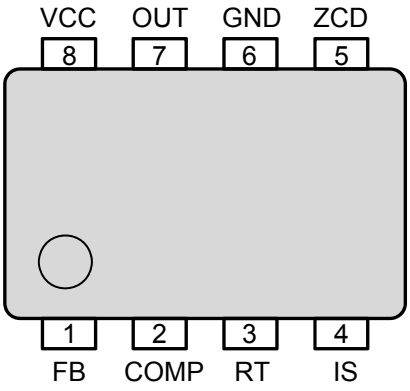


5. Block diagram



6. Functional description of pins

Pin No.	Pin name	Pin Function
1	FB	Feedback Voltage Input *1
2	COMP	Compensation *1
3	RT	Set Maximum on time *1
4	IS	Current Sense Input *1
5	ZCD	Zero Current Detection Input *1
6	GND	Ground
7	OUT	Output
8	VCC	Power Supply *1



Notes)
*1 connect the capacitor.

7. Rating & characteristics

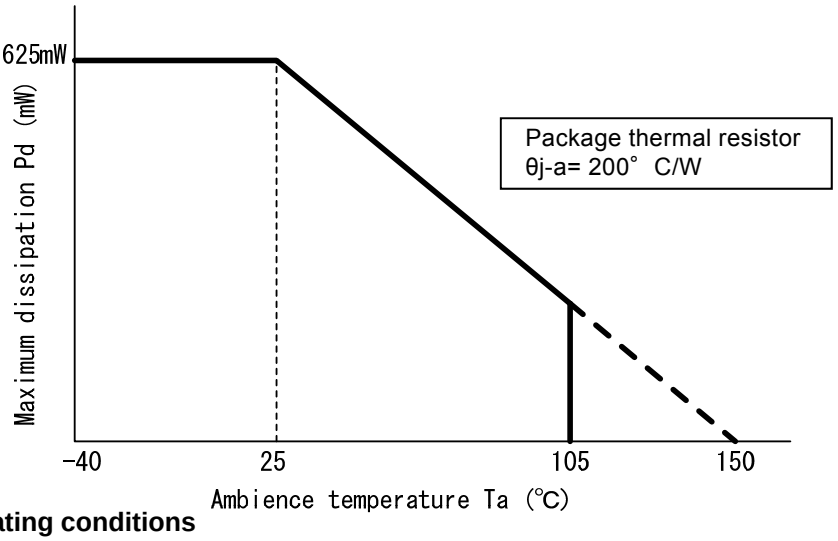
Stress exceeding absolute maximum ratings may malfunction or damage the device.
"-" shows source and "+" shows sink in current descriptions.

(1) Absolute maximum ratings

Item	Symbol	Rating	Unit
Total Power Supply and Zener Current	Icc+Iz	15	mA
Supply Voltage*1	VCC	28	V
Voltage at OUT pin	VOUT	-0.3 to VCC+0.3	V
Output Peak Current Source or Sink*1	Io	-500 +1000	mA
Control pin input voltage(FB)	Vinfb	-0.3 to 5	V
Control pin input current(FB)	Iinfb	-100 to +100	uA
Control pin input voltage(COMP)	Vincomp	-0.3 to 5	V
Control pin input current(COMP)	Iincomp	-100 to +100	uA
Control pin input voltage(RT)	Vinrt	-0.3 to 5	V
Control pin input current(RT)	Iinrt	-100 to +100	uA
Control pin input voltage(IS)	Vinis	-0.3 to 5	V
Control pin input current(IS)	Iinis	-100 to +100	uA
Zero Current Detect Input Voltage	Vinzcd	-2.0 to 8.6	V
Zero Current Detect Input: High State Forward Current Low State Reverse Current	Iinzcd	+50 -10	mA
Power dissipation(Ta=25℃) *1	Pd	625	mW
Operating Ambient Temperature	Ta	-40 to +105	℃
Operating Junction Temperature	Tj	-40 to +150	℃
Storage Temperature	Tstg	-40 to +150	℃

*1 Never exceed power dissipation Pd.

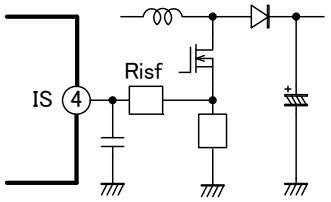
※Maximum dissipation curve



(2) Recommended operating conditions

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	VCC	10	12	26	V
RT pin resistance	Rrt	39	82	150	kΩ
IS pin filter resistance *3	Risf	-	-	100	Ω
ZCD pin current	Izcd	-	-	±3	mA
Operating Ambient Temperature	Ta	-40	-	85	℃

※Recommended value is conditions for guaranteeing that the product operates normally.
If it is used out of this condition, there is possibility of have a negative influence on operation and reliability.
※Please use it after confirming operation enough with your products when you use it.



（3）DC electrical characteristics

The characteristics in this section are those in conditions as follows unless otherwise specified. The voltages described in the conditions are DC input, not AC input.
Tj=25℃, VCC=12V, V(FB)=1.0V, V(COMP)=5V, V(IS)=0V, V(ZCD)=0V, Rrt=82kΩ
Notes)
(1) The item which indicated "*1" are not 100% tested and guaranteed by design.
(2) "—" means that it is not guaranteed.
(3) "-" shows source current and "+" shows sink current in output characteristics.

Error Amplifier (FB pin, COMP pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage feedback input threshold	Vfb	FB pin and Comp pin are shorted	2.465	2.500	2.535	V
Line regulation	Regline	VCC=10V to 26V	-20	-10	—	mV
Temperature stability *1	VdT	Tj=-40 to 125℃	—	±0.5	—	mV/℃
Transconductance	Gm	V(FB)=2.25V, 2.75V, V(COMP)=2.5V, Gm=Icomp_2.75-Icomp_2.25/(2.75-2.25)	50	75	100	umho
Output source current	Icompso	V(FB)=1.0V, V(COMP)=2.5V	-60	-40	-20	uA
Output sink current	Icompsi	V(FB)=4.0V, V(COMP)=2.5V	30	50	70	uA

Ramp oscillator (RT pin, COMP pin, FB pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OUT pin maximum on time	Tonmax	V(COMP)=5.0V, V(FB)=Vfb	20	26	32	us
OUT pin maximum frequency	Fmax	V(COMP)=0.8V	160	220	280	kHz
Maximum frequency Voltage *5	Vfbmax	V(COMP)=0.9V	0.9	1.1	1.3	V
COMP pin threshold voltage for stop switching at OUT pin	Vthcomp	VCOMP(DC) decrease Switching at OUT pin stop	0.6	0.7	0.8	V
RT pin output voltage	Vrt		0.90	1.15	1.40	V

*5: After starting the IC, until FB pin voltage go over the "Maximum frequency voltage" once, off-time of the OUT pin is "Restart timer delay ". And it go over "Maximum frequency voltage" once ,off-time of the OUT pin is "OUT pin maximum frequency lock time " or "(1/"OUT pin maximum frequency") - "OUT pin on time"".

Over voltage comparator(FB pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static OVP threshold voltage for stop switching at OUT pin	Vsovph	V(FB)=2.5V to 3.0V Switching at OUT pin stop	1.070 ×Vfb	1.090 ×Vfb	1.105 ×Vfb	V
	Vsovpl	V(FB)=3.0V to 2.5V Switching at OUT pin start	1.025 ×Vfb	1.045 ×Vfb	1.065 ×Vfb	V
	Vsovphys	Vsovph – Vsovpl	0.020 ×Vfb	0.040 ×Vfb	0.060 ×Vfb	V
Pull up current	Ipullup	V(FB)=2.5V	-2.4	-1.8	-1.2	uA
Dynamic OVP threshold voltage for limiting pulse width of OUT Pin	Vdovp	V(FB)=2.5V to 3.0V, Ton=Tonmax×0.7	1.025 ×Vfb	1.050 ×Vfb	1.075 ×Vfb	V
Staric to dynamic OVP hysteresis voltage	Vhyssd	Vsovph-Vdovp	0.020 ×Vfb	0.040 ×Vfb	0.060 ×Vfb	V

FB short comparator (FB Pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FB pin threshold voltage for stop switching at OUT pin	Vthfb	VFB(DC) decrease Switching at OUT pin stop	0.10	0.22	0.50	V

Current sense comparator(IS pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IS pin threshold voltage for OUT pin turn off	Vthish	VIS(DC) increase Pulse width at OUT pin change	0.63	0.65	0.67	V
Temperature stability of IS pin threshold *1	Vthishdt	Tj=-40℃ to 125℃	—	±1	±2	%
Delay to output (IS pin to OUT pin)	Tphl	IS square pulse, High level = 1.05V, *2 Low level = 0V Transmission delay of IS pin to OUT pin (turn off)	—	180	500	ns

*2: High level（1.05V）is the split voltage of 5V divided by 7.5kΩ and 2kΩ.

Zero current detector(ZCD pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ZCD pin threshold voltage for stop switching at OUT pin *3	Vthzcdh	VZCD(DC) increase Switching at OUT pin stop	1.65	1.8	1.95	V
ZCD pin threshold voltage for start switching at OUT pin	Vthzcdl	VZCD(DC) derease Switching at OUT pin start	0.52	0.67	0.82	V
Hysteresis voltage	Vhyszcd	Vthzcdh-Vthzcdl	1.03	1.13	1.23	V
Input clamp voltage	Vih	Isource=-3.0mA	7.0	7.6	8.2	V
	Vil	Isink=+3.0mA	-1.6	-1.0	-0.4	V
Minimum detect pulse width *1	Tmw	f=110kHz, ZCD pulse, High level=2V, ZCD pulse, Low level=0.3V	100	—	—	ns
Delay to output (ZCD pin to OUT pin)	Tzcd	ZCD square pulse, High level = 2V, Low level = 0.3V Transmission delay of ZCD pin to OUT pin (turn on)	—	100	300	ns
OUT pin maximum frequency lock time	Tzcdmax	VFB(DC)=2.0V Off width of OUT pin	1.4	2.0	2.6	us
Temperature stability of maximum frequency lock time *1	Tzcdmaxdt	Tj=-40℃ to 125℃	—	±5	±10	%

*3: If ZCD becomes high when OUT pin is High, OUT pin does not become low. OUT pin will not become high unless ZCD becomes low.

Driver output(OUT pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage low state	Vol	VCC=12V, V(COMP)=0V, Isink(OUT)= 200mA	—	1.2	3.3	V
Output voltage high state *1	Voh	VCC=12V, Isource(OUT)= -200mA	7.8	8.4	—	V
Output voltage rise time	Tr	V(COMP)=5V, C(OUT)=1000pF	—	50	120	ns
Output voltage fall time	Tf	V(COMP)=5V, C(OUT)=1000pF	—	25	100	ns

Restart timer(OUT pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Restart timer delay	Tdly	V(FB)=0.5V Off width of OUT pin	10	30	50	us

Under voltage lock out(VCC pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Startup threshold voltage	Von	VCC(DC) increase Switching at OUT pin start	11.5	13.0	14.0	V
Shutdown threshold voltage	Voff	VCC(DC) decrease Switching at OUT pin stop	8.0	9.0	10.0	V
UVLO hysteresis width	Vhysvcc	Von-Voff	3.0	4.0	5.0	V
NMOS on resistance *4	Rcomp UVLO	V(VCC)=12V to 8V, V(COMP)=2V	2.0	4.0	6.0	kΩ

*4: When the supply voltage decreases after starting operation, operation stops at 9V (typ.) and the capacitor connected to the COMP pin is discharged by the discharging circuit within the COMP pin.

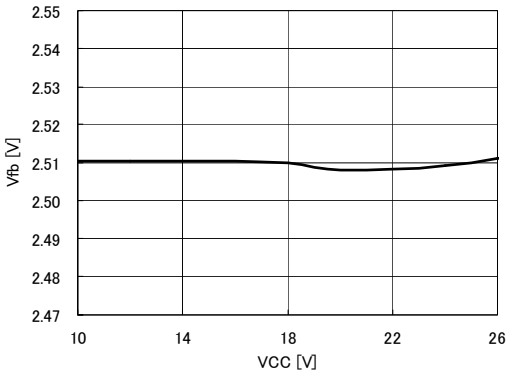
Power supply current(VCC pin)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Startup power supply current	Istart	V(VCC)=Von-0.1V	—	—	80	uA
Operating power supply current	Icc	V(COMP)=Open, C(OUT)=Open	—	1.5	3.0	mA
Dynamic operating power supply current	Iop	V(COMP)=Open, C(OUT)=1000pF	—	2.0	4.0	mA
Stand-by current	Istb	V(FB)=0	—	30	60	uA

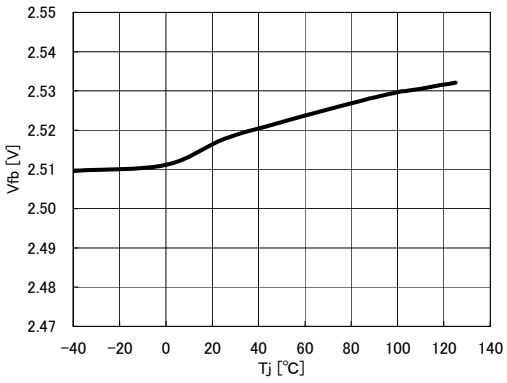
8. Characteristic curve

The characteristics in this section are those in conditions as follows unless otherwise specified.
Tj=25℃, VCC=12V, V(FB)=1.0V, V(COMP)=5V, V(IS)=0V, V(ZCD)=0V, Rrt=82kΩ
Notes)
(1) "-" shows source current and "+" shows sink current.
(2) The data listed here show the typical characteristics of an IC and it does not guarantee the characteristic.

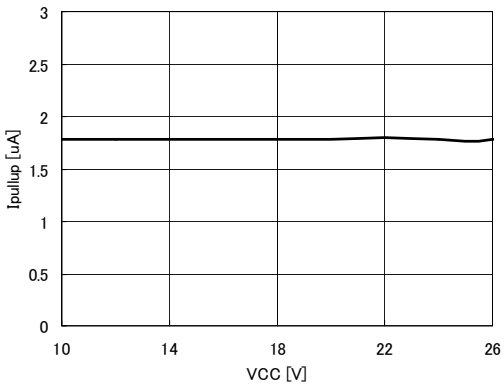
Error amplifier voltage feedback input Threshold (Vfb) vs. supply voltage (Vcc)



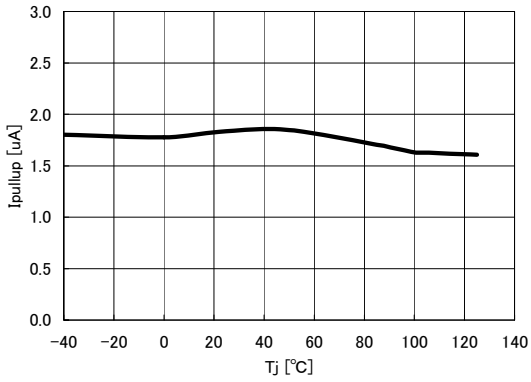
Error amplifier voltage feedback input Threshold (Vfb) vs. junction temperature (Tj)



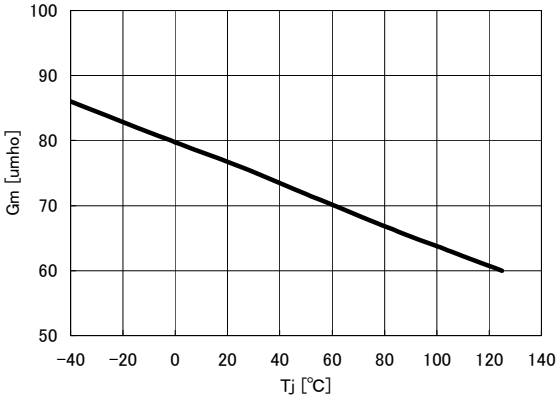
Pull up current (Fb) vs. supply voltage (Vcc)



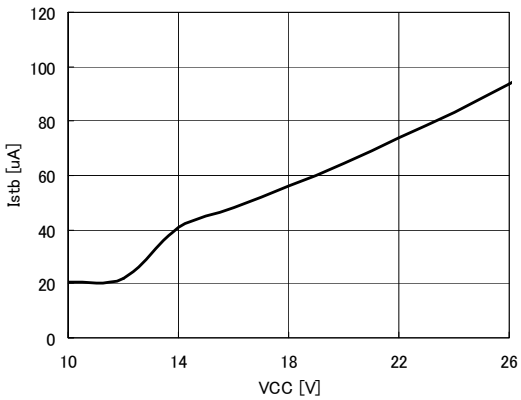
Pull up current (Fb) vs. junction temperature (Tj)



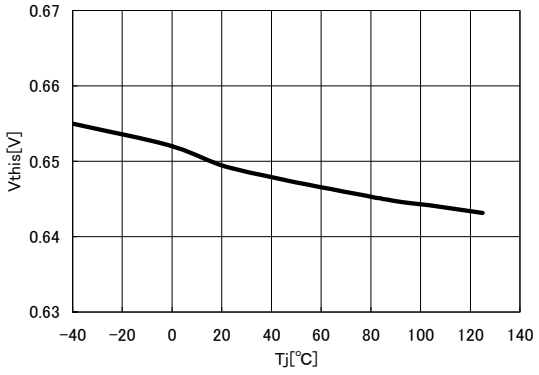
Error amplifier transconductance (Gm) vs. junction temperature (Tj)



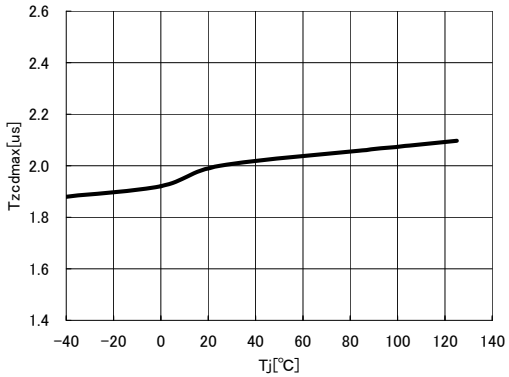
Standby current (Istb) vs. supply voltage (Vcc)



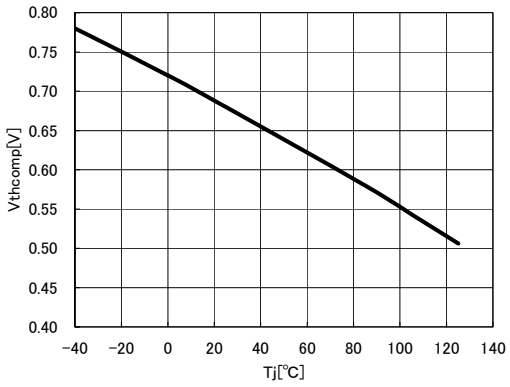
Current sense comparator maximum threshold（Vthis）vs. junction temperature（Tj）



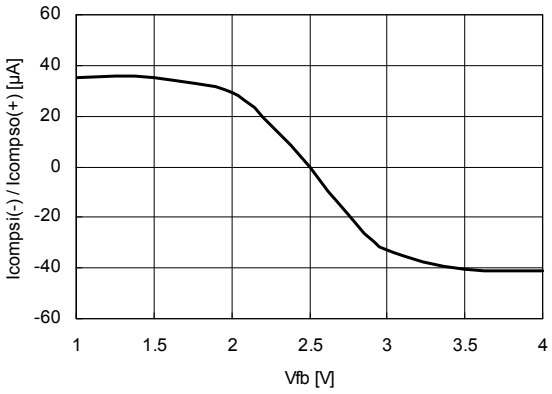
Maximum frequency lock time（Tzcdmax）vs. junction temperature（Tj）



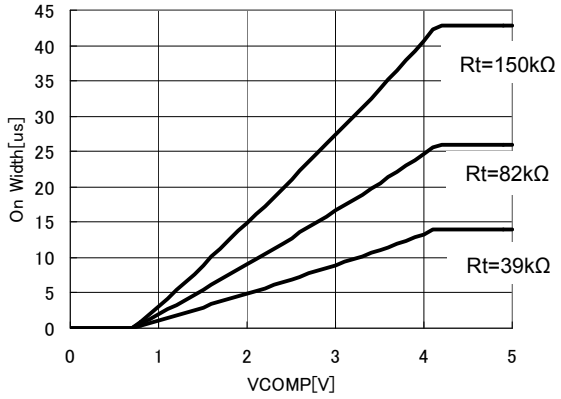
COMP Threshold voltage（Vthcomp）vs. junction temperature（Tj）



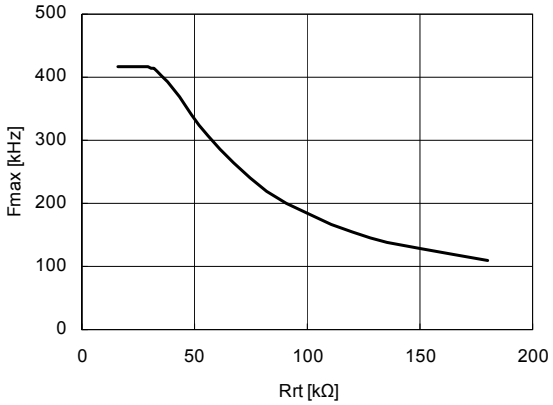
Error amplifier sink/source current（ Icompsi/Icompso）vs. FB Pin voltage（VFB） Vcomp=2.5V



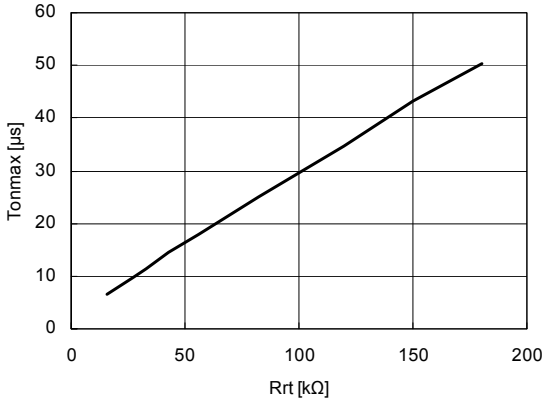
On pulse width vs. COMP Pin voltage（VCOMP）



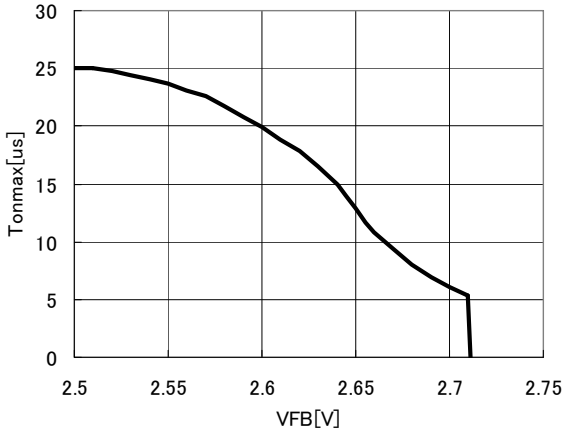
Maximum oscillating frequency（Fmax） vs.
RT resistance（Rrt）



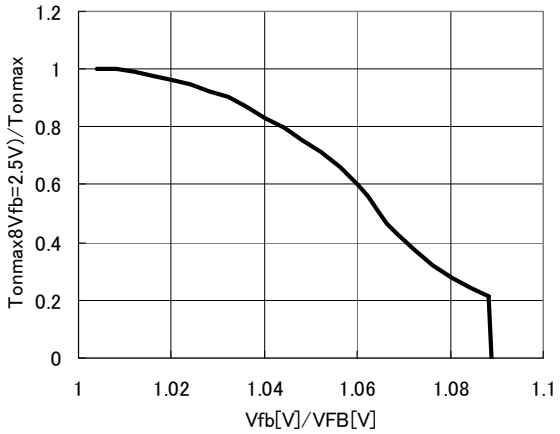
Maximum on-range（Tonmax） vs.
RT resistance（Rrt）



Maximum on-range（Tonmax）vs.
FB voltage（VFB）



Maximum on-range（Tonmax（Vfb=2.5V）/Tonmax） vs.
FB Voltage（VFB[V]/Vfb[V]）



9. Outline of circuit operation

This IC is a power-factor correction converter utilizing a boosting chopper or flyback, operating in critical mode. Hereinafter is outline of the operation consisting of switching operation and power-factor correction operation using the circuit diagram shown in Fig. 1.

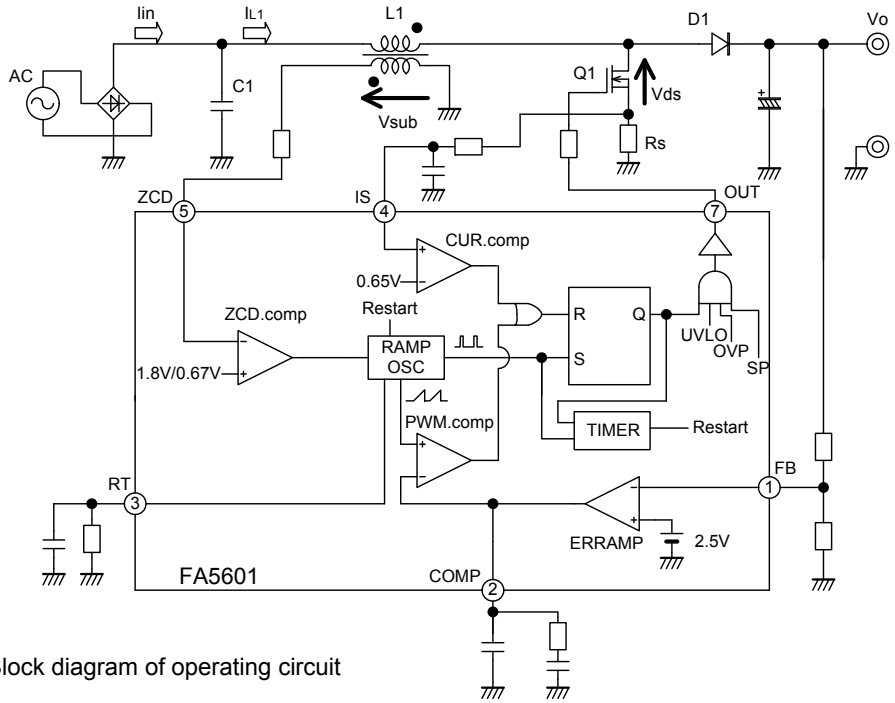


Fig.1 Block diagram of operating circuit

(1) Switching operation

This IC performs the switching operation in the critical mode applying self-oscillation without using an oscillator. Fig. 2 shows the outline of waveforms of the switching operation in steady state. The operation is as follows.

t1. Q1 turns on, the current through inductor (L1) rises from zero. At the timing of Q1 on, Vramp; output of ramp oscillator states to rise.

t2. Vramp and Vcomp; output of the error amplifier are compared by the PWM comparator, and when Vramp>Vcomp, Q1 turns off and Vramp drops.
When Q1 turns off, the voltage across L1 inverts and the current through L1 decreases while the current is supplied to the output side through D1.
In the meantime, voltage Vsub of the auxiliary winding inverts and positive voltage is generated.

t3. When the current of L1 becomes zero completely, the voltage of L1 resonates with the parasitic capacitor and decreases rapidly. Voltage Vsub of the auxiliary winding installed on L1 decreases rapidly at the same time.

t4. When Vsub decreases to the internal reference voltage of 0.67V, output of the zero current detector (ZCD.comp) becomes low and pulse is output from the ramp oscillator to turn on Q1 and move to the next switching cycle (t1).

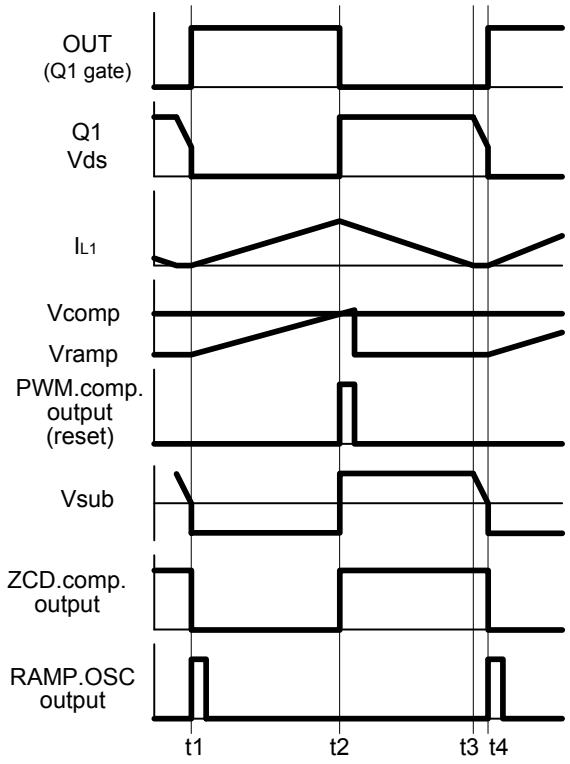


Fig.2 : Switching operation, Waveforms

By repeating the operations of t1 to t4, the switching in critical mode is continued.

With the power-factor correction circuit in the critical mode, the switching frequency is always changing due to instantaneous values of the AC input voltage. The switching frequency also changes when the input voltage or load changes.

(2)Power-factor correction operation

As explained in the switching operation, the current through inductor repeats in triangular waveforms. The mean value (IL1(mean)) of the triangular wave current becomes 1/2 of the peak value (IL1(peak)). (Fig. 3)
By controlling to make outline linking the peak of the inductor current to sine wave and removing switching ripple current, the smoothed AC input current has sine wave shape.
FA5601 uses fixed on time control shown in Fig. 4.
This control determines the on time of the output of IC (gate drive signal for MOSFET) with combination of the error amplifier output and saw tooth wave. While the load is constant, the output of the error amplifier is constant, and on time also stays constant.
Since an inclination of inductor current depends on input voltage (an inclination of inductor current is proportional to input voltage) and on time is constant, the outline linking the peak of the inductor current becomes same AC waveform as the input voltage, which enables power-factor correction operation.

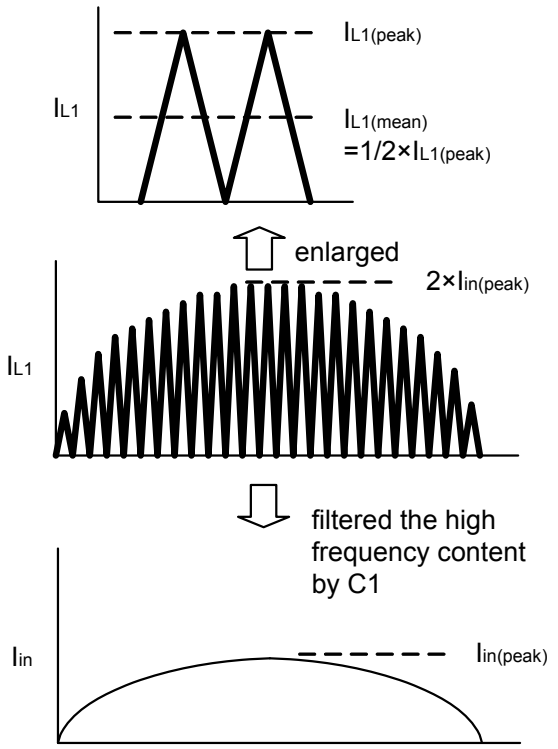


Fig.3 : Power-factor correction operation waveforms

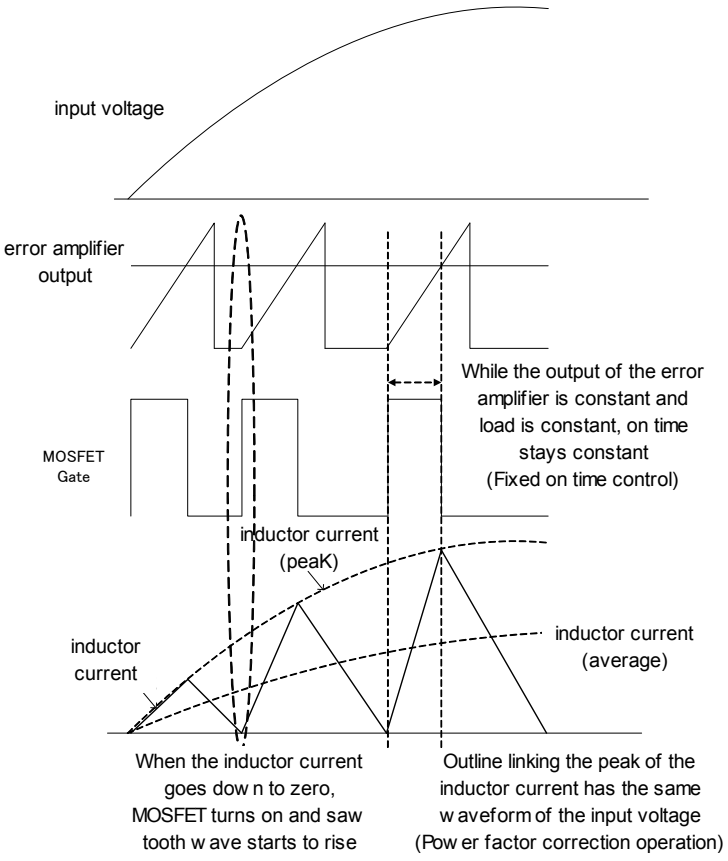


Fig.4 : Fixed on time control

10. Description of each circuit block

(1) Error amplifier circuit

The error amplifier is to make the output voltage constant with feedback control. For this IC, a transconductance type is used for the error amplifier.

The non-inverting input terminal is connected to internal reference voltage of 2.5V (typ.).

The inverting input terminal is fed with output voltage of the power-factor correction converter, and normally use divided voltage with resistors. To the inverting input, internal constant current source of 1.8μA is connected for FB open detection function.

The output of the error amplifier (COMP) is connected to the PWM comparator and controls the on time of the OUT output.

The output voltage of PFC contains much of ripple of frequency 2 times AC power line (50 or 60Hz). When this ripple component becomes largely appears in the output of the error amplifier, the power-factor correction converter does not stably operate. In order to obtain the stable operation, connect capacitors and a resistor between pin No.2 (COMP pin) and GND as shown in Fig.5.

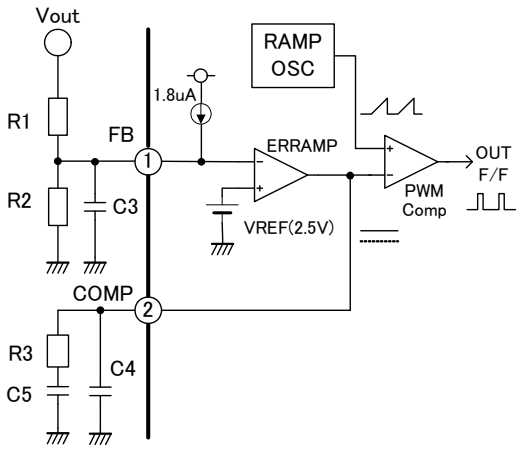


Fig.5 Error amplifier circuit

(2) Overvoltage protection circuit (OVP)

This circuit is to limit the voltage when the output voltage of the power-factor correction converter exceeds the set value.

When this IC starts up or load changes sharply, the output voltage of the converter may exceed the set value. In such a case, this protect circuit works to control the output voltage.

FA5601 has dynamic OVP function to narrow the on time when the FB pin voltage becomes above 2.5V, and static OVP function to stop the output when it becomes higher than 1.09 times the reference voltage.

Normally the voltage of the FB pin is 2.5V, approximately same as the reference voltage of the error amplifier. When the output voltage rises due to starting up or sharp load changes and the voltage of the FB pin becomes higher than 2.5V, the on time narrows by the dynamic OVP function. When the voltage further rises and exceeds the comparator reference voltage, output voltage of the comparator(OVP) inverts to stop the OUT pulse.(Fig. 6)

When the output voltage turns below 1.045 times the reference voltage, the OUT pulse resumes.

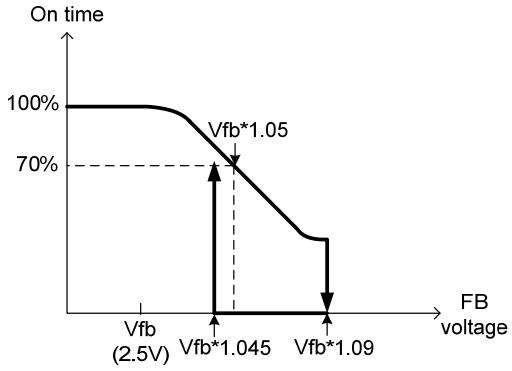


Fig.6 On time at overvoltage

(3)FB short/open-circuit detection circuit

(Standby circuit)

In the PFC circuit of booster type, if feedback voltage is not properly provided to the FB pin due to short-circuit of R2 or open-circuit of R1, the error amplifier cannot control the constant voltage and the output voltage abnormally rises. In such a case, the overvoltage protection circuit also cannot operate because the detection of the output voltage is abnormal.

To avoid such situation, this IC is equipped with FB short-circuit detection circuit.

This circuit is composed of the reference voltage of 0.22V (typ.) and comparator (SP). When the input voltage of the FB pin becomes 0.22V or lower due to such trouble as short-circuit of R2 or open-circuit of R1, the output of the comparator (SP) inverts to stop the output of the IC and the IC stops operation resulting in standby state.

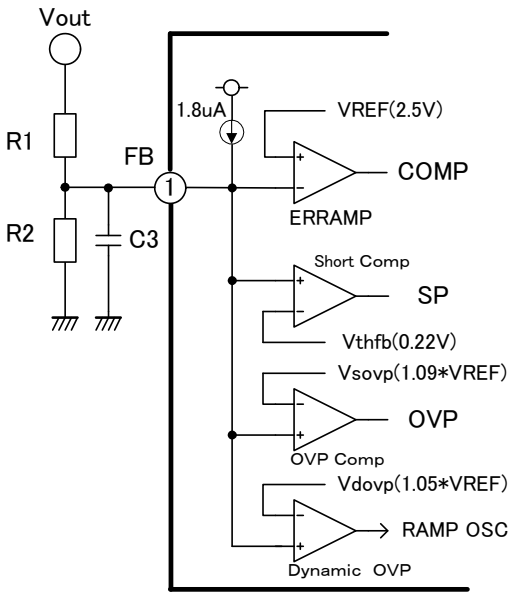


Fig.7 FB pin circuit

Once the voltage of the FB pin decreases to almost zero and the output of the IC stops, and then when the voltage of the FB pin returns to 0.22V or higher, the IC resumes from the standby state and the OUT pulse restarts.
When the connection between the FB pin and the node of voltage dividing resistors is open-circuit, the FB pin voltage is forcefully raised by the internal constant current source of 1.8μA connected to the FB pin. Since the error amplifier output (COMP) voltage decreases as the FB pin voltage rises, the output voltage decreases or OUT output is stopped.

(4) Ramp oscillating circuit

The ramp oscillating circuit receives signal from the zero current detection circuit or restart circuit, and outputs the set signal of F/F for OUT output and saw tooth waveform signal for deciding the duty of the PWM comparator.

(4-1) Maximum frequency limiting

The switching frequency of PFC in the critical mode has characteristic to rise at light load.
FA5601 has the maximum frequency limiting function to improve the efficiency at light load and limits the switching frequency to Fmax (Hz). (Fig. 8)
The maximum frequency Fmax depends on the resistance connected between the RT pin and GND.
When the switching frequency is lower than Fmax, the zero level of the inductor current is detected and MOSFET is turned on to adjust turning on take place at the bottom of Vds waveform, as shown in Fig. 9.
In case of light load where the switching frequency is limited to Fmax, the zero level of the inductor current is detected and no turn-on occurs after the zero current detection delay Tzcd, but turn-on occurs at the cycle of 1/Fmax, as shown in Fig. 10.

(5) Zero current detection circuit

This IC performs the switching operation by self-oscillation in critical mode instead of the oscillator with the fixed frequency. The zero current detection circuit ZCD.comp detects that the inductor current becomes zero to perform the critical mode operation.
The voltage of the auxiliary winding (sub) installed on the inductor is input to the ZCD pin in the polarity as shown in Fig. 11. Positive voltage is generated in the auxiliary winding while MOSFET is off.
Subsequently when the inductor current becomes zero, the auxiliary winding voltage decreases rapidly. This voltage drop is detected by ZCD.comp and the ramp oscillating circuit (RAMP OSC) sends the setting signal to the R-S flip flop to turn on MOSFET and move to the next cycle.

The auxiliary winding voltage changes significantly depending on circuit and input voltage. To cope with this problem, a clamp circuit with the upper limit of 7.6V(typ.) and the lower limit of -1.0V(typ.) is provided.

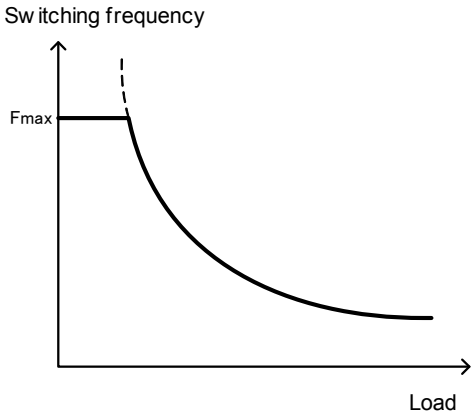


Fig.8 maximum frequency limiting

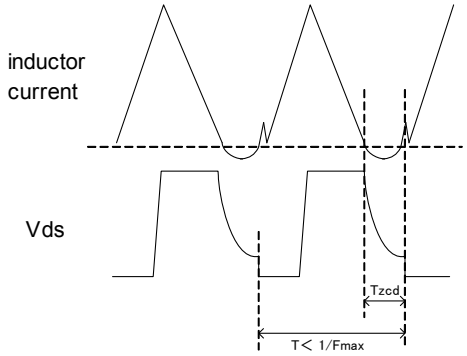


Fig.9 when the switching frequency is lower than the maximum frequency Fmax

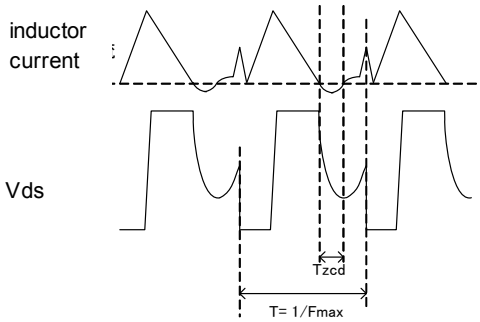


Fig.10 when the switching frequency is limited to the maximum frequency Fmax

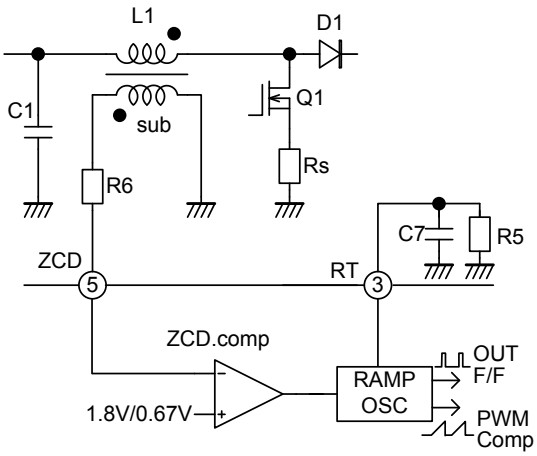


Fig.11 Zero current detection circuit

(6) Overcurrent detection protective circuit

The overcurrent detection protective circuit detects the inductor current and protects MOSFET by turning off the OUT output when it becomes higher than a set current level. For overcurrent detection, the voltage generated in the current sense resistance Rs, which is connected between the MOSFET source and the GND line, is input into the IS pin and compared by the overcurrent detection comparator.

When the IS pin voltage becomes 0.65V (typ) or more, it is output as overcurrent state.

When the overcurrent is detected, the F/F for OUT output is reset to make MOSFET turn off.

(7) Restart timer circuit

This IC utilizes self oscillation instead of the oscillator with fixed frequency, and in the steady operation, it turns on MOSFET with a signal from the zero current detector.

But in start up or light load condition, a trigger signal is required for starting up or stable operation.

This IC is provided with a restart timer.

At the time of start-up, until the FB pin voltage is more than once a maximum oscillation frequency operating voltage Vfbmax (1.1Vtyp),

If the ZCD pin voltage is Low level and OUT output has continued off period 30μs (typ) or more, restart timer generates a trigger signal.

If FB pin voltage is greater than or equal to the maximum oscillation frequency operating voltage Vfbmax (1.1Vtyp), by the ZCD pin voltage is Low level, in a state in which it is limited by the maximum frequency, and then turned on.This signal can realize stable operation even when starting up or the load is light.

(8) Under Voltage Lock Out circuit (UVLO)

UVLO is equipped to prevent circuit malfunction when supply voltage drops.

When the supply voltage rises from zero, the operation starts at 13V (typ.) for FA5601.

When the supply voltage decreases after starting operation, operation stops at 9V (typ.) and the capacitor connected to the COMP pin is discharged by the discharging circuit within the COMP pin.

When UVLO is on and IC stops operation the OUT pin becomes Low and cuts off the output. The current consumption of the IC decreases to 80μA or less.

(9) Output circuit

The output circuit consists of a push-pull circuit, directly drives MOSFET. The peak current of the OUT output is 1.0A maximum for sink and 0.5A maximum for source.

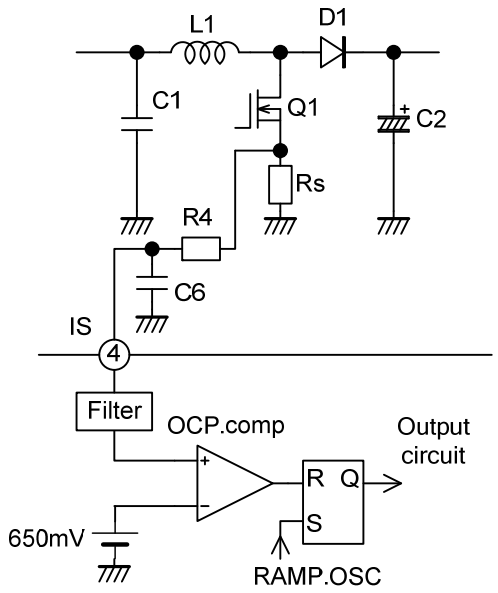


Fig.12 Overcurrent detection protective circuit

11. How to use each pin and advice for designing

(1) Pin No.1 (FB pin)

Functions

(i) Input of feedback signal of output voltage setting
(ii) Detect short-circuit of FB pin
(iii) Detect output overvoltage

How to use

(i) Feedback signal input
- Connection method
  Connect the node between voltage dividing resistors for setting output voltage.
- Operation
  The output voltage Vout of PFC is controlled so that FB voltage matches the internal reference voltage (2.5V).
  To detect FB pin open-circuit, pull-up current (Ipullup) is supplied to the FB pin. This current flows to GND via R2. For this reason, resistance R1, R2 should be set in consideration of this current when the output voltage (Vout) is set.

$$Vout = (VREF/R2 - Ipullup) \times R1 + VREF$$

VREF : Reference voltage =2.5V(typ)
Ipullup : FB pin pull-up current =1.8μA(typ)

To prevent malfunction due to noise, capacitor C3 of 100pF to 3300pF should be connected between the FB pin and GND.

(ii) FB pin short-circuit detection
- Connection method
  Same as for the (i) Feedback signal input
- Operation
  When the input voltage of the FB pin becomes 0.22V or lower due to short-circuit of R2, the output of the comparator (SP) inverts to stop the output of the IC.

(iii) Output overvoltage detection
- Connection method
  Same as for the (i) Feedback signal input
- Operation
  Normally the voltage of the FB pin is 2.5V almost same as the reference voltage of the error amplifier. When the output voltage rises for some reason and the voltage of the FB pin reaches the comparator reference voltage (1.09*VREF), the output of the comparator (OVP) inverts to stop the OUT pulse. If the output voltage returns to the normal value, the OUT pulse resumes.

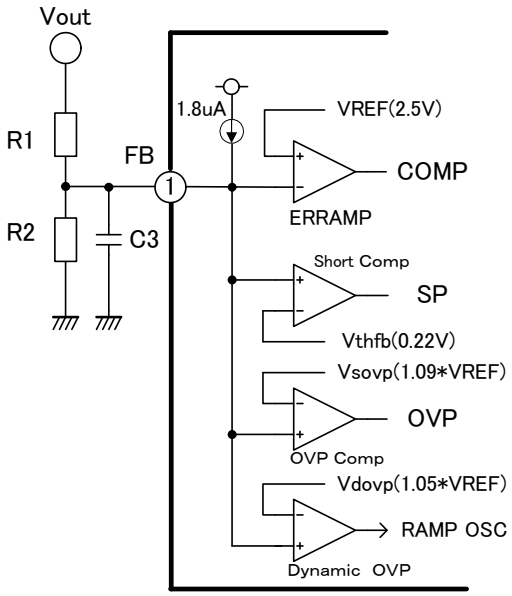


Fig.13 FB pin circuit

(2) Pin No.2 (COMP pin))

Function

(i) Phase compensation of internal ERRAMP output
(ii) Soft start
(iii) ON/OFF operation from exterior

How to use

(i) Phase compensation of internal ERRAMP output
- Connection method
  Connect C, R between COMP pin and GND as shown in Fig. 14.
- Operation
  Connecting C, R to the COMP pin suppress ripple component at 2 times the frequency of the AC line that appears in the FB output.

(Reference)
Example of application circuit : C4=0.1μF
C5=0.15μF
R3=68kΩ
The above is a reference example, and it should be decided by sufficiently verifying with actual application circuit.

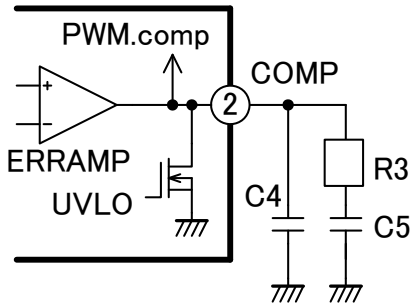


Fig.14 COMP pin circuit

(ii) Soft start
- Connection method
  Connect C between COMP pin and GND as shown in Fig. 14.
- Operation
  By connecting C to the COMP pin, the speed of the COMP pin voltage increase is slowed to restrict sudden widening of the ON time.
  When the capacity of capacitor connected to the COMP pin is larger, the soft start time becomes longer. However, the phase compensation and transient response characteristics are changed at the same time, and so make adjustment while checking actual operation.

(iii) On/off operation from exterior
- Connection method
  Connect the switch such as transistors between COMP pin and GND.
- Operation
  By lowering the voltage of the COMP pin to Vthcomp or less, the output pulse from the IC is stopped. Example of connection is shown in Fig. 15.

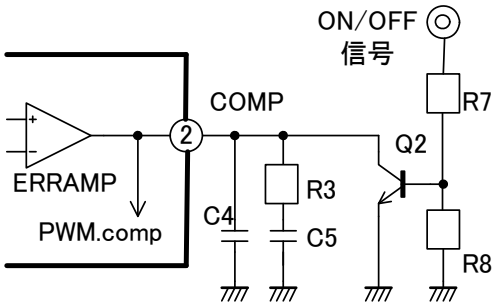


Fig.15 ON/OFF circuit

(3) Pin No.3 (RT pin)

Functions

(i) Set maximum on time
(ii) Set maximum oscillation frequency

How to use

(i) Set maximum on time
In the PFC circuit of booster type, on time Ton in each switching cycle with input and output conditions is theoretically expressed by the following formula.

$$Ton = \frac{2 \times Lp \times Po}{Vac^2 \times \eta}$$

Input Voltage (Vrms) : Vac
Inductor (H) : Lp
Maximum Output Power (W) : Po
Efficiency : η

The maximum on time Tonmax must be set equal to or more than the on time at minimum input voltage Vac(min) at which the on time is maximum. Set the maximum on time Tonmax by the following formula.

$$Tonmax > \frac{2 \times Lp \times Po}{Vac(min)^2 \times \eta}$$

(ii) Set maximum oscillation frequency

To improve the efficiency at light load, FA5601 limits switching frequency at light load to Fmax(Hz). The maximum frequency Fmax depends on the resistance connected between RT pin and GND.

- Connection method

Connect R5 between RT pin and GND as shown in Fig. 16. For the resistance dependency of the maximum on time and maximum oscillation frequency, see Chapter 8. Characteristic Curve.

The current sourced from the RT pin changes depending on the resistance connected. When R5 is relatively large, for example, 82kΩ, the current is about 10uA. When the current is relatively small, it is recommended to connect a capacitor of about 0.01μF in parallel to the resistor to stabilize the RT voltage, as shown in Fig. 16.

In addition, the oscillator slope is changed by the resistance value of RT. Therefore the on time characteristics of MOSFET to the COMP pin voltage is changed and so the circuit gain is changed.

Resistance value of RT is small -> Circuit gain is small

Resistance value of RT is large -> Circuit gain is large

Therefore operation stability and input and load regulations are changed. Make adjustment while checking actual operation.

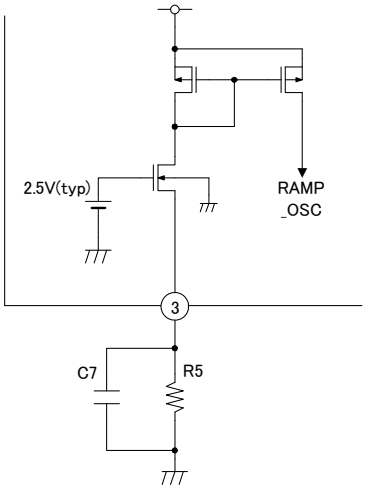


Fig.16 RT pin circuit

(4) Pin No.4 (IS pin)

Function

(i) Detect overcurrent through the MOSFET and turn off OUT output

How to use

(i) Detect current value through the MOSFET

The maximum threshold voltage Vthis of the IS pin is 0.63V(min) to 0.67V(max).

The current detection resistance Rs is set so that necessary current can be supplied for this Vthis.

With maximum output Po(W) and minimum input voltage Vac(min), the maximum value of peak current (ILP(max)) through the inductor and MOSFET can be approximately expressed by the following formula.

$$I_{LP(max)} = \frac{2 \times \sqrt{2} \times Po}{\eta \times Vac_{(min)}}$$

Therefore, the value of Rs(Ω) is determined as follows.

$$Rs < \frac{V_{this}}{I_{LP(max)}} = \frac{0.63}{I_{LP(max)}}$$

- Connection method

Connect the current detection resistor Rs between the source terminal of MOSFET and GND. The voltage across Rs is fed to the IC as the current/voltage conversion signal.

- Operation

(i) When the IS pin voltage becomes larger than 0.65V(typ), the comparator output signal inverts and turns off the OUT output.

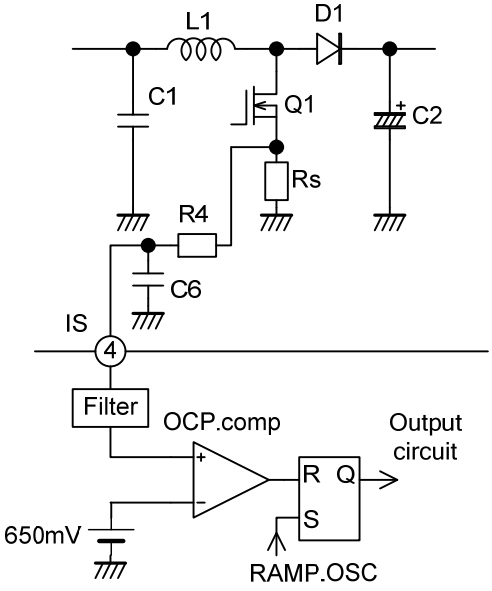


Fig.17 IS pin circuit

- Additional explanation
  When MOSFET turns on, the gate driving current of MOSFET and surge current due to discharging the parasitic capacitors run to the current detection resistance Rs. Large surge current may cause malfunction following disturbed input current waveform. Depending on the amperage of the surge current or timing, whisker-like pulse may be mixed in the turn-on portion of the OUT pulse of the IC. Normally, therefore, a CR filter is connected as shown in Fig.17. The cutoff frequency of this CR filter must be set sufficiently higher than the switching frequency so that it will not affect the normal operation.
  It is recommended to set this cutoff frequency to about 1MHz to 2MHz.

$$\frac{1}{2\times\pi\times C6\times R4} \fallingdotseq 1 \text{ to } 2[\text{MHz}]$$

(5) Pin No.5 (ZCD pin)

Function

(i) Detect zero current

How to use

(i) Detect zero current

The auxiliary winding voltage of L1 is input into the ZCD pin to detect the timing for turning on MOSFET. To use the current, which is flowed into the ZCD pin, within the IC rating, usually the resistance R6 for current limitation is set between the ZCD pin and the auxiliary winding shown in Fig.18.

- Connection method

Connect the R6 between the ZCD pin and the auxiliary winding shown in Fig.18.

It is necessary to limit the current, which is flowed through the clamp circuit of ZCD pin, to 3mA or less in order to operate the IC normally as advised in the recommended conditions. The following formula must be satisfied.

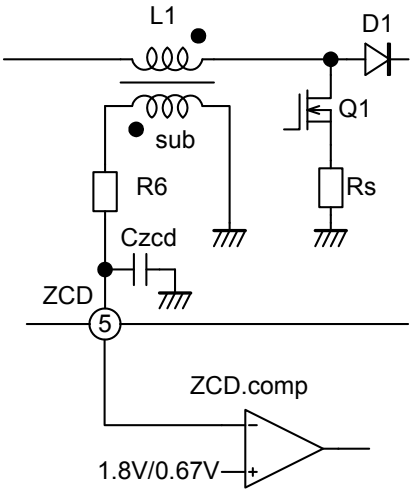


図18: ZCD端子回路

ON:

$$R6 > \frac{-0.4+\sqrt{2}\times Vac(max)\times\frac{Ns}{Np}}{3\times10^{-3}}$$

OFF:

$$R6 > \frac{Vo\times\frac{Ns}{Np}-7.0}{3\times10^{-3}}$$

・Adjustment of the turn-on timing

MOSFET (Q1) turns on after the current of inductor L1 becomes zero. Subsequently Vds between the drain and the source in MOSFET starts vibration just before the turn-on due to the resonance between L1 and the parasitic capacitor element.

Adjust R6 and CZCD so that MOSFET turns on in this resonance trough.

Generally R6 is 10kΩ to 100kΩ, and if adjustment cannot be made only by resistor, CZCD is added to make adjustment (usually the value becomes about 10pF to 100pF).

Then, the switching loss caused when MOSFET is turned on is kept minimal and the surge current generated at the time of turn-on is kept minimal.

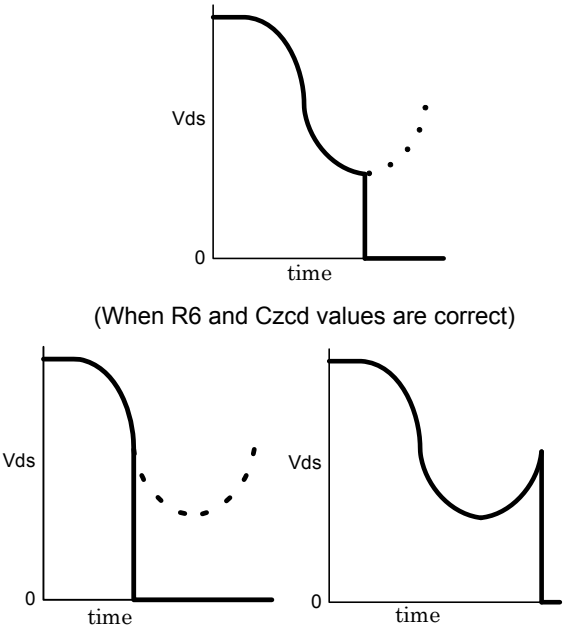


Fig.19 MOSFET waveform just before turn-on

(6) Pin No.6 (GND pin)

Function

This voltage of GND pin is the reference for each portion of whole circuits.

(7) Pin No.7 (OUTpin)

Function

This drives MOSFET.

How to use

- Connection method

Connect it to the gate terminal of MOSFET through resistance.(Fig.20)

- Operation

During the period when turn on MOSFET, the output state is high, and the output voltage is almost VCC.

During the period when turn off MOSFET, the output state is low, and the output voltage is almost 0V.

- Additional explanation

The gate resistor is connected to limit the current of the OUT pin and prevent oscillation of the gate terminal voltage. The rating of the output current is 0.5A for source and 1A for sink.

Using the connections shown in Fig.21 and Fig.22, it is possible to independently set the gate driving current of turning on and off MOSFET.

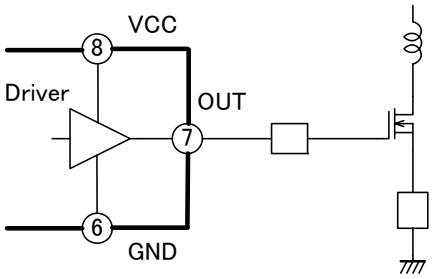


Fig.20 OUT pin circuit (1)

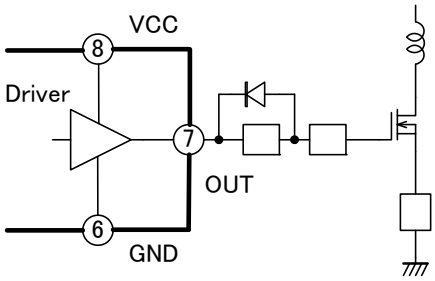


Fig.21 OUT pin circuit (2)

(8) Pin No. 8 (VCC pin)

Function

(i) Supply the power of IC.

How to use

(i) Supply the power of IC.

- Connection method

Connect the start up resistor R7 between VCC pin and Voltage line after rectifying from AC line, which supplies power before IC starts switching operation.

In general application, the power is provided from the auxiliary winding of the transformer through D2 during operation.

In some application, DC power supply can be connected.

- Operation

In the application without DC power supply to feed VCC pin, the current through start up resistor R7 charges the smoothing capacitor C8, and when VCC voltage rises to the on threshold voltage of UVLO, the IC starts operating. Before starting operation, it is necessary to supply current higher than 80μA(max), the startup current of the IC. During steady operation, the VCC is supplied from the auxiliary winding of the inductor. (Fig.23)

When the supply voltage rises from zero, the operation starts at 13V (typ.) for FA5601.

If the supply voltage decreases after the operation starts, the operation stops and capacitor connected to the COMP pin discharged at 9V(typ.) by UVLO. After IC stops operation due to UVLO, the OUT pin is Low state to cut off the output.

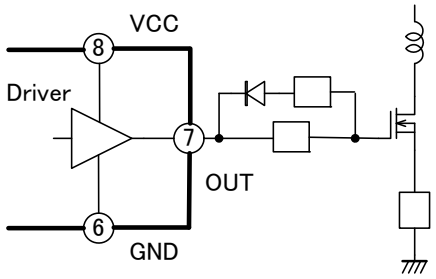


Fig.22 OUT pin circuit (3)

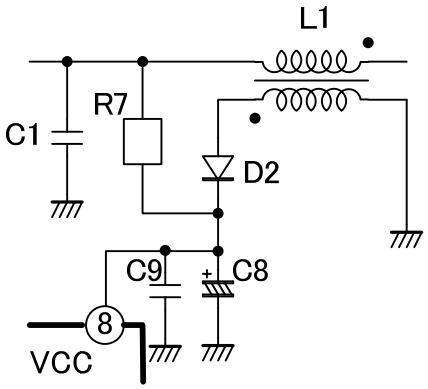


Fig.23 VCC pin circuit (1)

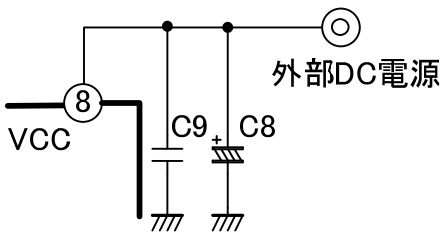


Fig.24 VCC pin circuit (2)

- Additional explanation

UVLO is preventive function to keep the circuit from malfunction when the supply voltage decreases.
With the start up resistor R7, it is necessary to supply current of 80μA or higher, the startup current, until start operating, and the following formula must be satisfied.

$$R8 < \frac{\sqrt{2} \times Vac(min) - Von(max)}{80 \times 10^{-6}}$$

Von(max) : ON threshold voltage of UVLO
FA5601 14V(max)

The value of R7 expressed with the formula is, however, at least necessary and minimum condition to start the IC, and actually it should be decided considering the starting up time required for each application circuit.
During the steady operation, Vcc is supplied from the auxiliary winding of the transformer. But there is some time delay until the auxiliary winding voltage sufficiently rises after the IC starts switching operation. To prevent Vcc from decreasing to the off threshold voltage of UVLO, it is necessary to decide the capacitance of the C8 connected to Vcc. Since this time delay differs depending on the circuit, it should be decided after checking with actual circuit.
It is also recommended to place the ceramic capacitor C9 (about 0.1μF) to remove switching noise.

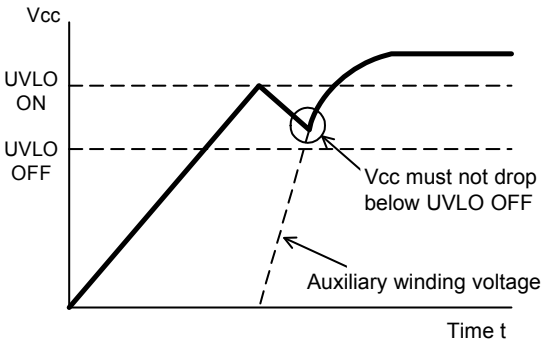


Fig.25 Vcc voltage at startup

- Startup time

When Vcc increases up to the ON threshold voltage of 13V and the IC starts operation, the COMP voltage increases. When the COMP voltage reaches 0.7V, OUT signal is output and operation is started.
The starting time Tstart can be estimated roughly by the following formula:

$$Tstart = \frac{C8 \cdot Von}{\frac{Vac(min) \cdot \sqrt{2}}{R7} - Istart}$$

Istart : startup current

This starting up time must be examined by measuring in actual circuit operation.
Usually capacitor C8 connected to Vcc cannot be so small in capacity and so starting takes time when the starting resistance R7 is large. If the starting resistance R7 is small, the starting time is shortened but loss of starting resistance increases and the efficiency is decreased. As one of measures, it is advised to construct the starting circuit as shown in Fig.26 to shorten the starting time without reducing the efficiency.

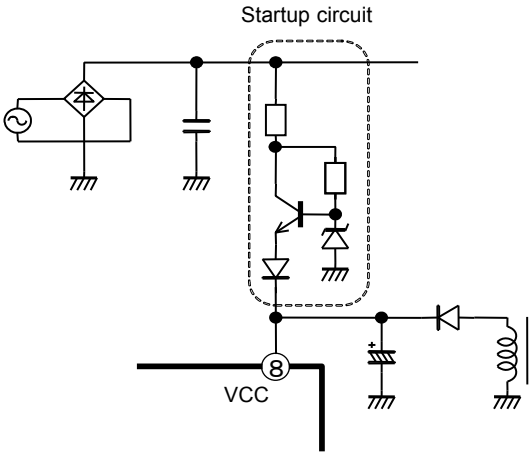


Fig.26 Startup circuit

(9) Minus voltage of each pin

In some cases, the voltage oscillation of Vds just before MOSFET turns on is applied to the OUT pin through parasitic capacitors, etc. and minus voltage may be added to the OUT pin. If this minus voltage is large, the parasitic element inside the IC is activated, and the IC may malfunction.
If this minus voltage is expected to exceed -0.3V, Schottky barrier diode should be connected between the OUT pin and GND. With the forward voltage of the Schottky barrier diode, the minus voltage can be clamped.
For other pins as well, care should be taken so that minus voltage will not be applied in the same way.

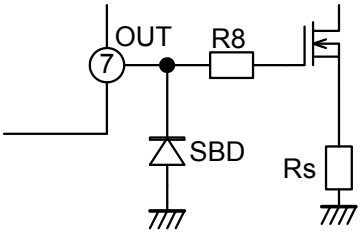


Fig.27 Protection circuit of OUT pin against the negative voltage

(10)Designing auxiliary winding of L1

The auxiliary winding typically has two functions:
-Detecting that inductor current reaches zero
-Supplying Vcc voltage of IC

To achieve these functions, you have to determine a proper ratio of it to the main winding.

The voltage of auxiliary winding always changes according to each instantaneous voltage of AC line. The outline of the auxiliary winding voltage is shown in Fig. 14.
The following conditions should be satisfied based on this various voltage.

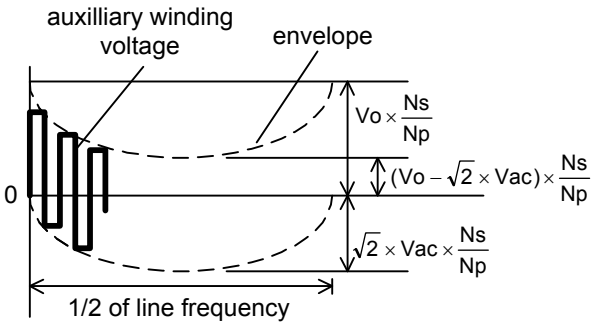


Fig.28 Auxiliary winding voltage

ZCD Threshold Voltage

The threshold voltage of ZCD comparator is 1.95V(max.) when ZCD pin voltage rises. It is necessary for the minimum voltage of auxiliary winding to exceed this threshold voltage. Therefore, the following condition must be satisfied.

$$Ns/Np > \frac{1.95}{(Vo - \sqrt{2} \times Vac(max))}$$

Vcc voltage

The following condition must be satisfied, so that Vcc voltage will be set between 10V and 26V according to the recommended condition.

$$\frac{10}{Vo} < Ns/Np < \frac{26}{Vo}$$

The turns ratio Ns/Np must satisfy both two condition.

If the boost voltage ratio of PFC (the ratio of Vo to Vac) is too small, the turns ratio can not satisfy both condition. This problem can be solved with following methods.

- Attach two auxiliary windings for both ZCD and Vcc respectively.

- Set ZCD condition preceding Vcc condition. In this case, there is possibility for Vcc to exceed the recommended conditions. Therefore, clamp the Vcc with internal ZD or additional ZD (Fig. 29). In this case, a resistance for current limit (R11) is needed between the auxiliary winding and Vcc pin. In addition, especially when using internal ZD, mind that “Total power supply and zener current” and “Power dissipation” must not exceed the absolute maximum rating value.

In some case, the Vcc voltage cannot be supplied enough in light load condition. In this case, the circuit shown in Fig.30 may be effective to improve the Vcc.
The appropriate value of C8 and R10 should be tested and determined in actual circuit because they depend on each circuit.

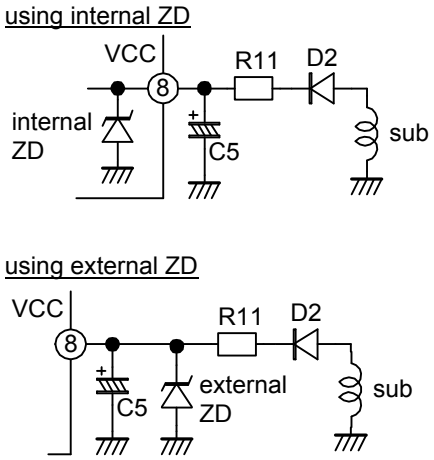


Fig.29 Vcc clamp circuit

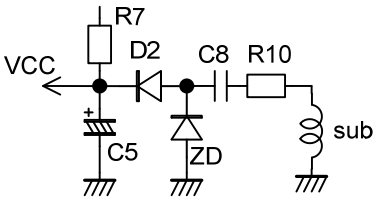


Fig.21 Vcc pin circuit (3)

12. Advice for design

(1) Advice in pattern designing

Main circuit MOSFET, inductor, diodes, etc. perform switching under high voltage and large current. If wiring of IC or signals inputted to IC gets too near such main circuit parts, they may operate erratically upon being affected by noise generated there.

Attention must be paid particularly in following cases (examples of faulty cases).

・IC is arranged under inductor or other main circuit parts, or immediately behind main circuit parts on double sided circuit board (Fig. 31)

・IC is arranged close to inductor, MOSFET or diode (Fig. 32)

・Signal wiring is placed under inductor or near MOSFET or diode (Fig. 33)

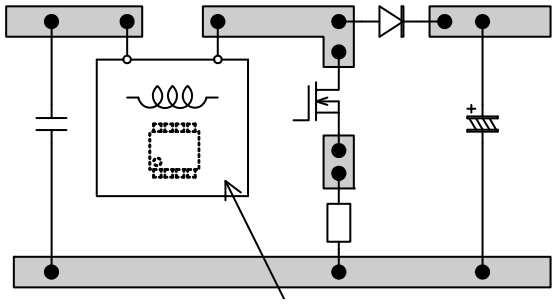


Fig.31 Bad example (1)

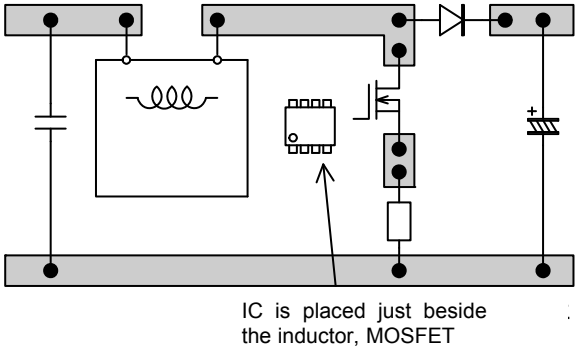


Fig.32 Bad example (2)

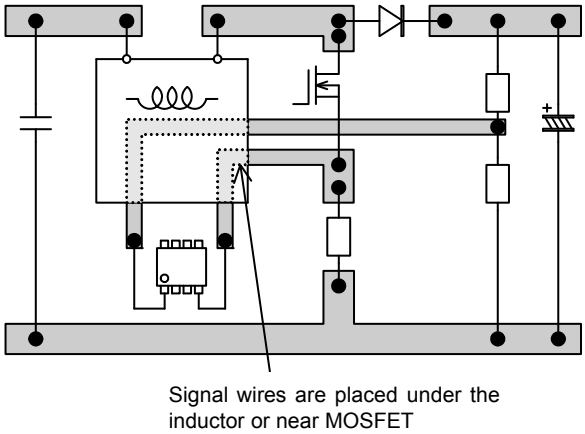


Fig.33 Bad example (3)

(2)Example of GND wiring around IC

Notes）

Wiring is exemplified for you to understand how to connect the GND line.

Noise and incidental erratic operations differ from one instrument to another. Adopting any wiring exemplified in Fig. 34 will not necessarily guarantee normal operations of your instruments.

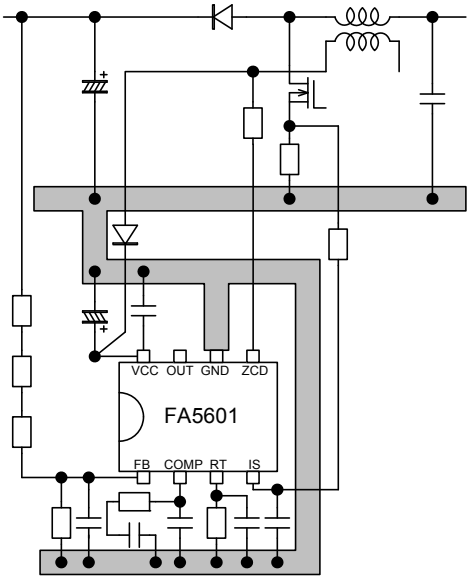


Fig.34 Example of advisable GND wiring

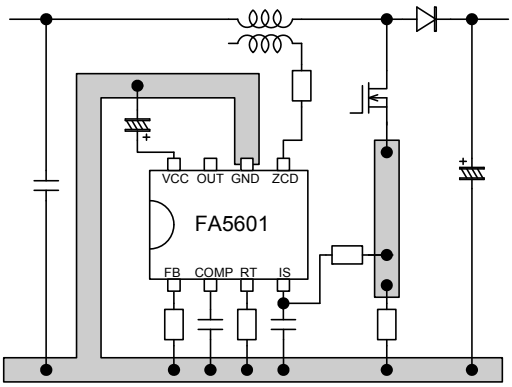


Fig.32 Bad example of GND wiring around IC
(GND is common to signal line parts and main circuit)

13. Example of application circuit (390V / 0.25A output)

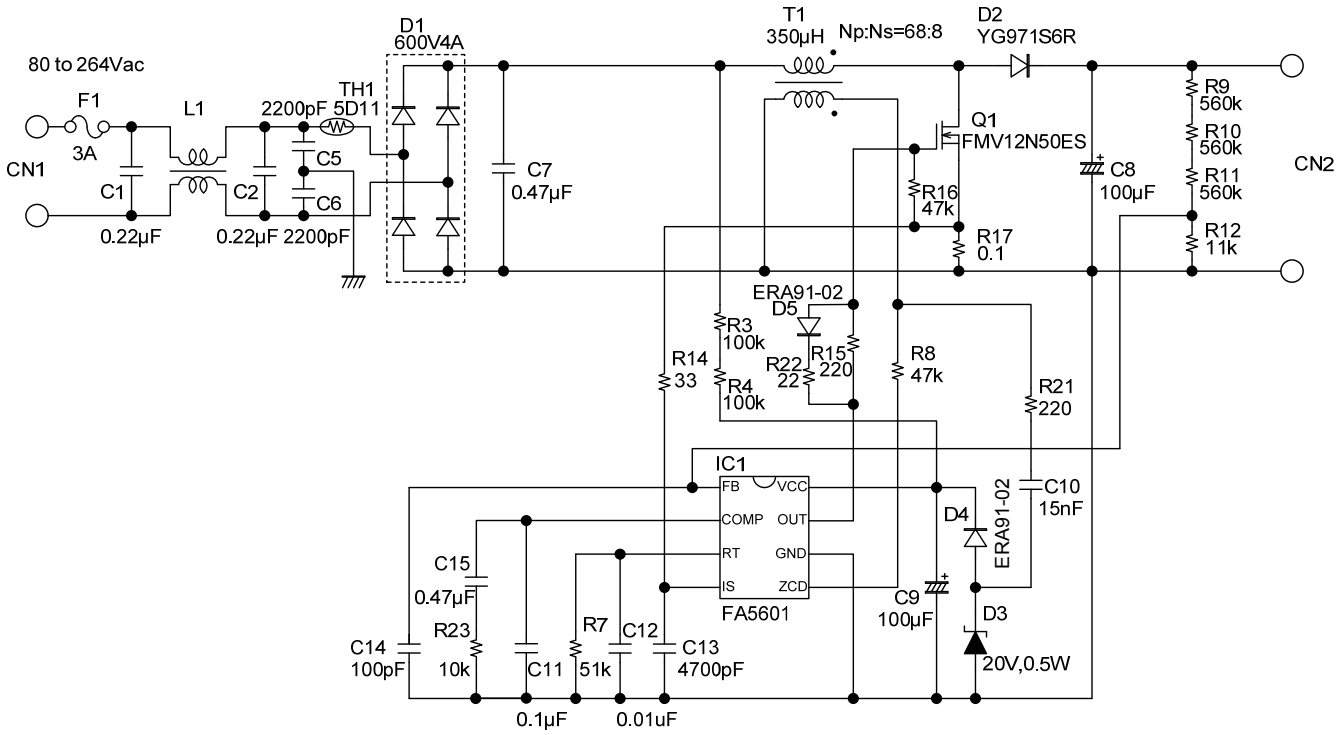


Fig.36 Example of boost PFC circuit

Note) This application circuit is a reference material for describing typical usage of this IC, and does not guarantee the operation or characteristics of the IC.

14. Example of PFC flyback circuit

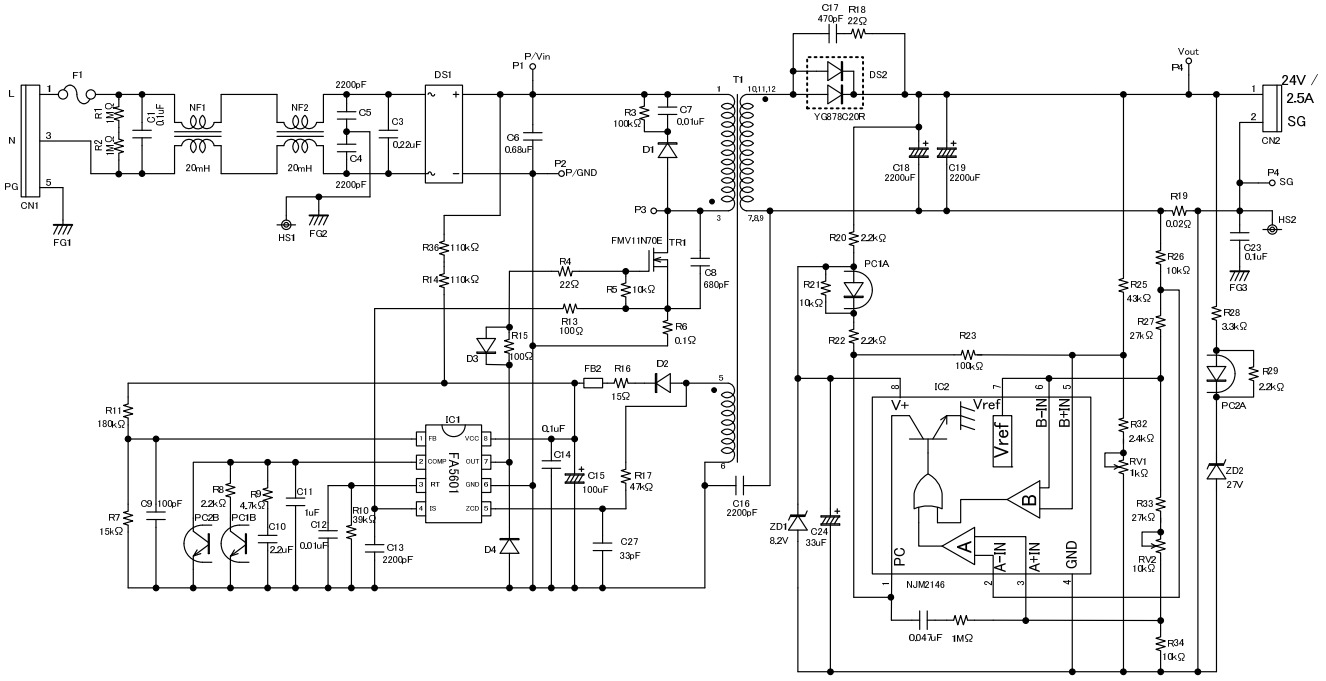


Fig.37 Example of PFC flyback circuit (CV/CC control)

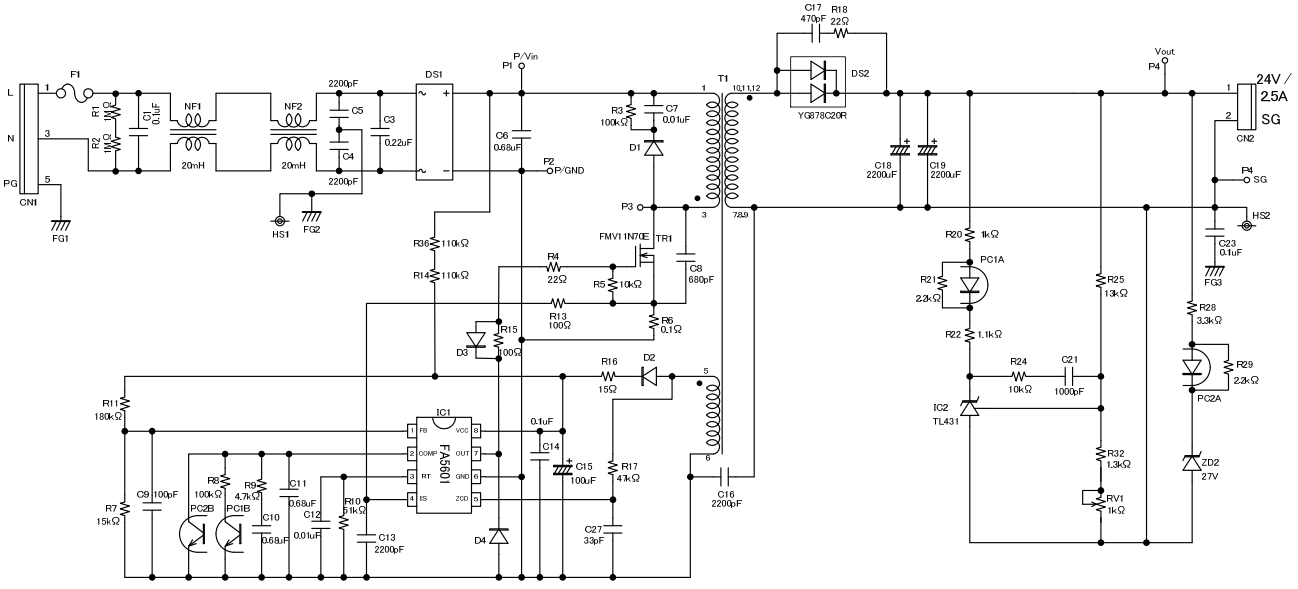


Fig.38 Example of PFC flyback circuit (CV control)

Note) This application circuit is a reference material for describing typical usage of this IC, and does not guarantee the operation or characteristics of the IC.

15. Advice for design of PFC flyback circuit

(1) Design of feedback circuit

Fig.39 shows an example circuit using a photo-coupler for secondary-side feedback in an isolated circuit configuration such as an application circuit.

[1] Voltage of 0.6V to 2.0V is input into the FB pin so that the error amplifier output (COMP) becomes high-level output during operation.

[2] In this example circuit, the COMP pin is used for both phase compensation and output feedback and so C and R are connected to the photo-coupler as shown in Fig.39. If resistance R4 which restricts the photo-coupler is too large, control cannot be performed during light load. Usually 15kΩ or less is advised.

When load is kept constant by phase the compensation capacitors C4, C5 and the resistance R3, adjust the COMP pin voltage to be almost flat (DC).

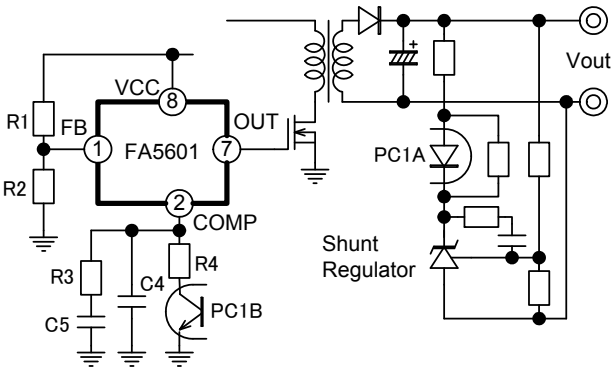


Fig.39 Example of feedback circuit

(2) Adjustment of turn-on timing

The ZCD pin is connected to the auxiliary winding installed on the transformer through the CR circuit of R_{ZCD} and C_{ZCD} (fig. 40).

Be careful of the polarity of the transformer auxiliary winding.

If voltage of the ZCD pin decreases to 670mV or less, MOSFET is turned on. The auxiliary winding voltage changes significantly in both positive and negative directions. To protect IC against this voltage, a clamp circuit is provided.

Just before turn-on, the MOSFET voltage oscillates due to the resonance between the transformer inductance and the resonant capacitor Cd. Adjust C_{ZCD} so that MOSFET turns on in the trough of this resonance (Fig. 41).

Generally R_{ZCD} is 10kΩ to 100kΩ and C_{ZCD} is about 10pF to 100pF.

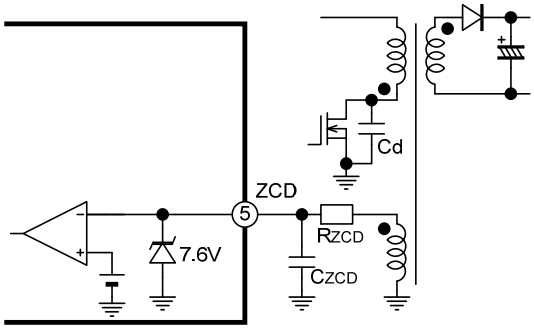


Fig.40 Example of ZCD pin circuit

(3) Starting operation

Example connection of the VCC pin is shown in Fig.42.

When Vcc increases to the ON threshold voltage of 13V due to the current by the starting resistance R7, the UVLO circuit is released and the IC starts operation. When operation is started, the COMP pin voltage increases. When it reaches 0.7V, OUT signal is output and operation is started (Fig.43).

Vcc is supplied form the transformer auxiliary winding during steady operation. After the IC starts, however, there is slight time lag before the auxiliary winding voltage starts sufficiently. It is necessary to determine the proper capacity of the capacitor C8 connected to Vcc so that Vcc does not decrease to the UVLO off threshold voltage during this time lag.

Since this time lag changes depending on circuits, determine the capacity while checking actual operation.

It is advised to install a ceramic capacitor C9 (about 0.1μF) near the IC to remove switching noise.

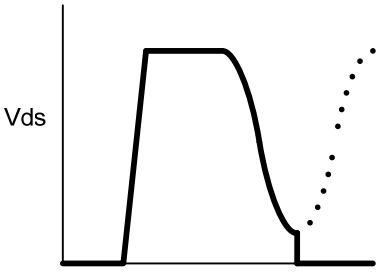


Fig.41 MOSFET Vds waveform

The IC starting time Tstart can be estimated roughly by the following formula.

$$Tstart = \frac{C8 \cdot Von}{\frac{Vac(min) \cdot \sqrt{2}}{R7} - Istart}$$

Istart : Startup current

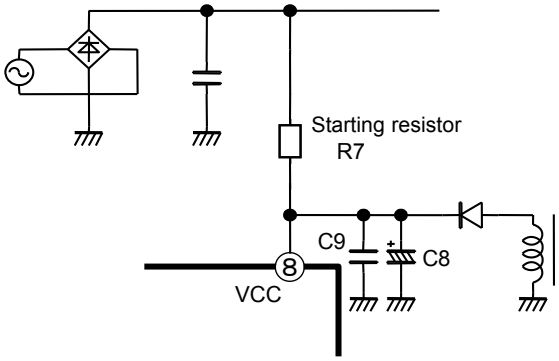


Fig.42 VCC pin circuit

Usually capacitor C8 connected to Vcc cannot be so small in capacity and so starting takes time when the starting resistance R7 is large.

If the starting resistance R7 is small, the starting time is shortened but loss of starting resistance increases and the efficiency is decreased. As one of measures, it is advised to construct the starting circuit as shown in Fig.44 to shorten the starting time without reducing the efficiency.

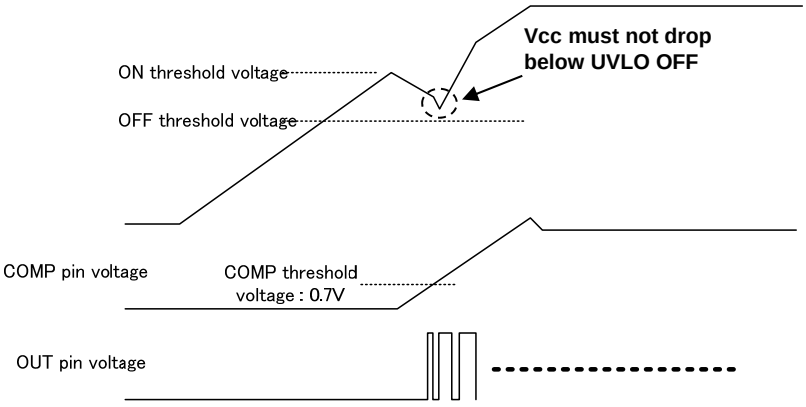


Fig.43 Vcc voltage at startup

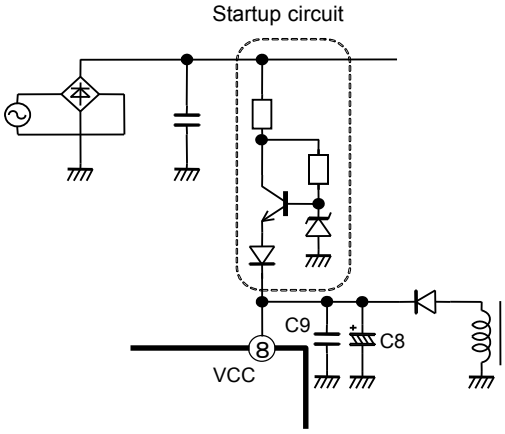


Fig.44 Startup circuit

16. Advice for use of PFC flyback circuit

(1) Precautions for designing patterns

Due to principal current, lightning surge test, AC input surge test and static electricity test, current may flow into the negative-side pattern and its surge voltage (noise) may cause malfunction of the control IC (unstable voltage, unstable waveform and latch stop). Therefore carefully study the following for design to avoid malfunction.

There are the following current pathways in the power source.

[1] Principal current, which flows from the electrolytic capacitor to the transformer primary winding, MOSFET and current detection resistor after rectification of AC power supply

[2] Rectified current, which flows from the transformer auxiliary winding to the electrolytic capacitor, and drive current, which flows from the electrolytic capacitor to the control IC and the MOSFET gate

[3] Control current of the control IC such as output feedback

[4] Filter current and surge current, which flow between the primary and secondary sides

- Separate the negative-side patterns [1] to [4] so that they are not interfered.
- The pathway where the primary current flows must be the shortest loop to keep the MOSFET surge voltage minimal.
- The electrolytic capacitor and the film capacitor between the VCC pin and GND must be installed immediately near the respective pins and connected in the shortest distance.
- Place the filter capacitors connected to the FB pin, IS pin and ZCD pin immediately near the respective terminals and connect them in the shortest distance. Especially separate the negative-side pattern of FB pin from other patterns wherever possible.
- Do not place the high impedance control circuit and the patterns just below the transformer.

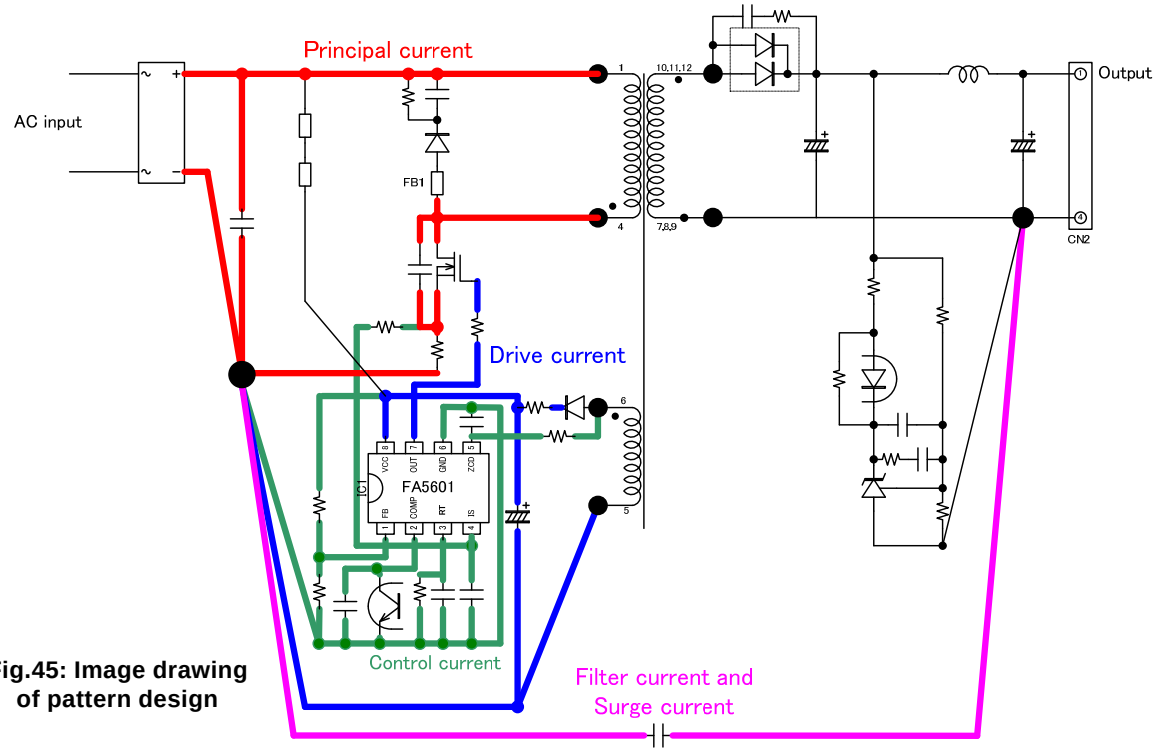


Fig.45: Image drawing of pattern design

17. Precautions in use regarding terminal noise

When the single-pulse noise is input each pin of IC, IC may malfunction following below. Please confirm that neither the instable operation nor the malfunction occurs by noise and use this IC

条件	端子 Pin	懸念される不具合 malfunction in fear	入力の規定 Input regulations	設計上の注意事項 cautions in design
ノイズ入力 (定格電圧以内) input noise (within absolute maximum ratings)	FB	ノイズが過電圧保護レベルを越えると、スイッチングが停止する可能性があります switching may stop when noise is over over voltage protection level	入力信号は出力電圧のフィードバック電圧もしくは、固定電圧としてください input signal for feedback voltage of output voltage or the fixed Voltage	端子直近にコンデンサを接続してください connect capacitor near terminal pin
		ノイズがショート検出レベルを下回るとICがスタンバイモードになる可能性があります (スタンバイモード解除後はリスタート動作になます) IC may become stanbay mode when noise is under short detection level (after standby mode cancellation become restart mode)		
		ノイズによって、出力電圧にオフセットが発生し、出力電圧が上昇又は低下する可能性があります offset occurs in output voltage and output voltage rises or falls by a noise		
	COMP	ノイズにより、オン幅が負荷によって一定でなくなり、出力が大きく変動する可能性があります on width may become not constant by load, output may change heavily	ノイズが入らないようにしてください cancel noise	位相補償の定数は十分確認してください confirm sufficiently phase compensation constant
		ノイズがスレッシュホールド電圧超えると、スイッチングする可能性があります switching may become when noise is over threshold voltage		
		ノイズがスレッシュホールド電圧を下回ると、スイッチングが停止する可能性があります switching may stop when noise is under threshold voltage		
	RT	ノイズにより、オン幅が負荷によって一定でなくなり、出力が大きく変動する可能性があります on width may become not constant by load, output changes heavily	ノイズが入らないようにしてください cancel noise	端子直近にコンデンサを接続してください connect capacitor near pin
		端子電圧よりも高い電圧が入ると最大オン幅制限が効かなくなる可能性があります (端子電圧よりも高い電圧が入るとオン幅が変動する可能性があります) restriction of maximum on time may not work when voltage is higher than pin voltage (on width may change when voltage is higher than pin voltage)		
		端子電圧よりも低い電圧が入ると オン幅及び最大周波数制限が変動する可能性があります on width and restriction of maximum frequency may change when voltage is lower than pin voltage		
	IS	ノイズがスレッシュホールド電圧超えると、スイッチング停止する可能性があります switching may stop become when noise is over threshold voltage	ノイズが入らないようにしてください cancel noise	端子直近にコンデンサを接続してください connect capacitor near IC
	ZCD	ノイズによって、意図しないタイミングでターンオンが発生し、Mos/Diodeの発熱が多くなる、スイッチングノイズが大きくなる可能性があります turn-on occurs unintentional timing, Mos/Diode heat and switching noise may becomes bigger by a noise	ノイズが入らないようしてください cancel noise	端子直近にコンデンサを接続してください connect capacitor near pin
		ターンオンスレッシュを越える時間が遅延時間以下だとターンオンしない可能性があります It may not turn on when the time over turn-on threshold is less than delay time	インダクタとMosの容量成分が共振しても遅延時間以上スレッシュを越える電圧を入力してください Although Inductor and Mos capacitance is resonant, input voltage more than threshold over delay time	端子直近にコンデンサを接続してください connect capacitor near pin
		ノイズの周波数が設定の最大発振周波数より速いと最大発振周波数動作となる可能性があります it may become maximum frequency mode when noise frequency is faster than maximum frequency of setting	ノイズが入らないようしてください cancel noise	端子直近にコンデンサを接続してください connect capacitor near pin
	GND	基準電位が変動し、ICが正常な動作をしない可能性があります reference voltage changes, IC may not behave normally	ノイズが入らないようにしてください cancel noise	GND配線は太い配線としてください ground wiring should be a wide wiring
	OUT	ドライバの能力以上の信号が入力されるとMosを正常に駆動できず、出力が低下する可能性があります the output may fall not to be able to drive Mos normally when signals more than the ability of the driver are input	ノイズが入らないようにしてください cancel noise	—
	VCC	UVLOを下回るノイズが入力されるとICが停止する可能性があります IC may stop when noise under UVLO is input	動作時にUVLOを下回るノイズを入力しないでください don't input noise under UVLO when operating	端子直近にコンデンサを接続してください connect capacitor near pin
マイナス電圧入力 (絶対最大定格以下) input minus voltage (less than absolute maximum voltage)	FB COMP RT IS ZCD VCC	寄生素子が動作し、IC停止等の誤動作が発生する可能性があります a parasitism element works, and the malfunction such as IC stop may occur	絶対最大定格を下回るマイナス電圧を入力しないでください don't input minus voltage less than maximum absolute voltage	—
	OUT	ICが破壊する可能性があります IC may be destroyed		—
プラス電圧入力 (絶対最大定格以上) input plus voltage (more than absolute maximum voltage)	FB COMP RT IS ZCD OUT VCC	ICが破壊する可能性があります IC may be destroyed	絶対最大定格を上回るプラス電圧を入力しないでください don't input minus voltage more than maximum absolute voltage	—

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   - Machine tool - Audio Visual equipment - Home appliance - Personal equipment
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