iC-MCB

SPI-TO-BiSS BRIDGE WITH RS422 TRANSCEIVER

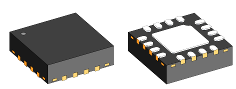
FEATURES

- BiSS Interface slave
- Full BiSS protocol support
- Two data channel configurable
- Three slave IDs occupiable
- Single-cycle data buffer of 64 byte organized in multiple banks for simultaneous access
- Built-in control communication
- RS422 line driver/receiver for BiSS/SSI point-to-point network
- BiSS bus structure capable
- SPI slave interface for sensor data provided by microcontroller
- Fast Sensor interface for direct sensor data provided by an SPI slave device
- BiSS safety related features: Two data channels for Control and Safety Position Word, 6/16 bit CRC + CRC start value
- BiSS timeout: adaptive, 2 µs, 20 µs
- SSI protocol support
- Operation from 3.0 V to 5.5 V
- Operating temperature range of -40° C to +125° C
- Space-saving 16-pin QFN package

APPLICATIONS

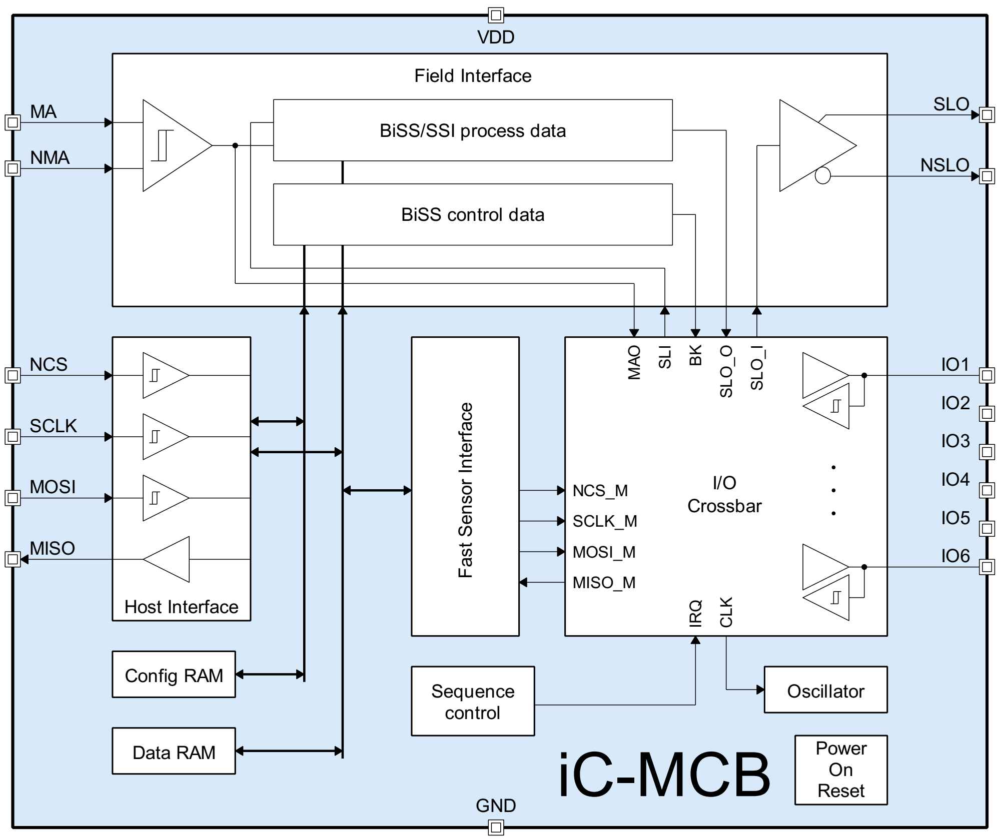
- BiSS slave implementation
- Multiple sensor devices
- Encoder
- Condition monitoring extension
- Diagnosis extension
- Torque sensor
- Acceleration sensor
- Inclinometer
- Safety light curtain

PACKAGES



16-pin QFN
3 mm x 3 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-MCB is a BiSS slave bridging iC to implement BiSS slave functionality into any sensor technology and platform. A wide range of combinations can be covered with the iC-MCB on direct component access and via microcontroller host software solution support.

BiSS sensor implementations are possible. A downgrading configuration to SSI sensor operation is also possible.

Full BiSS C protocol functionality including single-cycle data (SCD) for sensors (SCDS) and control communication for commands and register access. Timing critical protocol response is handled by the iC-MCB directly and relieves the microcontroller host.

Typical applications use a device host microcontroller for providing data and coordinating control communications content. The host microcontroller configures and controls the iC-MCB via SPI interface. The iC-MCB can also be operated without any device sided microcontroller, just by BiSS device configuration boot sequence and self-sustaining operation.

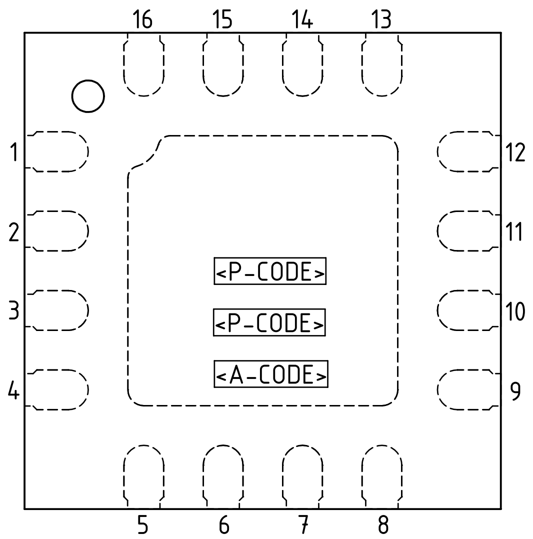
iC-MCB can access and control various sensors directly by an own Fast Sensor Interface. The Fast Sensor Interface is a configurable SPI master interface on the I/O crossbar. The configuration controls the sequence, timing and content of an external SPI slave device into iC-MCB data channel.

The integrated RS422 transceiver for the physical layer of the field interface (PHY) enables for BiSS point-to-point encoder applications. The maximum BiSS clock rate is 10 MHz.

The integrated I/O crossbar and an additional RS422 transceiver PHY enables BiSS bus structure applications. With the integrated I/O crossbar the BiSS bus structure position can be defined by configuration.

PACKAGING INFORMATION

PIN CONFIGURATION
QFN16-3x3 (3 mm x 3 mm x 0.9 mm)
(according to JEDEC Standard MO-220)

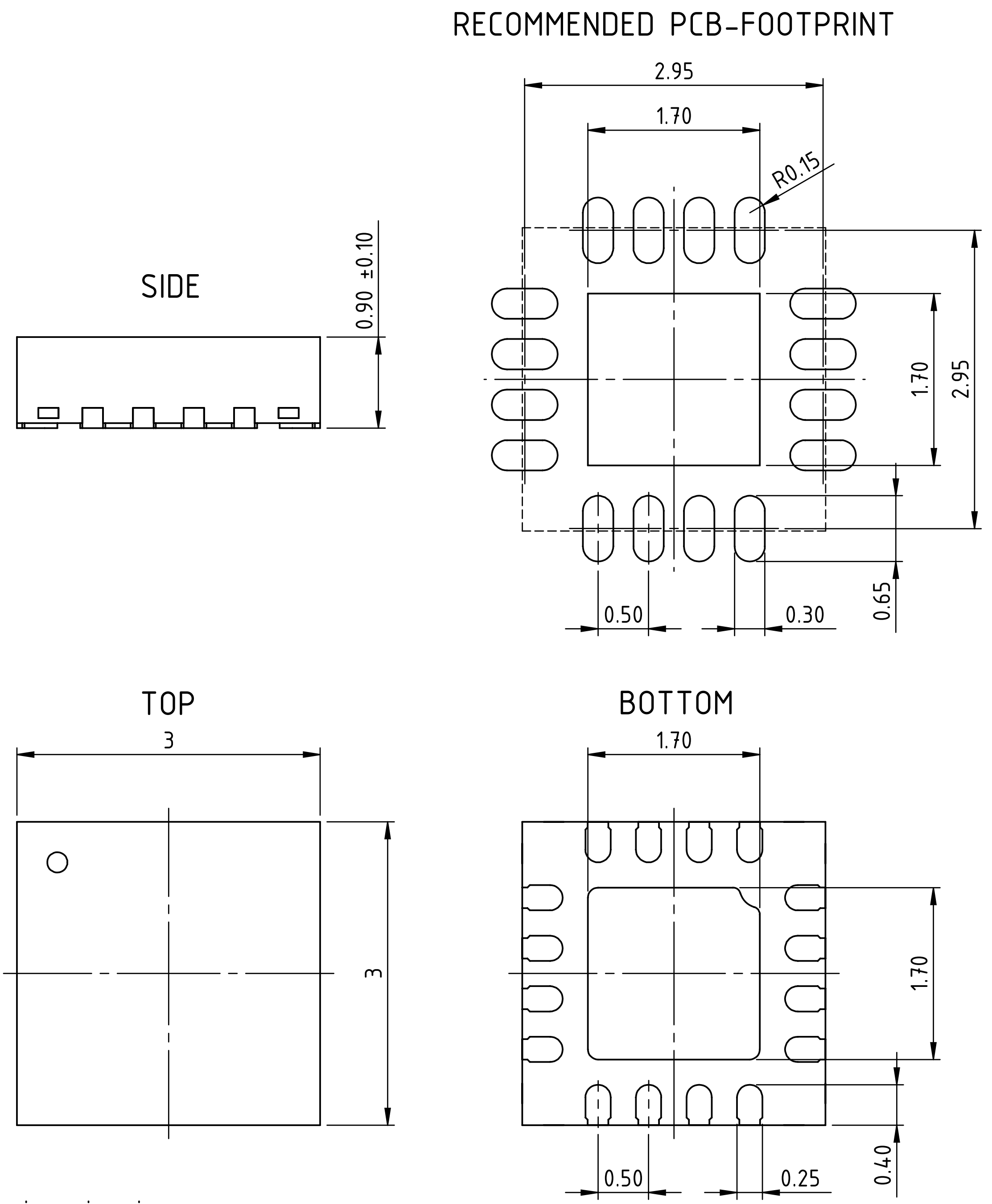


PIN FUNCTIONS

No.	Name	Function
1	MISO	SPI Serial Data Output
2	NCS	SPI Chip Select Input
3	SCLK	SPI Clock Input
4	MOSI	SPI Serial Data Input
5	IO1	Digital Port Input/Output
6	IO2	Digital Port Input/Output
7	IO3	Digital Port Input/Output
8	IO4	Digital Port Input/Output
9	IO5	Digital Port Input/Output
10	IO6	Digital Port Input/Output
11	GND	Ground
12	VDD	+3.0 V to +5.5 V Supply Voltage
13	NSLO	BiSS Data Line Output (inverted)
14	SLO	BiSS Data Line Output
15	MA	BiSS Clock Line Input
16	NMA	BiSS Clock Line Input (inverted)
	BP	Backside Paddle 1)

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS QFN16 3 mm x 3 mm x 0.9 mm



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

drb_qfn16-3x3-1_pack_1, 15:1

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V(VDD)	Voltage at VDD		-0.3	6	V
G002	V()	Voltage at MISO, NCS, SCLK, MOSI, IO1, IO2, IO3, IO4, IO5, IO6	V() < V(VDD) + 0.3 V	-0.3	6	V
G003	V()	Voltage at SLO, NSLO		-0.3	6	V
G004	V()	Voltage at MA, NMA		-10	10	V
G005	I(VDD)	Current in VDD		-100	150	mA
G006	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G007	Tj	Junction Temperature		-40	150	°C
G008	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package QFN16-3x3	-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN16-3x3 surface mounted to PCB according to JEDEC 51 thermal measurement standards		45		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD	Permissible Supply Voltage		3.0		5.5	V
002	I(VDD)	Supply Current	without load		5	8	mA
003	Vc()hi	Clamp Voltage hi at MISO, NCS, SCLK, MOSI, IO1, IO2, IO3, IO4, IO5, IO6	Vc()hi = V() - VDD; I() = 1 mA	0.4		1.5	V
004	Vc()lo	Clamp Voltage lo at MISO, NCS, SCLK, MOSI, IO1, IO2, IO3, IO4, IO5, IO6	I() = -1 mA	-1.5		-0.3	V
Field Interface: RS422 Line Driver Outputs SLO, NSLO							
201	Vs()hi	Saturation Voltage hi	Vs() = VDD - V(); I() = -20 mA			500	mV
202	Vs()lo	Saturation Voltage lo	I() = 20 mA			400	mV
203	Isc()hi	Short-circuit Current hi	V() = 0 V	-60	-30	-20	mA
204	Isc()lo	Short-circuit Current lo	V() = VDD	20	45	90	mA
Field Interface: RS422 Line Receiver MA, NMA							
210	Vin()	Permissible Input Voltage		-10		10	V
211	Vcm()	Input Common Mode Voltage		-7		7	V
212	Vdiff()	Differential Input Voltage	Vdiff() = V(MA) - V(NMA)	-12		12	V
213	Rin()	Input Resistance	MA vs. GND, NMA vs. GND	4			kΩ
214	Vt()diff	Differential Input Threshold	Vt(MA)diff = V(MA) - V(NMA)	-200		200	mV
215	Vt()hys	Differential Input Hysteresis	Vt()hys = V(MA) - V(NMA)	5	60	200	mV
216	Vt()hi	Input Threshold Voltage hi at MA	ESE = 1			70	%VDD
217	Vt()lo	Input Threshold Voltage lo at MA	ESE = 1	30			%VDD
Field Interface: Timing							
220	fclk()	Permissible Clock Frequency at MA	SSI protocol BiSS C protocol			4 10	MHz MHz
221	tr()	Rise Time hi at SLO, NSLO	RL = 100 Ω to GND, rise 10 % to 90 %			20	ns
222	tf()	Fall Time lo at SLO, NLSO	RL = 100 Ω to VDD, fall 90 % to 10 %			20	ns

223	$t_P()$	Output Propagation Delay at SLO	versus clock edge MA, ESE = 1;
			versus clock edge MA, ESE = 0;
			versus clock edge MAO via IOx;
			refers to timing Figure 1
				0
				0
				-10
						40
						75
						10
							ns
							ns
							ns

224	$t_{out}()$	Slave Timeout at SLO	adaptive (NTOA = 0);
			short (NTOA = 1, TOS = 1);
			long (NTOA = 1, TOS = 0);
				2/fosc
				
					30/fosc
					375 /fosc
						375 /fosc	

225	T_{CLK}	Period of BiSS Timeout Sampling Clock	refers to Characteristics in BiSS Interface PROTOCOL DESCRIPTION		0.75 /fosc		

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Host Interface NCS, SCLK, MOSI, MISO							
301	Vs()hi	Saturation Voltage hi at MISO	Vs() = VDD - V(); I() = -1.6 mA			0.4	V
302	Vs()lo	Saturation Voltage lo at MISO	I() = -1.6 mA			0.4	V
303	tr()	Rise Time at MISO	CL = 50pf VDD = 3.0 . . . 3.6 V, rise 10 % to 70 % VDD = 4.5 . . . 5.5 V, rise 10 % to 70 %			 35 25	 ns ns
304	tf()	Fall Time at MISO	CL = 50pf VDD = 3.0 . . . 3.6 V, fall 90 % to 0.8 V VDD = 4.5 . . . 5.5 V, fall 10 % to 0,8 V			 45 35	 ns ns
305	Vt()hi	Threshold Voltage hi at NCS, SCLK, MOSI				70	%VDD
306	Vt()lo	Threshold Voltage lo at NCS, SCLK, MOSI		30			%VDD
307	Vt()hys	Threshold Hysteresis at NCS, SCLK, MOSI		200			mV
308	Ipu()	Pull-up Current at NCS	V() = 0 V...VDD − 1 V	-70		-2	µA
309	Ipd()	Pull-down Current at SCLK, MOSI	V() = 1 V...VDD	2		80	µA
310	$t_{P1}()$	Output Propagation Delay at MISO	CL = 50pf, MISO = 0.5*VDD after SCLK hi → lo refers to timing Figure 3 VDD = 3.0 . . . 3.6 V VDD = 4.5 . . . 5.5 V			 40 25	 ns ns
Oscillator							
401	f_{osc}	Internal Oscillator Frequency		12	20	28	MHz
Power-On Reset							
501	VDDon	VDD Turn-on Threshold	increasing voltage at VDD vs. GND	1.5		2.9	V
502	VDDoff	VDD Turn-off Threshold (undervoltage reset)	decreasing voltage at VDD vs. GND	1.2		2.7	V
503	VDDhys	VDD Hysteresis	VDDhys = VDDon - VDDoff	200			mV
I/O Crossbar: IO1, IO2, IO3, IO4, IO5, IO6							
601	Vs()hi	Saturation Voltage hi	Vs() = VDD - V(); I() = -1.6 mA			0.4	V
602	Vs()lo	Saturation Voltage lo	I() = -1.6 mA			0.4	V
603	tr()	Rise Time	CL = 50pf VDD = 3.0 . . . 3.6 V, rise 10 % to 70 % VDD = 4.5 . . . 5.5 V, rise 10 % to 70 %			 35 25	 ns ns
604	tf()	Fall Time	CL = 50pf VDD = 3.0 . . . 3.6 V, fall 90 % to 0.8 V VDD = 4.5 . . . 5.5 V, fall 10 % to 0,8 V			 45 35	 ns ns
605	Vt()hi	Threshold Voltage hi				70	%VDD
606	Vt()lo	Threshold Voltage lo		30			%VDD
607	Vt()hys	Threshold Hysteresis		200			mV
608	Ipd()	Pull-down Current	V() = 1 V...VDD	2		80	µA

OPERATING REQUIREMENTS: Field Interface BiSS

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	t_{frame}	Permissible Frame Repetition		*	indefinite	
I002	t_{busy}	Processing Time w/o Start Bit Delay		$2 \cdot t_C$		
I003	t_C	Permissible Clock Period		90		ns
I004	t_{L1}	Clock Signal hi Level Duration		45	t_{out}	ns
I005	t_{L2}	Clock Signal lo Level Duration		45	t_{out}	ns
I006	t_P	Output Propagation Delay		refer to Elec. Char. 223		
I007	t_{out}	Slave Timeout at SLO	depending on NTOA and TOS	refer to Elec. Char. 224		

*Allow t_{out} to elapse.

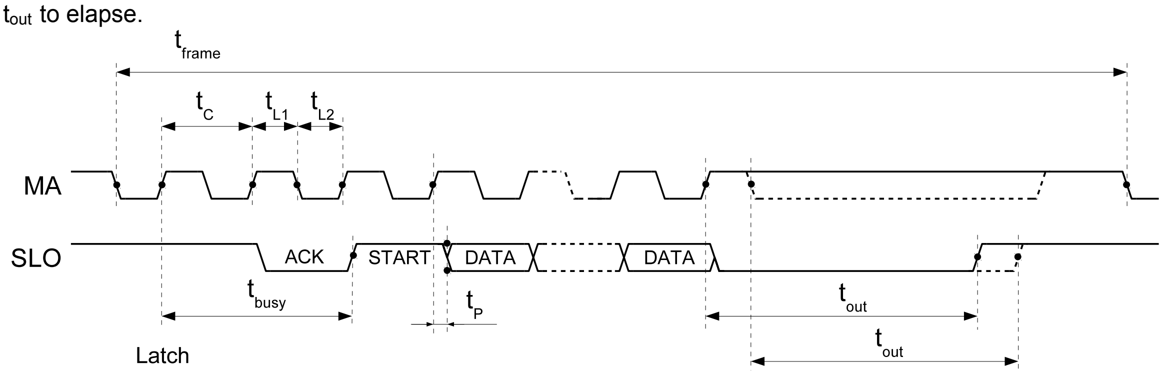


Figure 1: BiSS Protocol Timing

OPERATING REQUIREMENTS: Field Interface SSI

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	t_{frame}	Permissible Frame Repetition		*	indefinite	
I102	t_C	Permissible Clock Period		200		ns
I103	t_{L1}	Clock Signal hi Level Duration		45	t_{out}	ns
I104	t_{L2}	Clock Signal lo Level Duration		45	t_{out}	ns
I105	t_{RQ}	REQ Signal lo Level Duration		45	t_{out}	ns
I106	t_P	Output Propagation Delay		refer to Elec. Char. 223		
I107	t_{out}	Slave Timeout at SLO	depending on TOS	refer to Elec. Char. 224		

*Allow t_{out} to elapse.

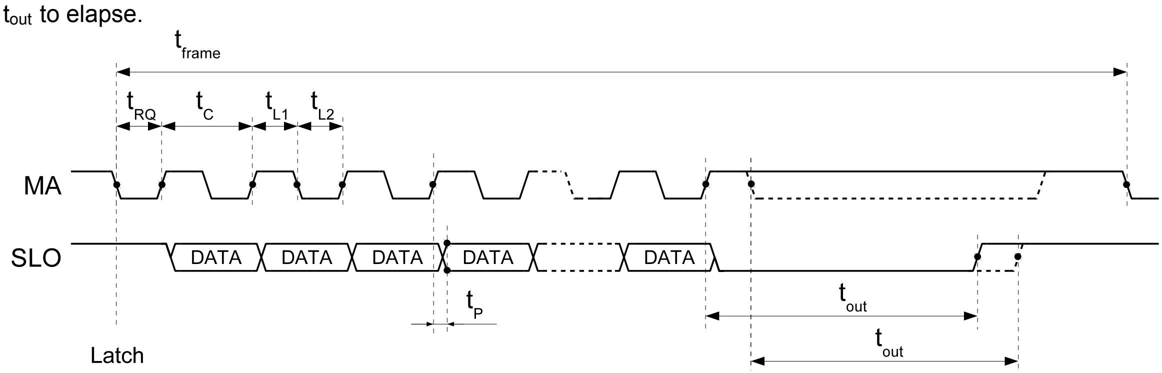


Figure 2: SSI Protocol Timing

OPERATING REQUIREMENTS: Host Interface SPI Slave

Operating Conditions: VDD = 3.0 . . . 5.5 V, T_j = -40 . . . 125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I201	t_{C1}	Permissible Clock Cycle Time		50		ns
I202	t_{L1}	Clock Signal lo Level Duration		25		ns
I203	t_{L2}	Clock Signal hi Level Duration		25		ns
I204	t_{H1}	Hold Time: NCS lo after SCLK lo → hi		50		ns
I205	t_{H2}	Hold Time: MOSI stable after SCLK lo → hi		20		ns
I206	t_{S1}	Setup Time: NCS lo before SCLK lo → hi		25		ns
I207	t_{S2}	Setup Time: MOSI stable before SCLK lo → hi		20		ns
I208	t_{P1}	Propagation Delay: MISO stable after SCLK hi → lo		refer to Elec. Char. 310		
I209	t_{P2}	Propagation Delay: MISO hi impedance after NCS lo → hi			50	ns
I210	t_W	Wait Time: between NCS lo → hi and NCS hi → lo		250		ns

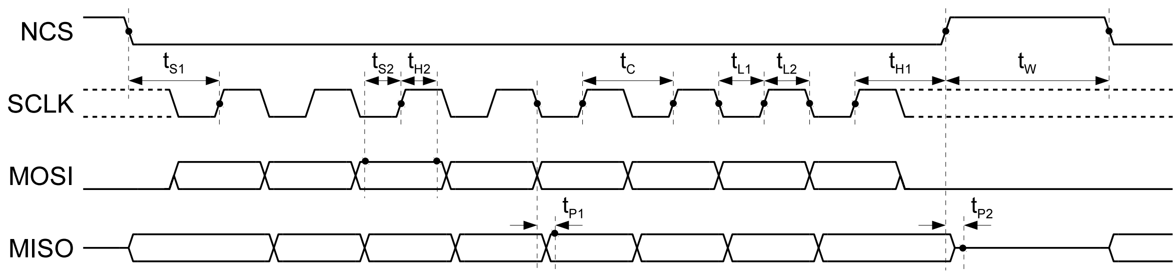


Figure 3: SPI Protocol Timing

CONFIGURATION PARAMETERS

STARTUP AND OPERATION .... Page 12

CHPREL:	Chip release
CFGOK:	Tag configuration data as valid
ACQMODE:	Acquisition mode
BANKSW:	Bank switch
USDST:	Activity on missing sensor data

FIELD INTERFACE: General .... Page 13

ESE:	Enable single-ended operation

FIELD INTERFACE: BiSS .... Page 13

BUSY:	Minimum start bit delay
DLEN1:	Data length SCD 1
ENDC1:	Enable data channel 1
CPOLY1:	CRC polynomial data channel 1
CSTART1:	CRC start value for data channel 1
DLEN2:	Data length SCD 2
ENDC2:	Enable data channel 2
CPOLY2:	CRC polynomial data channel 2
CSTART2:	CRC start value for data channel 2
ASID:	Request an additional Slave ID
CMD01DI:	BiSS Command 0/1 Control
CMD2EN:	BiSS Command 2 Control
REGPROT:	Enable register protection

FIELD INTERFACE: SSI .... Page 16

ENSSI:	Protocol selection
NTOA:	Disable adaptive timeout
TOS:	Shorten timeout sensor data
GRAY1:	Binary to Gray conversion
RSSI:	SSI ring operation

HOST INTERFACE: SPI SLAVE .... Page 17

CVALID:	Control valid indication
IVALID:	Valid indication for BiSS commands
CONFIRM:	Confirmation for BiSS register access
RDATA:	Register access transfer byte

FAST SENSOR INTERFACE: SPI MASTER Page 25

ENFSI:	Enable Fast Sensor Interface
DLFSI:	Data length Fast Sensor Interface
HEADL:	SPI request header length
STAFSI:	Observe start bit from sensor
IDLE:	Idle state at MOSI
CPOL:	SPI communication protocol polarity
CPHA:	SPI communication protocol phase
CLKDIV:	SPI clock divider
HEADER:	SPI request header
G2B:	Gray to binary conversion for sensor data
REQ_FT:	BiSS request feedthrough
OSCDIV2:	Oscillator Frequency divide by 2

I/O CROSSBAR .... Page 27

CB_FSI:	Configuration Fast Sensor Interface
CB_CLK:	Input for external clock oscillator
CB_IRQ:	Interrupt request output
CB_MAO:	BiSS MA clock output
CB_SLI:	BiSS Slave input SLI
CB_SLO:	BiSS Slave output SLO
CMD2EN:	BiSS Command controlled pin BK

REGISTER MAP: CONFIG RAM

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIELD INTERFACE								
0x0	GRAY1	ENDC1	DLEN1(5:0)					
0x1	CSTART1(5:0)						CPOLY1(1:0)	
0x2	0	ENDC2	DLEN2(5:0)					
0x3	CSTART2(5:0)						CPOLY2(1:0)	
0x4	BUSY(7:0)							
0x5	RSSI	ENSSI	CMD2EN	CMD01DI	ASID	TOS	NTOA	REGPROT
OPERATION								
0x6	0	0	0	0	0	USDST [1]	BANKSW	ACQMODE
FAST SENSOR INTERFACE								
0x7	OSCDIV2 [2]	ENFSI	DLFSI(5:0)					
0x8	0	IDLE	STAFSI(1:0)		HEADL(3:0)			
0x9	CLKDIV(3:0)				G2B	REQ_FT	CPHA	CPOL
0xA	HEADER(7:0)							
RESERVED								
0xB	0	0	0	0	0	0	0	0
CROSSBAR								
0xC	CB_SLO	CB_SLI	CB_MAO	CB_IRQ	CB_CLK	CB_FSI(2:0)		
STARTUP								
0xD	CFGOK	0	ESE	0	CHPREL(3:0)			
BiSS CONTROL COMMUNICATION								
0xE	RDATA(7:0)							
0xF	0	0	0	CONFIRM [1]	IVALID [1]	CVALID(2:0)		
Notes								
The address offset is 0x60 for BiSS and 0x40 for SPI access.								
[1] Not implemented before chip revision Z.								
[2] Not implemented from chip revision Z.								

Table 7: Register layout

STARTUP AND OPERATION

Startup

After power on the configuration RAM is initialized with zero and must be programmed through the host (SPI) or the field (BiSS) interface. The chip release can be verified with the ROM value CHPREL. After the configuration phase, which will end by setting the parameter CFGOK, the device is ready for BiSS respectively SSI access. While CFGOK is zero, the data output SLO remains high to allow error detection in the SSI output format; the device listens to a write access via BiSS.

CHPREL	Addr. 0xD; bit 3:0 R
0x0	iC-MCB
0x1	Reserved
0x2	iC-MCB 2
0x3	iC-MCB 3
0x4	iC-MCB Z
0x5 ... 0xF	Reserved

Table 8: Chip release

CFGOK	Addr. 0xD; bit 7 R/W 0
0	Configuration data invalid, SLO remains high
1	Configuration data valid

Table 9: Tag configuration data as valid

Operation

The iC-MCB provides sensor data after receiving the request from the BiSS Interface. Therefore, two interfaces are implemented to import sensor data to the Data RAM.

- SPI master: The iC-MCB is active and uses a SPI master as a Fast Sensor Interface to load sensor data from an external serial sensor. The interface is enabled with ENFSI. Detailed information can be found in chapter FAST SENSOR INTERFACE: SPI MASTER on page 25.
- SPI slave: The iC-MCB is passive and receives sensor data from a microprocessor using the host interface. Further details are described in chapter HOST INTERFACE: SPI SLAVE on page 17.

The operating sequence is shown in Figure 4. After a BiSS request the sensor data must be placed in the Data RAM. The following data transmission starts after a configurable delay to allow subsequent BiSS slaves to calculate their sensor data (see parameter BUSY). Unlike to the loading of sensor data via the Fast Sensor Interface, which starts always isochronic to the BiSS request, the microprocessors has two acquisition options.

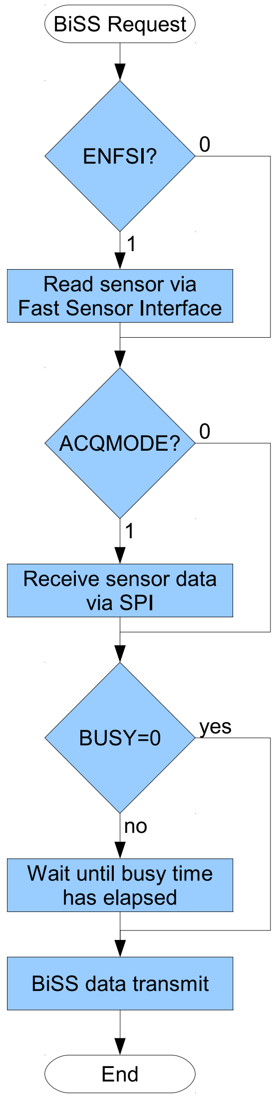


Figure 4: Sequence diagram

In the Request mode (ACQMODE = 1), the iC-MCB waits after signalizing the request with IRQ (see CB_IRQ at page 27) until sensor data is written with a particular SPI command (Transmit SDAD) into the 64 byte Data RAM. In the meantime the incomming data at SLI will also be stored in the Data RAM. If an overflow of the Data RAM is pending, waiting for sensor data is cancelled and zero data will be send to prevent loosing data from previous BiSS slaves.

ACQMODE	Addr. 0x6; bit 0 R/W 0
0	No delay
1	Request

Table 10: Acquisition mode

In the Nodelay mode (ACQMODE = 0) the sensor data are written into the Data RAM independently and asynchronously to the BiSS frames. In the BiSS frame the lately stored sensor data are used and sent without any additional delay. In this mode it is necessary to enable the bank switch with the parameter BANKSW, which separates the Data RAM into four banks with 16 bytes each.

BANKSW	Addr. 0x6; bit 1 R/W 0
0	Bank switch disabled
1	Bank switch enabled (three banks)

Table 11: Bank switch

Three banks are written alternately by the microcontroller, the iC-MCB manages the bank selection, and the fourth is used to temporarily store the current send data. If no new sensordata are written by the microcontroller since the last BiSS frame, the parameter USDST configures, if the same sensor data are used several times or if the sensor data are marked as invalid by sending zero data.

USDST	Addr. 0x6; bit 2 R/W 0
0	Send zero data
1	Use sensor data several times
Note	USDST is not implemented before chip revision Z.

Table 12: Activity on missing sensor data

Note: The activity on missing sensordata is not defined before chip revision Z.

Table 13 shows the arrangement in the Data RAM if BANKSW is set.

Data RAM	R/W 0
0x00 . . . 0x0F	Bank 0
0x10 . . . 0x1F	Bank 1
0x20 . . . 0x2F	Bank 2
0x30 . . . 0x3F	Temporary buffer for send data

Table 13: Data RAM arrangement (bank switch enabled)

FIELD INTERFACE: General

Line transceiver

iC-MCB provides one RS422 line receiver for the clock input MA and one current limited RS422 driver for the data output SLO. The line receiver includes internal resistors to allow a common mode voltage range of -7 V to +7 V. A single ended TTL mode for MA can be selected with the parameter ESE.

ESE	Addr. 0xD; bit 5 R/W 0
0	Differential ended operation at MA, NMA
1	Single-ended operation at MA

Table 14: Enable single ended operation

FIELD INTERFACE: BiSS

The BiSS Interface is a serial, bidirectional interface which is used to transmit process data and to parameterize the device. For a detailed description of the protocol refer to the BiSS Interface website http://www.ichaus.de/BiSS_interface.

The BiSS frame

A BiSS frame is used to interchange process data between master and slave and to transmit one bit in each direction for the control communication. Process data is distinguished into sensor data, which is transferred from slave to master, and actuator data for the opposite direction. The iC-MCB signalizes the start of each frame with IRQ at the first rising edge of MA. This moment is defined in BiSS as the latch point. Now the iC-MCB waits for sensor data (ACQMODE = 1), which must be provided via SPI with the command Transmit SDAD (sensor and actuator data access). After that the start bit is generated when the configurable busy counter BUSYCNT (configured by BUSY) has expired, otherwise the start bit is delayed with the configurable time measured from the latch point.

BUSY	Addr. 0x4; bit 7:0	R/W 0
	before chip release Z	from chip release Z
0x00	No additional delay	
0x01	1 (50 ns)	4 (200 ns)
0x02 . . . 0xFE	2 (100 ns) . . . 254 (12.7 us)	8 (400 ns) . . . 1016 (50.8 us)
0xFF	255 (12.75 us)	1020 (51 us)

Table 15: Minimum start bit delay in clocks f_{OSC}

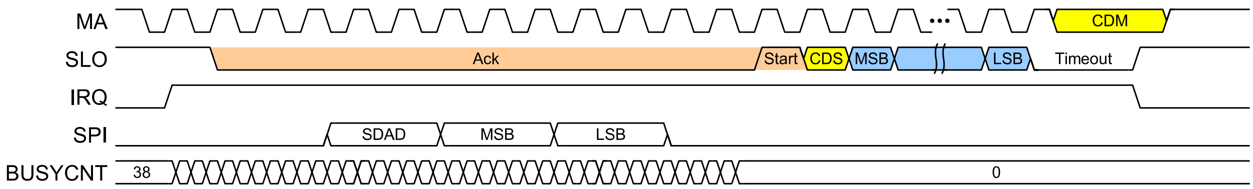


Figure 5: Start bit delay in BiSS frame

The process data consists of several logical data channels. Each channel has a programmable data length (DLEN1, DLEN2) and CRC to increase the transmission safety. The generator polynomial (CPOLY1, CPOLY2) and the start value for CRC calculation (CSTART1, CSTART1) is programmable too. ENDC1 and ENDC2 enable the corresponding data channel. With the BiSS protocol two channels can be configured in iC-MCB.

DLEN1	Addr. 0x0; bit 5:0 R/W 0
0x00	1 bit
...	(DLEN1 + 1) bit
0x3F	64 bit

Table 16: Data length channel 1

ENDC1	Addr. 0x0; bit 6 R/W 0
0	Data channel 1 disabled
1	Data channel 1 enabled

Table 17: Enable data channel 1

CPOLY1	Addr. 0x1; bit 1:0 R/W 0
0x0	no CRC generated (0 bit CRC)
0x1	CRC polynomial = 0x25 (5 bit CRC)
0x2	CRC polynomial = 0x43 (6 bit CRC)
0x3	CRC polynomial = 0x190D9 (16 bit CRC)

Table 18: CRC polynomial data channel 1

CSTART1	Addr. 0x1; bit 7:2 R/W 0
0x00 . . . 0x3F	Start value for CRC calculation

Table 19: CRC start value for data channel 1

DLEN2	Addr. 0x2; bit 5:0 R/W 0
0x00	1 bit
...	(DLEN2 + 1) bit
0x3F	64 bit

Table 20: Data length channel 2

ENDC2	Addr. 0x2; bit 6 R/W 0
0	Data channel 2 disabled: data channel length 0 bit
1	Data channel 2 enabled (condition: ENDC1 = 1)

Table 21: Enable data channel 2

CPOLY2	Addr. 0x3; bit 1:0 R/W 0
0x0	no CRC2 generated (0 bit CRC)
0x1	CRC2 polynomial = 0x25 (5 bit CRC)
0x2	CRC2 polynomial = 0x43 (6 bit CRC)
0x3	CRC2 polynomial = 0x190D9 (16 bit CRC)

Table 22: CRC polynomial data channel 2

CSTART2	Addr. 0x3; bit 7:2 R/W 0
0x00 . . . 0x3F	Start value for CRC calculation

Table 23: CRC start value for data channel 2

BiSS timeout

The (automatic) BiSS timeout adaption (refer to www.biss-interface.com) is based on the BiSS MA clock period T_{MA} and the device specific internal sampling frequency $1/T_{CLK}$.

The iC-MCB measures the 1.5 periods (from the first falling to the second rising edge) of MA each frame and calculates an adaptive timeout with $T_{CLK} = \frac{4}{3 * fosc}$ (see El. Char., 401).

Symbol	Condition	Min.	Max.
timeout	$T_{CLK} \leq 1.5 * T_{MA}$	$1.5 * T_{MA}$	$1.5 * T_{MA} + 3.0 * T_{CLK}$
	$T_{CLK} \geq 1.5 * T_{MA}$	$1.0 * T_{CLK}$	$1.5 * T_{MA} + 3.0 * T_{CLK}$

Table 24: Adaptive BiSS timeout

Note:
Using parameters NTOA and TOS (described in chapter FIELD INTERFACE:SSI) may be considered for a constant long BiSS timeout (approx. 20 µs) or constant short BiSS timeout (approx. 2 µs) as well.

The control frame

The iC-MCB manages a dedicated set of BiSS commands and registers automatically. The number of occupied slave IDs is equal to the number of enabled data channels, but can be increased by one using ASID. If CFGOK is not set or if the SSI protocol is enabled, the control frame will be executed without evaluating the slave ID. A register overview is shown in Table 25.

Addr.	Name	Size	Managed by
0x00 .. 0x3F	Register bank	64 bytes	Host
0x40	Bank selection	0..8 bits (1 byte)	Host
0x41	EDS bank	0..8 bits (1 byte)	Host
0x42 .. 0x43	Profile ID	16 bits (2 bytes)	Host
0x44 .. 0x47	Serial number	32 bits (4 byte)	Host
0x48 .. 0x5F	Slave register	23 bytes	Host
0x60 .. 0x6F	Config RAM	16 bytes	iC-MCB
0x70 .. 0x73	Slave register (Recommended: Status)	4 bytes	Host
0x74 .. 0x77	Slave register (Recommended: Command)	4 bytes	Host
0x78 .. 0x7D	Device ID	48 bits (6 bytes)	Host
0x7E .. 0x7F	Manufacturer ID	16 bits (2 bytes)	Host

Table 25: BiSS Register Assignment

ASID	Addr. 0x5; bit 3 R/W 0
0	0 (condition ENDC1 = 0, ENDC2 = 0)
	1 (condition ENDC1 = 1, ENDC2 = 0)
	2 (condition ENDC1 = 1, ENDC2 = 1)
1	1 (condition ENDC1 = 0, ENDC2 = 0)
	2 (condition ENDC1 = 1, ENDC2 = 0)
	3 (condition ENDC1 = 1, ENDC2 = 1)

Table 26: Number of occupied Slave IDs

The BiSS commands with the codes 0 and 1 are managed by iC-MCB, but they can be disabled per configuration bit CMD01DI.

CMD01DI	Addr. 0x5; bit 4 R/W 0
0	Enable BiSS commands 0 and 1
1	Disable BiSS commands 0 and 1

Table 27: BiSS Command 0/1 Control

Bit CMD2EN configures if the BiSS command with the opcode 2 is managed by the iC-MCB or by the host. In iC-MCB the command opcode 2 is used to switch an IO port, e.g. for controlling a bus coupler.

CMD2EN	Addr. 0x5; bit 5 R/W 0
0	BiSS command 2 managed by host
1	BiSS command 2 enabled (control BK at IOx)

Table 28: BiSS Command 2 Control

The BiSS access to the Config RAM uses the register addresses 0x60 to 0x6F. The access is denied when REGPROT is set.

REGPROT	Addr. 0x5; bit 0 R/W 0
0	BiSS access to Config RAM allowed
1	BiSS access to Config RAM denied

Table 29: Register protection

All other BiSS commands and register accesses need to be handled by the host.

FIELD INTERFACE: SSI

The interface uses the SSI protocol when ENSSI is set.

ENSSI	Addr. 0x5; bit 6	R/W 0
0	BiSS C protocol	
1	SSI protocol	

Table 30: Protocol selection

The SSI frame

As the SSI protocol does not support the delayed transmission of sensor data, the data must already be stored in the RAM when the SSI frame starts (ACQMODE = 0). Therefore the data RAM in iC-MCB can be divided into three banks (BANKSW). The banks are automatically switched after writing into the data RAM with the SPI command Transmit SDAD. Fig. 6 shows the active RAM bank with BANKSEL.

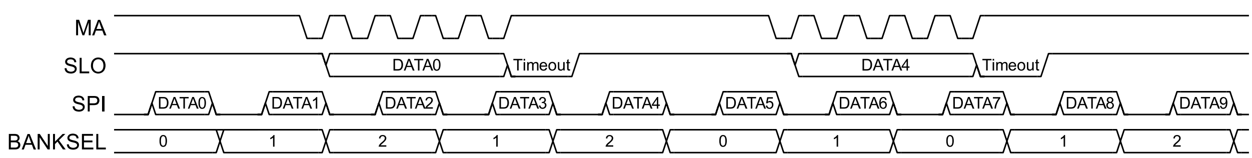


Figure 6: SSI frame

Serial timeout

For SSI operation the adaptive timeout is not recommended. A fixed timeout is enabled with NTOA with a length selected by TOS.

NTOA	Addr. 0x5; bit 1	R/W 0
0	Adaptive timeout enabled (TOS configuration not relevant)	
1	Adaptive timeout disabled (TOS configuration relevant)	

Table 31: Adaptive timeout

TOS	Addr. 0x5; bit 2	R/W 0
0	Long timeout (approx. 20 µs)	
1	Short timeout (approx. 2 µs)	

Table 32: Serial timeout

Data format

A binary to Gray conversion can be enabled with GRAY1. With the SSI protocol two channels can be configured in iC-MCB to separate GRAY coded content in data channel 1 and following non GRAY coded content in data channel 2. If the data contains additional SSI data bits which shall not be converted to gray code, those additional bits can be placed in the data channel 2.

GRAY1	Addr. 0x0; bit 7	R/W 0
0	No data conversion	
1	Binary to Gray conversion	

Table 33: SSI data format

Ring operation

The ring operation, which is selected with RSSI, defines a ring buffer with the data channel 1. In ring operation the data channel 2 can be used to define one or more bits, e.g. one stop bit, to separate the repetition.

RSSI	Addr. 0x5; bit 7	R/W 0
0	Ring operation disabled	
1	Ring operation enabled	

Table 34: Ring operation

Note: The fixed short or long timeout can also be used with the BiSS protocol.

HOST INTERFACE: SPI SLAVE

The iC-MCB uses 8 bit wide SPI with phase and polarity = 0, or phase and polarity = 1.

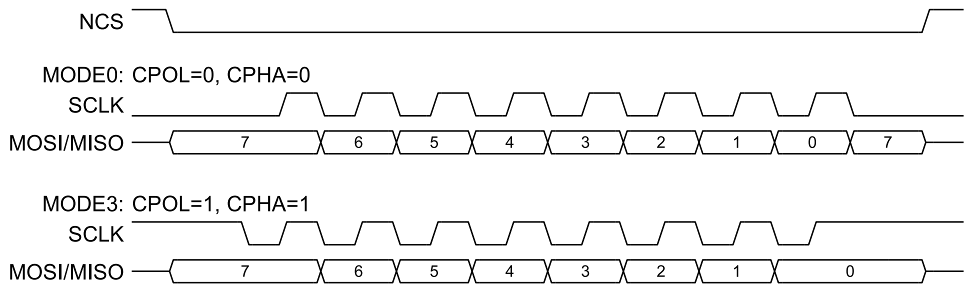


Figure 7: SPI: timing, phase and polarity

The host uses the SPI interface to configure iC-MCB, to write sensor data to iC-MCB and to read actuator data from iC-MCB.

Table 35 shows the register assignment for the SPI access.

Addr.	Name	Size	Access direction
0x00 .. 0x3F	Data RAM	64 bytes	R/W
0x40 .. 0x4F	Config RAM	16 bytes	R/W

Table 35: Table of register assignment

The SPI Frame
Each SPI frame starts with one byte OPCODE sent from the host via MOSI and one byte STATUS sent from iC-MCB via MISO.

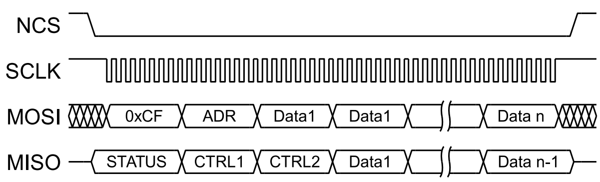


Figure 8: SPI frame example with OPCODE(0xCF), STATUS, CTRL1 and CTRL2

SPI Opcodes

OPCODE	
Code	Description
0xA6	Transmit SDAD
0x81	Read Register
0xCF	Write Register
0xE3	Sensor Feedthrough

Table 36: SPI Opcodes

All bytes after the first STATUS byte sent from iC-MCB via MISO depend on the SPI OPCODE and may contain additional BiSS Control Communication Data CTRL1 and CTRL2 or related device data.

STATUS								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SPI_ERR	NCS_ERR	IRQ	STB	CTO(3:2)		PACTIVE(1:0)	

Table 37: STATUS Byte (returned during SPI access)

PACTIVE	bit 1:0	R
0x0	All BiSS data channel deactivated	
0x1	BiSS data channel 1 activated	
0x2	BiSS data channel 2 activated	
0x3	BiSS data channel 1 + 2 activated	

Table 38: Process data channel active/inactive

The PACTIVE status indicates the host that BiSS commands have activated or deactivated individual BiSS data channels. PACTIVE is not affected by ENDC1 or ENDC2.

CTO	bit 3:2	R
0x0	No control Communication running	
0x1	BiSS Command Access	
0x2	BiSS Read register access	
0x3	BiSS Write register access	

Table 39: BiSS Control Communication

A running BiSS Control Communication is indicated with CTO $\neq 0$. It should be read every BiSS frame.

STB	bit 4	R
0	No action pending	
1	Register access or command execution must be confirmed by host	

Table 40: Strobe for read/write register access and command execution

With STB iC-MCB indicates that the host has to confirm the validity of a pending BiSS Command or Register Access request.

IRQ	bit 5	R
0	No interrupt request	
1	Interrupt request active	

Table 41: Interrupt request line/signal

Bit IRQ signals an active interrupt request. Its value can also be output at the I/O crossbar if enabled. Details are available in chapter I/O CROSSBAR on page .

NCS_ERR	bit 6	R
0	No NCS error	
1	NCS pulse too short. Last SPI access not finished.	

Table 42: Frame separation error

If the pulse on the chip select line NCS is too short, an error is indicated with NCS_ERR.

SPI_ERR	bit 7	R
0	No SPI error	
1	SPI error detected. Possible reasons are: • Invalid SPI OPCODE • Register access to an address which is not implemented	

Table 43: SPI Error

SPI Opcode: Transmit SDAD

To transmit sensor data to iC-MCB and actuator data from iC-MCB the SPI OPCODE 0xA6 is used. Following the opcode the Single-Cycle Data (SCDATA) is exchanged as shown in 9.

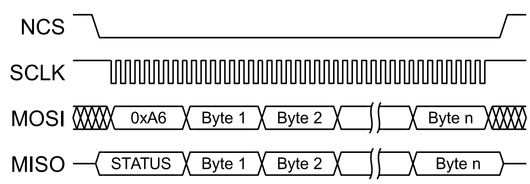


Figure 9: SPI: sensor and actuator data access (SDAD)

Within the Data RAM the SCDATA is arranged big-endian, i.e. with the highest-value byte at the lowest-value address. The MSB of data channel 1 is at address 0x00 and the LSB is always at bit position zero. The data for channel 2 starts at the next higher address following the memory area of data channel 1. The maximum data length is 8 byte per channel. Table 44 shows an example of data arrangement with 14 bit SCDATA length for channel 1 and 26 bit SCDATA2 length for channel 2 in the Data RAM. An access to the Data RAM during the BiSS frame is permitted if it is partitioned into multiple banks using BANKSW).

i SDAD access to the configuration RAM (0x40 ...0x4F) results in an SPI_ERR which will be sent in the STATUS during the next SPI frame.

Data RAM								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCD 1								
0x00	-	-	SCDATA1(13:8)					
0x01	SCDATA1(7:0)							
SCD 2								
0x02	-	-	-	-	-	-	SCDATA2(25:24)	
0x03	SCDATA2(23:16)							
0x04	SCDATA2(15:8)							
0x05	SCDATA2(7:0)							
0x06 ...0x3F	Unused in this example							

Table 44: Data RAM assignment (example)

SPI Opcode: Read Register
To read iC-MCB's registers the OPCODE 0x81 is sent via MOSI and followed by the address of the desired register. After the STATUS byte iC-MCB sends two additional control bytes CTRL1 and CTRL2 via MISO. The requested register data is sent in byte 4. Multiple consecutive bytes can be read during one read access. The register data stream on MISO is then extended and the address is incremented by one automatically.

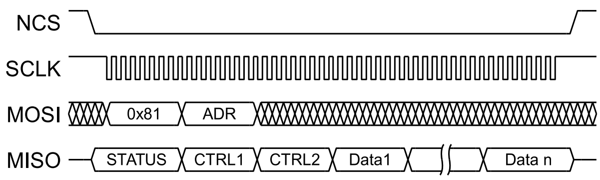


Figure 10: SPI: read register

SPI Opcode: Write Register
To write iC-MCB's registers the OPCODE 0xCF is sent followed by the address and the desired content of one or multiple consecutive registers via MOSI. After the STATUS byte iC-MCB sends two additional control bytes CTRL1 and CTRL2 via MISO. The transmitted register data is returned beginning in byte 4.

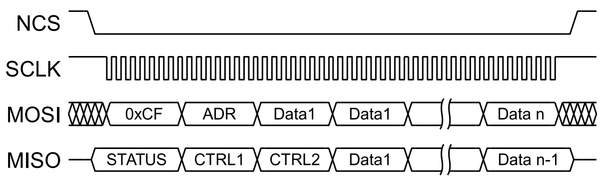


Figure 11: SPI: write register

Register access to an address above 0x4F results in an SPI_ERR which will be sent in the STATUS during the next SPI frame.

SPI Opcode: Sensor Feedthrough
To configure an SPI slave sensor that is connected to the Fast Sensor Interface the iC-MCB permits a Sensor Feedthrough to enable a direct communication between the host and a sensor. This connection to the fast sensor interface is enabled by the leading OPCODE 0xE3. The lines NCS, SCLK, MOSI and MISO are connected to the IOs after evaluating the opcode.

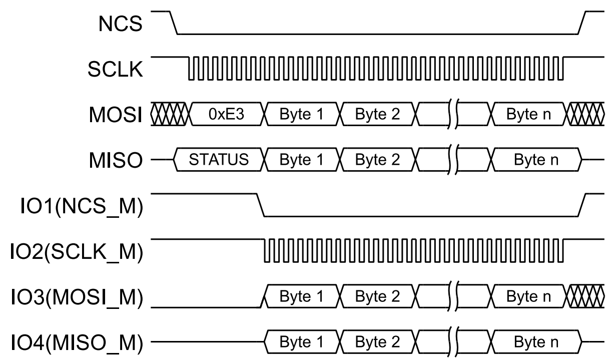


Figure 12: SPI: Sensor Feedthrough

If a BiSS request occurs while a Sensor Feedthrough operation is running, the data sent via BiSS is zero.

BiSS Control Communication
The basics of the BiSS control communication (BiSS Commands and Register Communication) are managed by iC-MCB. This includes receiving CDM, sending CDS, Slave ID assignment, addressing, processing time request and CRC calculation. The host has to support the iC-MCB in some commands and most register accesses.

To this end STATUS, CTRL1 and CTRL2 are sent by iC-MCB via MISO during a register access via SPI.

i iC-MCB sends its information for the Control Communication via STATUS, CTRL1 and CTRL2 while the host uses parameters RDATA, CVALID, CONFIRM and IVALID in register addresss 0xE and 0xF.

CTRL1								
Cond.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTO = 0	0	0	0	0	0	0	0	0
CTO = 1	IDSDC(7:0)							
CTO > 1	0	ADR(6:0)						

Table 45: Control word 1 (returned during SPI access)

CTRL2								
Cond.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTO = 0	0	0	0	0	0	0	0	0
CTO = 1	0	0	0	0	0	BROADC	CMD(1:0)	
CTO > 1	0	0	0	0	0	SIDDC(2:0)		

Table 46: Control word 2 (returned during SPI access)

CVALID(2:0)	Addr. 0xF; bit 2:0 R/W 0
0x0	Address or opcode not valid
0x1	Current address for BiSS Read Register Access is valid
0x2	Current address for BiSS Write Register Access is valid
0x3	Current address for BiSS Read Register Access and BiSS Write Register Access request is valid
0x4	BiSS Command OPCODE is valid
0x5	Confirming RDATA was read/ written or BiSS Command execution was successful
0x6	Current and next address for BiSS Write Register Access request are valid
0x7	Current address for BiSS Read Register Access request is valid. Additionally, current and next address for BiSS Write Register Access requests are valid

Table 47: Control valid indication

BiSS Command execution
The BiSS Command execution is indicated by iC-MCB with CTO = 0x1. Within the next four BiSS frames the host should read CTRL1 and CTRL2 which contain the mapped slave ID for BiSS Commands IDSDC, the BiSS Command CMD and the addressing BROADC and must permit (set CVALID = 0x4) or deny (set CVALID = 0x0) the BiSS Command, if the command is host managed (see CMD2EN). If the microcontroller is not able to set CVALID within four BiSS frames, the parameter IVALID can be used to permit all commands independently of BiSS CMD, BROADC and IDSDC. When iC-MCB sets STB = 1 the BiSS Command CMD must be executed and confirmed with CVALID = 0x5 as shown in Figure 13.

iC-MCB automatically maps the received slave ID to the enabled data channels ENDC1, ENDC2 and ASID. The mapped BiSS slave ID for BiSS commands IDSDC is sent via MISO with the CTRL1 byte.For example, if only one data channel is enabled (ENDC1 = 1, ENDC2 = 0 and ASID = 0 and iC-MCB is used in a Point-To-Point configuration, the BiSS Profile ID of channel 1 can be read via BiSS Control Communication with the slave ID = 0. If the iC-MCB is used in a Bus configuration with one slave connected to SLI and both process data channel enabled (ENDC1 = 1, ENDC2 = 1 and ASID = 0), the properties of channel 1 can be accessed via the Slave ID 2 and of channel 2 via Slave ID 1. In Table 50 the token DC1 and DC2 is used for addressing the single-cycle data channel 1 resp. 2 and DC0 is used for the additional slave ID enabled with ASID.

CMD	bit 1:0	R
0x0 . . . 0x3	BiSS Command	

Table 48: BiSS Command

BROADC	bit 2	R
0	BiSS Command is addressed	
1	BiSS Command is broadcast	

Table 49: Broadcast

IDSDC	bit 7:0	R
0x00	No DC is addressed with the BiSS command CMD	
0x01	DC1 is addressed (condition: ENDC1 = 1)	
0x02	DC2 is addressed (condition: ENDC2 = 1)	
0x03	DC1 and DC2 are addressed (condition: ENDC1 = 1, ENDC2 = 1)	
0x04	DC0 is addressed (condition: ASID = 1)	
0x05	DC1 and DC0 are addressed (condition: ENDC1 = 1), ASID = 1)	
0x06	DC2 and DC0 are addressed (condition: ENDC2 = 1), ASID = 1)	
0x07	DC1, DC2 and DC0 are addressed (condition: ENDC1 = 1, ENDC2 = 1, ASID = 1))	
0x08 . . . 0xFF	not used	

Table 50: Slave ID for BiSS command (mapped)

IVALID	Addr. 0xF; bit 3	R/W 0
0	Validity of BiSS command CMD is set individually by CVALID	
1	All BiSS commands CMD are valid	
Note	IVALID is not implemented before chip revision Z.	

Table 51: Validity of BiSS commands

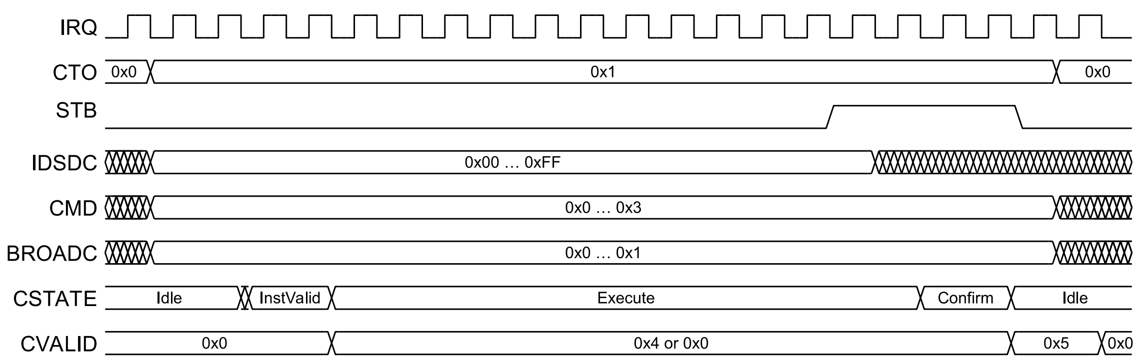


Figure 13: Command via BiSS

BiSS Read Register Access

The register read access starts with CTO = 0x2. Within the next four BiSS frames the host must read CTRL1 and CTRL2 which contain the register address ADR and the mapped slave ID for BiSS Register Access SIDDC and must determine if the address is valid for access. Just like IDSDC the slave ID SIDDC is also mapped to the internal ID range. If reading of the current address is allowed, the host sets CVALID = 0x1. With STB = 1 the register data should be written to RDATA and confirmed with CVALID = 0x5. This can be done in a single SPI Write frame. For BiSS Read Register Access of multiple registers the same procedure follows for the next bytes as shown in Figure 14.

ADR	bit 6:0	R
0x00 . . . 0x7F	BiSS slave register access address	

Table 52: BiSS register address

SIDDC	bit 2:0	R
0x0	DC1 is addressed (condition ENDC1 = 1)	
0x1	DC2 is addressed (condition ENDC2 = 1)	
0x2	DC0 is addressed (condition ASID = 1)	
0x3	not used	

Table 53: Slave ID for BiSS register access (mapped)

If the microcontroller is not able to set CVALID within four BiSS frames, the parameter CONFIRM can be used to confirm STB and CVALID can be set independently of register address ADR and SIDDC after bank switch.

CONFIRM	Addr. 0xF; bit 4 R/W 0
0	Register access not confirmed
1	Register access confirmed
Note	CONFIRM is not implemented before chip revision Z.

Table 54: Confirming BiSS register Access

The parameter RDATA in SPI register 0x4E is used for data exchange during both a BiSS Read Register Access and BiSS Write Register Access.

RDATA(7:0	Addr. 0xE; bit 7:0 R/W 0
0x00 . . . 0xFF	Any data value for register access

Table 55: Register access transfer byte

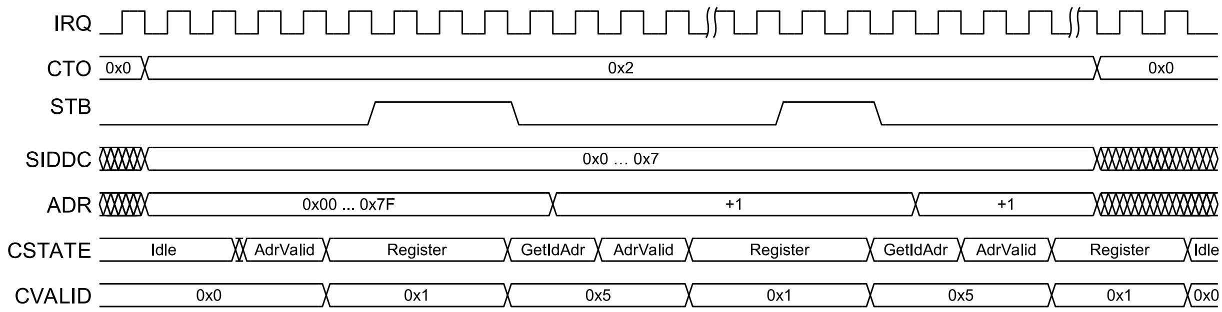


Figure 14: Register read via BiSS

BiSS Write Register Access
The BiSS Write Register Access starts also with CTO = 0x2. Thus, setting the CVALID is the same procedure as for read register. However, after four BiSS frames CTO changes to 0x3. With STB = 1 the data has to be read from RDATA in SPI register 0x4E and must be confirmed with CVALID = 5 as shown in Figure 15. The confirmation procedure has to be completed within two SPI frames. For multiple BiSS Write Register Accesses of consecutive registers the same procedure is repeated. The address is incremented automatically.

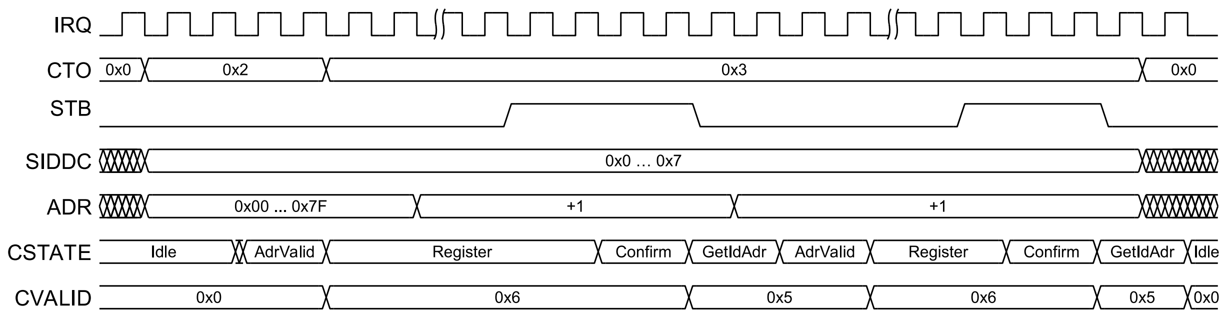


Figure 15: Register write via BiSS

Microcontroller Program Flow
Figure 16 shows the flow of the controller program that needs to be implemented in the host to manage BiSS Command execution and access to the Host's registers via BiSS Control Communication. The flag **EOF** is used to enter the control frame sequence in Figure 17 at least every other frame. During each entry to the control frame sequence one condition (grey box) is checked, one MCU procedure (green box) is executed and the next control frame state CSTATE is reached.

i See Table 25 for details on which BiSS Commands and BiSS Register Accesses have to be managed by the host.

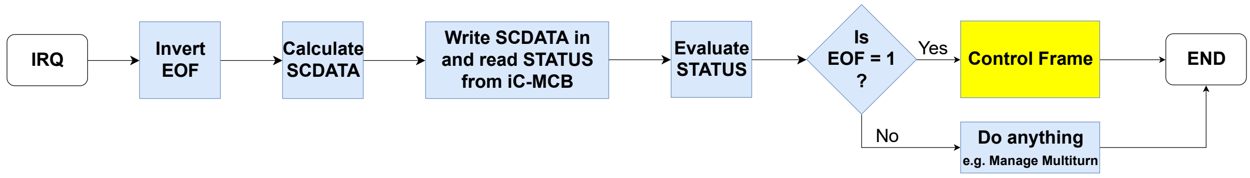


Figure 16: MCU program flow

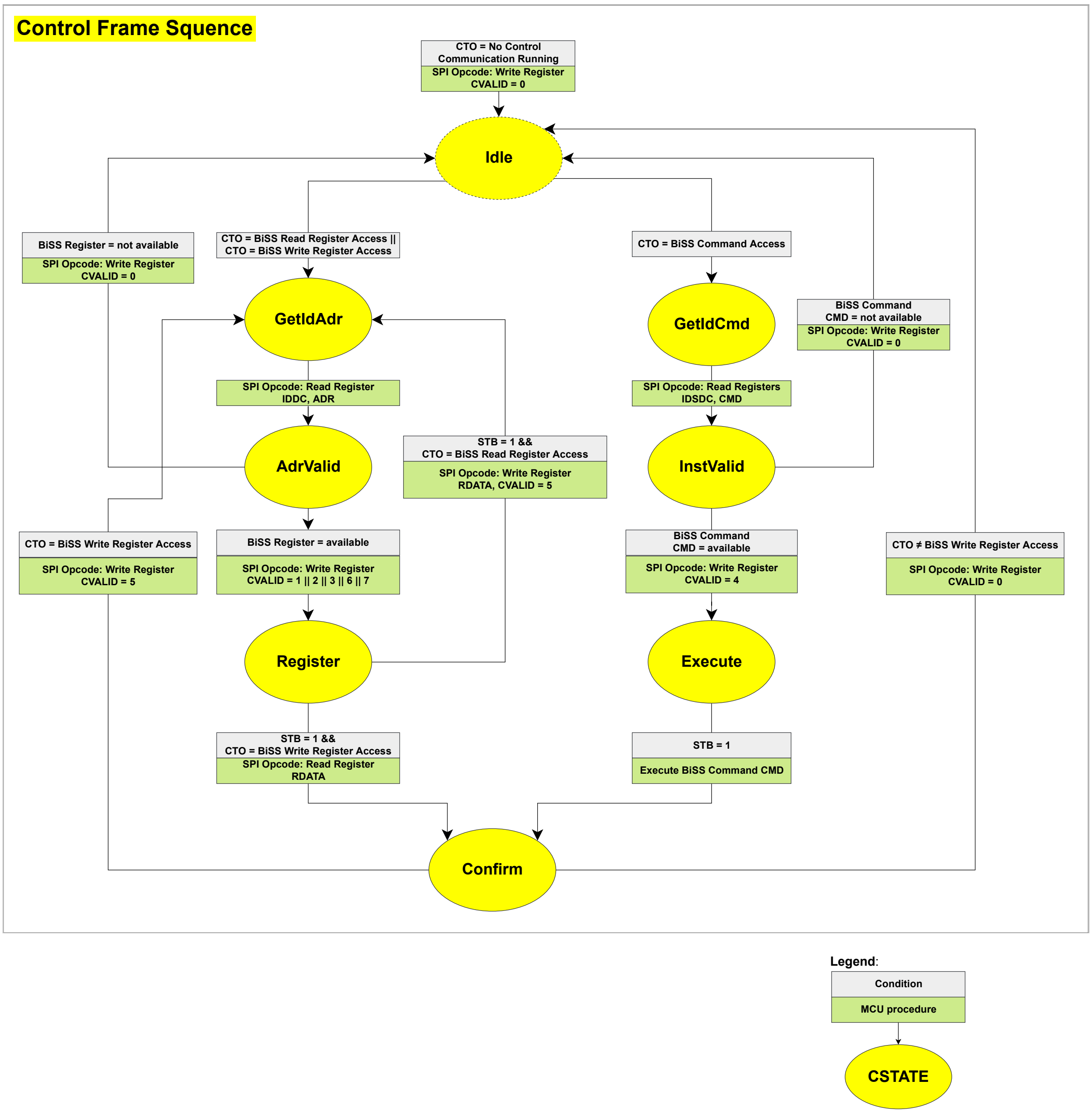


Figure 17: Microcontroller programm flow for control frame sequence using CVALID

As shown in Figure 17 CVALID is set several times to control the programm flow. Alternatively, CVALID can be set in advance and the programm flow is controlled by setting IVALID to accept BiSS Commands and CONFIRM to accept BiSS Register accesses. CONFIRM is suitable to grant sequential register access to complete BiSS banks (e.g. to allow a BiSS master to read the electronic data sheet). IVALID is suitable if all BiSS Commands are implemented. Figure 18 shows the MCU's programm flow when IVALID and CONFIRM are used.

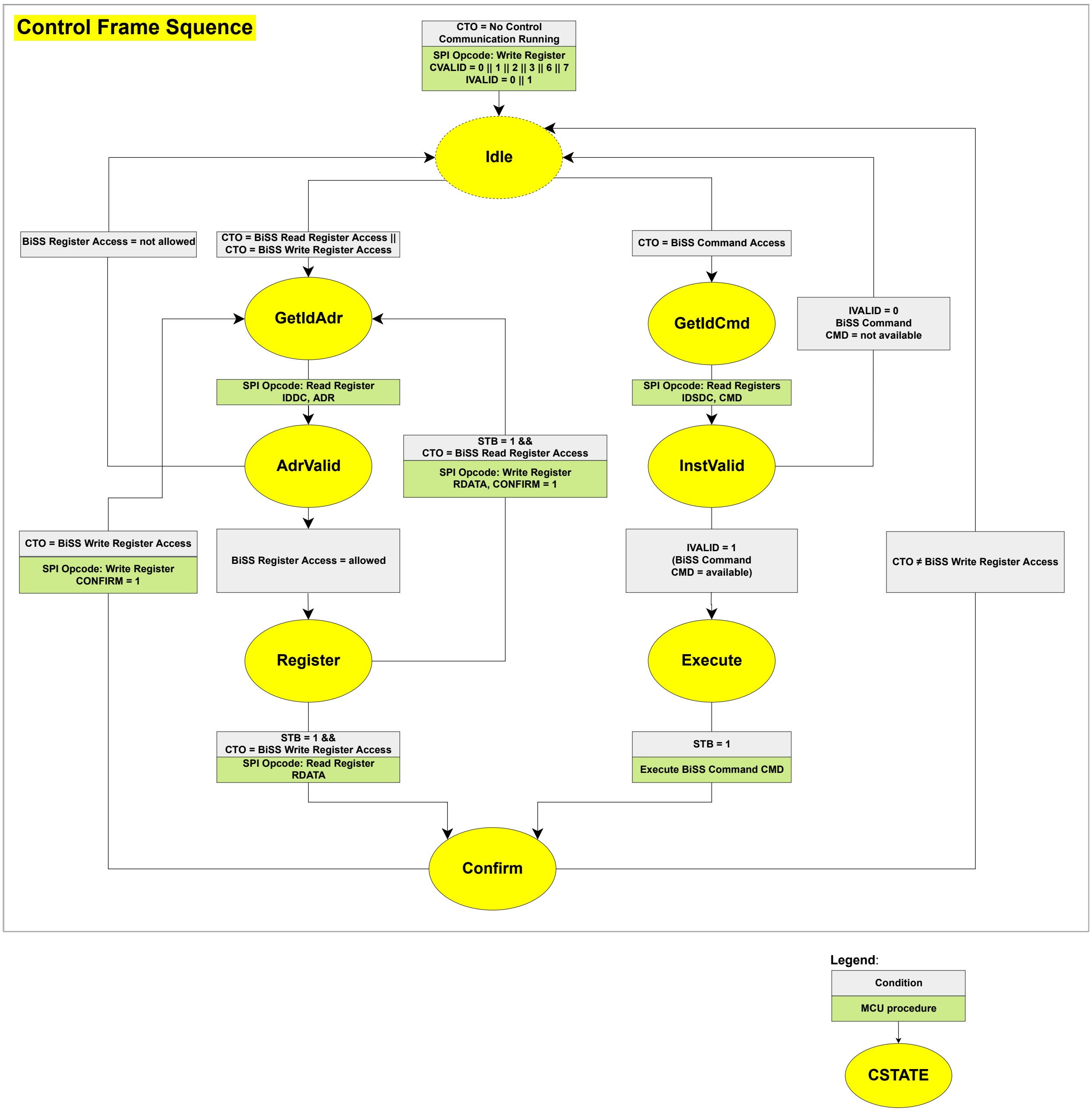


Figure 18: Microcontroller programm flow for control frame sequence using IVALID and CONFIRM. CVALID has to be set only once in advance.

FAST SENSOR INTERFACE: SPI MASTER

When ENFSI = 1 an external sensor can automatically be read in realtime without controller support via the Fast Sensor Interface at IO1 . . . IO4.

Depending on the crossbar configuration parameter CB_FSI at least the clock signal (SCLK) and a data signal (MISO or MOSI) are used. The polarity CPOL and phase CPHA are programmable as shown in Figure 19 and 20.The BiSS latch point is transferred to SCLK or to the additional chip select signal NCS using .

ENFSI	Addr. 0x7; bit 6	R/W 0
0	Fast Sensor interface disabled	
1	Fast Sensor interface enabled	

Table 56: Enable Fast Sensor Interface

DLFSI defines the data length/ count of SCLK clock periods at the Fast Sensor Interface.

DLFSI	Addr. 0x7; bit 5:0	R/W 0
0x00	1 bit	
...	(DLFSI + 1) bit	
0x3F	64 bit	

Table 57: Data length Fast Sensor Interface

HEADL defines the count of received MISO bits at the Fast Sensor Interface that are considered as header and not used for Single-Cycle Data.

HEADL	Addr. 0x8; bit 3:0	R/W 0
0x0 . . . 0xF	Header length (0 . . . 15 bit)	

Table 58: SPI request header length

With STAFSI=0x1 or 0x3 iC-MCB observes MISO and waits for a start bit. Therefore a delay of data availability (e.g. the SPI slave's processing time) can be considered and is indicated by the transmitted data.

STAFSI	Addr. 0x8; bit 5:4	R/W 0
0x0	No start bit in sensor data	
0x1	Wait for high active start bit	
0x2	Reserved	
0x3	Wait for low active start bit	

Table 59: Observe start bit from sensor

IDLE	Addr. 0x8; bit 6	R/W 0
0	MOSI at low level during idle	
1	MOSI at high level during idle	

Table 60: Idle state at MOSI

CPOL	Addr. 0x9; bit 0	R/W 0
0	SPI polarity 0	
1	SPI polarity 1	

Table 61: SPI protocol polarity

CPHA	Addr. 0x9; bit 1	R/W 0
0	SPI phase 0	
1	SPI phase 1	

Table 62: SPI protocol phase

CLKDIV	Addr. 0x9; bit 7:4	R/W 0
	before chip release Z	from chip release Z
0x0	1 (20 MHz)	
0x1	2 (10 MHz)	
0x2	4 (5 MHz)	
. . .	2*CLKDIV (3.33 MHz . . . 1.11 MHz)	
0xA	20 (1 MHz)	
0xB	22 (909 kHz)	24 (833 KHz)
0xC	24 (833 kHz)	32 (625 KHz)
0xD	26 (769 kHz)	40 (500 KHz)
0xE	28 (714 kHz)	50 (400 KHz)
0xF	30 (667 kHz)	64 (312.5 KHz)

Table 63: SPI clock divider

With HEADER an SPI Opcode for the connected sensor can be defined. This Opcode is sent as a leading byte via MOSI to request required data. This can also be useful to consider the SPI slave's processing time. The parameter HEADL is also relevant for the HEADER output.

HEADER	Addr. 0xA; bit 7:0	R/W 0
0x0 . . . 0xFF	Header (first byte only)	

Table 64: SPI request header

The parameter G2B is used to convert gray coded sensor data into binary for BiSS transmission.

G2B	Addr. 0x9; bit 3	R/W 0
0	No data conversion	
1	Gray to binary conversion	

Table 65: Gray to binary conversion for sensor data

REQ_FT	Addr. 0x9; bit 2	R/W 0
0	Feed forward to NCS	
1	Feed forward to SCLK	

Table 66: BiSS request Sensor Feedthrough

BiSS does latch the position data with the first rising edge. The parameter REQ_FT permits synchronous Fast Sensor interface latch that may be NCS based or SCLK based. With REQ_FT = 0 the first falling edge of NCS matches with the BiSS latch (first rising edge of MA).

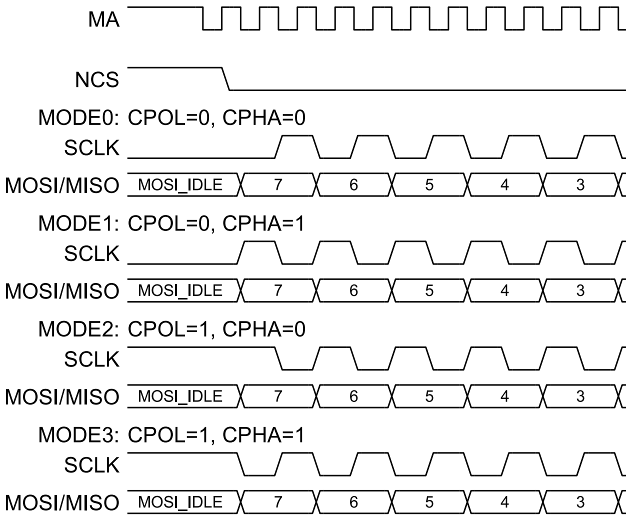


Figure 19: Fast Sensor Interface: phase and polarity (REQ_FT = 0)

OSCDIV2	Addr. 0x7; bit 8	R/W 0
0x0	f_{OSC} divide by 2 disabled	
0x1	f_{OSC} divide by 2 enabled	
Note	OSCDIV2 is not implemented from chip revision Z.	

Table 67: Oscillator Frequency divide by 2

With REQ_FT = 1 the first riding edge of SCLK matches with the BiSS latch (first rising edge of MA).

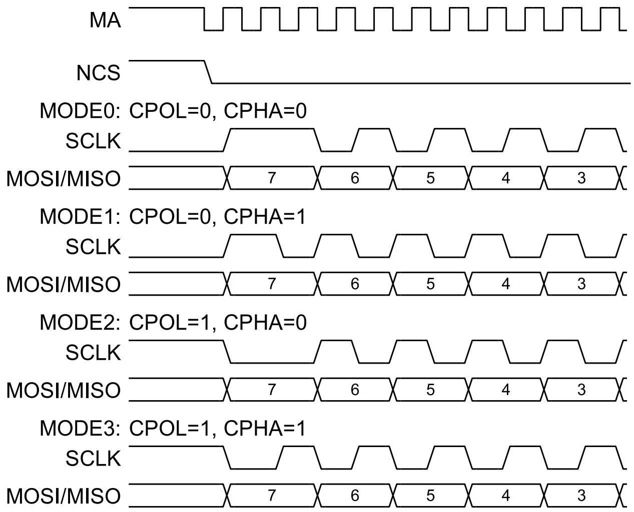


Figure 20: Fast Sensor Interface: phase and polarity (REQ_FT = 1)

Note: The parameter OSCDIV2 = 1 does half the internal oscillator frequency f_{OSC} and affects all f_{OSC} related timings of iC-MCB.

I/O CROSSBAR

The I/O crossbar is used to map several functions to the six IO ports. The mapping is created with a priority order; an enabled function uses the next unused IO. The Table 68 shows the priority in descending order (Highest priority on top, lowest priority at the bottom). A (X) is used for a possible mapping and a (-) if the function is not available at the appropriate IO.

Function	IO1	IO2	IO3	IO4	IO5	IO6
SCLK_M	X	-	-	-	-	-
MOSI_M	-	X	-	-	-	-
MISO_M	-	X	X	-	-	-
NCS_M	-	-	X	X	-	-
CLK	X	X	X	X	X	X
IRQ	X	X	X	X	X	X
MAO	-	X	X	X	X	X
SLI	-	-	X	X	X	X
BK	-	-	-	X	X	X
SLO_O	-	-	-	-	X	X
SLO_I	-	-	-	-	-	X

Table 68: Possible mappings to IOx ports

CB_FSI	Addr. 0xC; bit 2:0	R/W 0
0b000	Fast Sensor interface not used	
0b001	SCLK_M, MOSI_M and MISO_M used	
0b010	SCLK_M and MOSI_M used	
0b011	SCLK_M and MISO_M used	
0b100	Reserved	
0b101	SCLK_M, MOSI_M, MISO_M and NCS used	
0b110	SCLK_M, MOSI_M and NCS used	
0b111	SCLK_M, MISO_M and NCS used	

Table 69: Configuration Fast Sensor Interface

CB_CLK	Addr. 0xC; bit 3	R/W 0
0	Internal oscillator clock used	
1	External clock at IOx used	

Table 70: External clock oscillator input

CB_IRQ	Addr. 0xC; bit 4	R/W 0
0	IRQ not used	
1	IRQ connected to IOx	

Table 71: Interrupt request output

CB_MAO	Addr. 0xC; bit 5	R/W 0
0	MAO not used	
1	MAO connected to IOx	

Table 72: BiSS clock output MA

CB_SLI	Addr. 0xC; bit 6	R/W 0
0	SLI internally connected to ’0’	
1	SLI connected to IOx	

Table 73: BiSS data input SLI

CB_SLO	Addr. 0xC; bit 7	R/W 0
0	SLO_O and SLO_I internally connected	
1	SLO_O and SLO_I connected to IOx	

Table 74: BiSS data output SLO

CMD2EN	Addr. 0x5; bit 5	R/W 0
0	BK not used	
1	BK connected to IOx	

Table 75: Command controlled pin BK
(e.g. for controlling an external bus coupler)

The BK pin can control an external bus coupler for enabling or disabling/terminating BiSS bus structures and the related command control for opening or closing the BiSS bus structure with the bus coupler.

For BiSS bus coupling details please check the **BiSS C protocol** http://www.ichaus.com/BiSS and also the bus coupling capable RS422 line driver **iC-HF** http://www.ichaus.com/HF .

APPLICATION NOTES

This application example shows multiple possibilities on using iC-MCB.

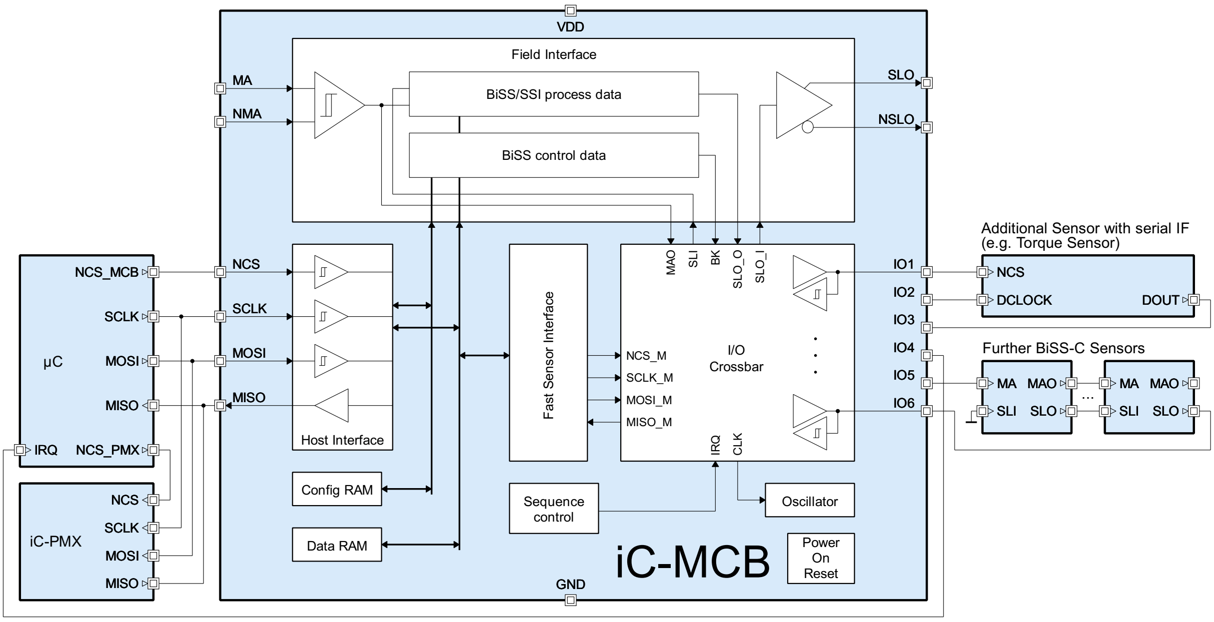


Figure 21: Multiple sensor integration with point-to-point BiSS interface

Point-to-point BiSS interface

iC-MCB provides the typical point-to-point BiSS interface physical layer based on RS422 MA input and RS422 SLO output. On a point-to-point BiSS interface setup no additional external RS422 transceiver is needed. BiSS bus capable device interfaces are also possible but require additional external RS422 transceiver: single receiver for SLI and single RS422 driver for MAO.

Host based sensor function

The microcontroller (µC) does manage related parts of a possible sensor functionality. The µC does configure iC-MCB and also additional SPI slave based devices, in this case iC-PMX. The data channel related CRC and the timeout of the device is generated by the iC-MCB. Register and control communication is replied by the connected BiSS bus devices and by the iC-MCB with support of the host. The µC is notified with the IRQ interrupt signal of the IO cross matrix. This can be useful to capture additional sensor data by the µC at the BiSS latch event.

Including additional BiSS devices with a device internal BiSS bus structure

Even on a point-to-point BiSS interface of the device BiSS permits an internal bus structure as a daisy chain setup. Here iC-MCB connects the additional BiSS slaves with the IO cross matrix. The additional data channels of those the additional BiSS slaves are passed through and not changed by the iC-MCB. This can be useful to add additional sensor functions to an existing BiSS slave bus e.g. a BiSS Safety sensor setup.

Including additional serial devices with the FAST SENSOR INTERFACE

iC-MCB connects the additional serial device (sensor) with the FAST SENSOR INTERFACE and IO cross matrix. The serial sensor device data is captured and mapped to a dedicated data channel of iC-MCB. The data channels related CRC is generated by the iC-MCB. This can be useful to add additional sensor data without the need to handle this data by µC and archiving a low sensors reply timing.

DESIGN REVIEW: Notes On Chip Functions

iC-MCB 3		
No.	Function, Parameter/Code	Description and Application Notes
1	USDST, IVALID, CONFIRM	Not available in chip revision 3.
2	BUSY, CLKDIV	Coding changed as of chip revision Z.
3	OSCDIV2	Not available as of chip revision Z.

Table 76: Notes on chip functions regarding iC-MCB chip revision 3

iC-MCB Z		
No.	Function, Parameter/Code	Description and Application Notes
		None at time of release.

Table 77: Notes on chip functions regarding iC-MCB chip revision Z

REVISION HISTORY

Rel.	Rel. Date[1]	Chapter	Modification	Page
A1	2017-11-17		Initial release.	

Rel.	Rel. Date[1]	Chapter	Modification	Page
B1	2020-09-11	STARTUP AND OPERATION	CHPREL extended by 0x04: iC-MCB Z	12
		STARTUP AND OPERATION	ACQMODE: "Direct" changed to "Undelayed" and "Sample" changed to "Request"	12
		STARTUP AND OPERATION	Parameter USDST added and description extended	12
		FIELD INTERFACE: BiSS	Parameter BUSY coding changed Renamed characteristic fsys → f_{osc}	13
		BiSS CONTROL COMMUNICATION	Parameter IVALID and CONFIRM added Renamed parameter IDS → IDSDC Renamed parameter BROADCAST → BROADC Renamed parameter OPCODE → CMD Renamed parameter SLAVEID → SIDDC	13
		HOST INTERFACE: SPI SLAVE	Renamed SPI Opcodes: SDAD Transmission → Transmit SDAD Read REGISTER (delayed) → Read Register Write REGISTER (cont.) → Write Register	17
		FAST SENSOR INTERFACE: SPI MASTER	Parameter CLKDIV coding and OSCDIV2 changed	25

[1] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-MCB	16-pin QFN16, 3 mm x 3 mm, thickness 0.9 mm, RoHS compliant	iC-MCB QFN16-3x3
Evaluation Board	80 mm x 100 mm eval board	iC-MCB EVAL MCB_1D

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