iC-HGP
3 A HIGH-SIDE LASER SWITCH

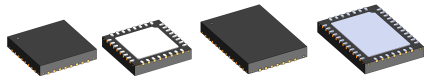
FEATURES

- Six channel laser switch from CW up to 200 MHz
- CW operation with up to 500 mA per channel
- Pulsed operation with up to 1.5 A per channel
- Spike-free switching of the laser current
- 6 x 1 channels with TTL inputs
- 3 x 2 channels with LVDS inputs
- Operates as six independent voltage-controlled current sources
- Laser supplies are 12 V capable for blue/green laser diodes
- Fast and slow switching mode
- Simple current control at pins CIx
- CIx voltage < 3 V for full CW current
- Wide supply voltage range from 3 to 5.5 V
- All channels can be paralleled for up to 3 A CW and 9 A pulsed operation
- Multiple iC-HGP can be connected in parallel for higher currents
- Open drain error output
- Thermal shutdown

APPLICATIONS

- Pump lasers
- Laser projection
- Laser TV
- Data transmission
- TOF camera lighting
- LIDAR lighting

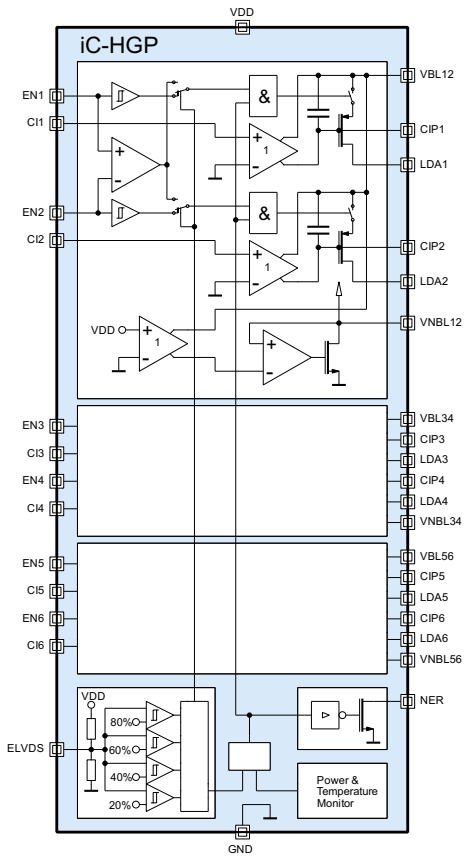
PACKAGES



QFN32
5 mm x 5 mm
RoHS compliant

QFN38
5 mm x 7 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

Six channel laser switch iC-HGP enables the spike-free switching of laser diodes with well-defined current pulses at frequencies ranging from DC to 200 MHz. The high-side circuit architecture of the iC-HGP allows the operation of common-cathode laser diode arrays with cathode grounded.

The diode current is determined by the voltages at pins CIx.

The six fast switches are controlled independently via TTL inputs. Input LVDS = hi selects LVDS type inputs and three channel mode. *TTL slow switch mode* is selected with 30% VDD and *LVDS slow switch mode* with 70% VDD at input ELVDS.

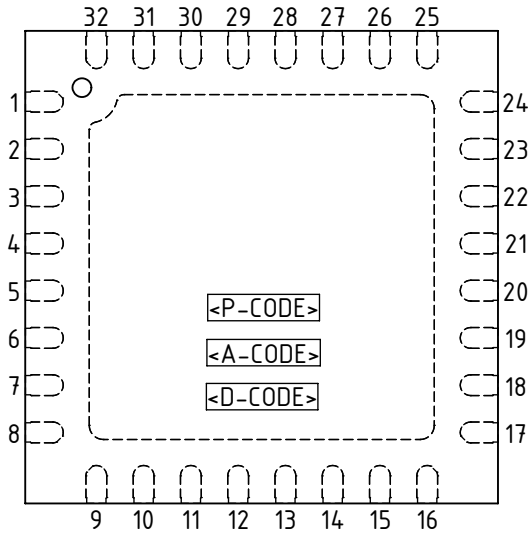
The laser diode can thus be turned on and off or switched between different current levels (LDAx connected) defined by the voltages at CIx.

Each channel can be operated up to 500 mA CW and 1500 mA pulsed current depending on the frequency, duty cycle and heat dissipation.

The integrated thermal shutdown feature protects the iC-HGP from damage by excessive temperature.

PACKAGING INFORMATION

PIN CONFIGURATION QFN32 5 mm x 5 mm

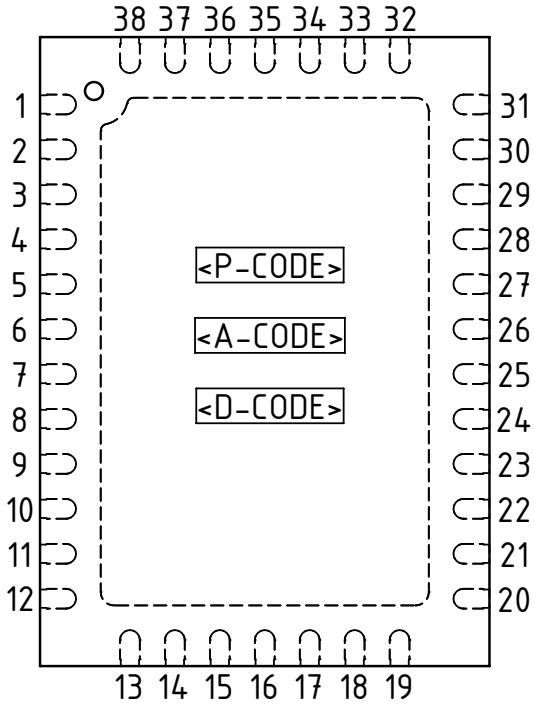


PIN FUNCTIONS

No.	Name	Function
1	CI1	Current control voltage channel 1
2	CI2	Current control voltage channel 2
3	CI3	Current control voltage channel 3
4	GND	Ground
5	CI4	Current control voltage channel 4
6	CI5	Current control voltage channel 5
7	CI6	Current control voltage channel 6
8	VBL12	Laser supply voltage channel 1 and 2
9	VNBL12	Supply voltage channel 1 and 2
10	VBL12	Laser supply voltage channel 1 and 2
11	VBL34	Laser supply voltage channel 3 and 4
12	VNBL34	Supply voltage channel 3 and 4
13	VBL34	Laser supply voltage channel 3 and 4
14	VBL56	Laser supply voltage channel 5 and 6
15	VNBL56	Supply voltage channel 5 and 6
16	VBL56	Laser supply voltage channel 5 and 6
17	EN6	TTL switching input channel 6 Negative LVDS Input channel 5 and 6
18	EN5	TTL switching input channel 5 Positive LVDS Input channel 5 and 6
19	EN4	TTL switching input channel 4 Negative LVDS Input channel 3 and 4
20	EN3	TTL switching input channel 3 Positive LVDS Input channel 3 and 4
21	GND	Ground
22	ELVDS	TTL/LVDS Fast/Slow Input selector
23	VDD	Supply voltage
24	EN2	TTL switching input channel 2 Negative LVDS Input channel 1 and 2
25	EN1	TTL switching input channel 1 Positive LVDS Input channel 1 and 2
26	LDA6	Laser diode anode channel 6
27	LDA5	Laser diode anode channel 5
28	LDA4	Laser diode anode channel 4
29	LDA3	Laser diode anode channel 3
30	LDA2	Laser diode anode channel 2
31	LDA1	Laser diode anode channel 1
32	NER	Error monitor output
TP		Thermal Pad (GND)

The *Thermal Pad* is to be connected to a *Ground Plane* (GND) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (iC HGP label and coding is subject to change).

PIN CONFIGURATION QFN38 5 mm x 7 mm



PIN FUNCTIONS

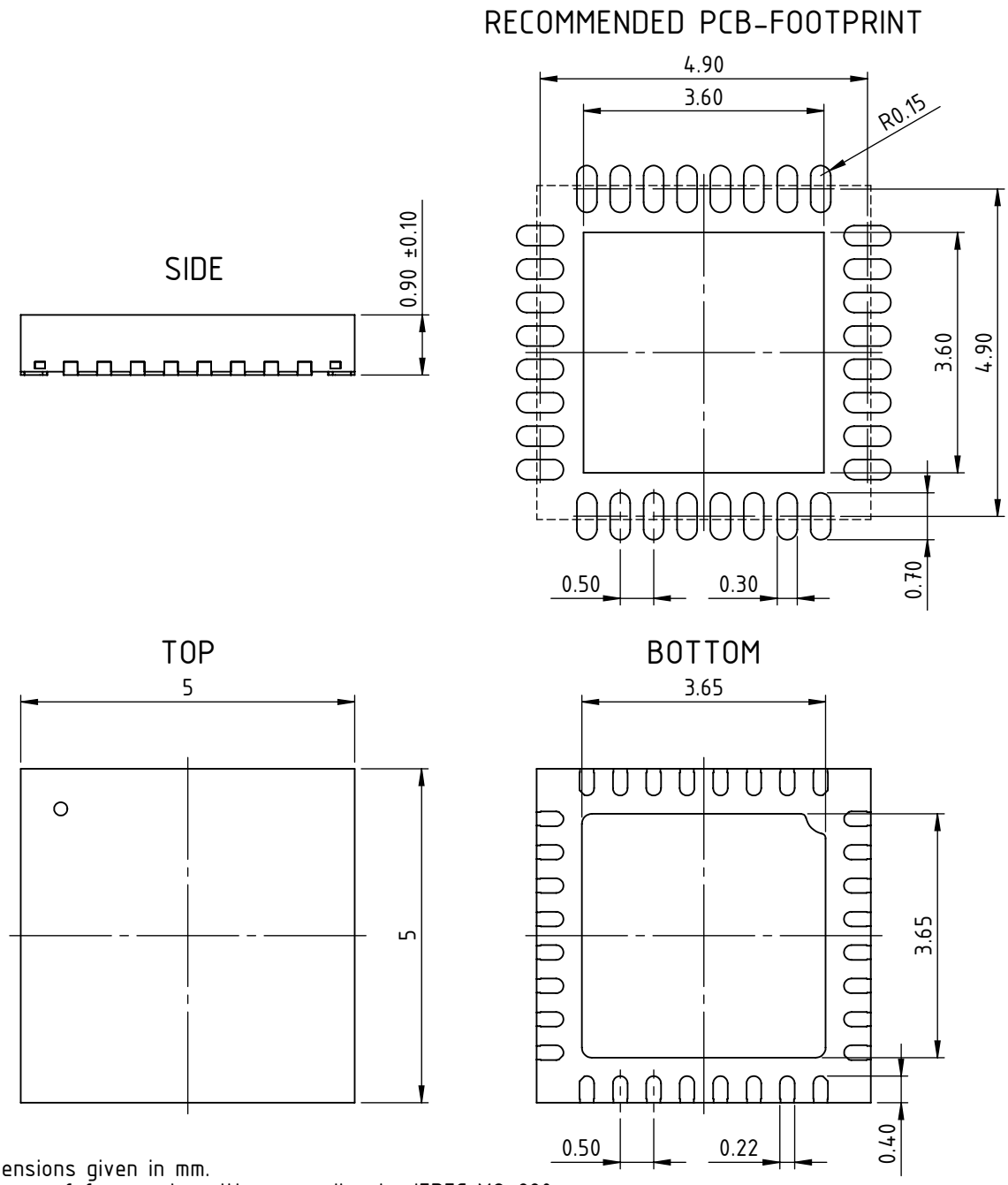
No.	Name	Function
1	CI6	Current control voltage channel 6
2	CIP6	Current control voltage high channel 6
3	VBL12	Laser supply voltage channel 1 and 2
4	VNBL12	Supply voltage channel 1 and 2
5	VBL12	Laser supply voltage channel 1 and 2
6	VBL34	Laser supply voltage channel 3 and 4
7	VNBL34	Supply voltage channel 3 and 4
8	VBL34	Laser supply voltage channel 3 and 4
9	VBL56	Laser supply voltage channel 5 and 6

PIN FUNCTIONS

No.	Name	Function
10	VNBL56	Supply voltage channel 5 and 6
11	VBL56	Laser supply voltage channel 5 and 6
12	EN6	TTL switching input channel 6 Negative LVDS Input channel 5 and 6
13	EN5	TTL switching input channel 5 Positive LVDS Input channel 5 and 6
14	EN4	TTL switching input channel 4 Negative LVDS Input channel 3 and 4
15	EN3	TTL switching input channel 3 Positive LVDS Input channel 3 and 4
16	GND	Ground
17	ELVDS	TTL/LVDS Fast/Slow Input selector
18	VDD	Supply voltage
19	EN2	TTL switching input channel 2 Negative LVDS Input channel 1 and 2
20	EN1	TTL switching input channel 1 Positive LVDS Input channel 1 and 2
21	LDA6	Laser diode anode channel 6
22	LDA5	Laser diode anode channel 5
23	LDA4	Laser diode anode channel 4
24	LDA3	Laser diode anode channel 3
25	LDA2	Laser diode anode channel 2
26	LDA1	Laser diode anode channel 1
27	NER	Error monitor output
28	CI1	Current control voltage channel 1
29	CIP1	Current control voltage high channel 1
30	CI2	Current control voltage channel 2
31	CIP2	Current control voltage high channel 2
32	CI3	Current control voltage channel 3
33	CIP3	Current control voltage high channel 3
34	GND	Ground
35	CI4	Current control voltage channel 4
36	CIP4	Current control voltage high channel 4
37	CI5	Current control voltage channel 5
38	CIP5	Current control voltage high channel 5
TP		Thermal Pad (GND)

The *Thermal Pad* is to be connected to a *Ground Plane* (GND) on the PCB.
Only pin 1 marking on top or bottom defines the package orientation (© HGP label and coding is subject to change).

PACKAGE DIMENSIONS QFN32-5x5



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

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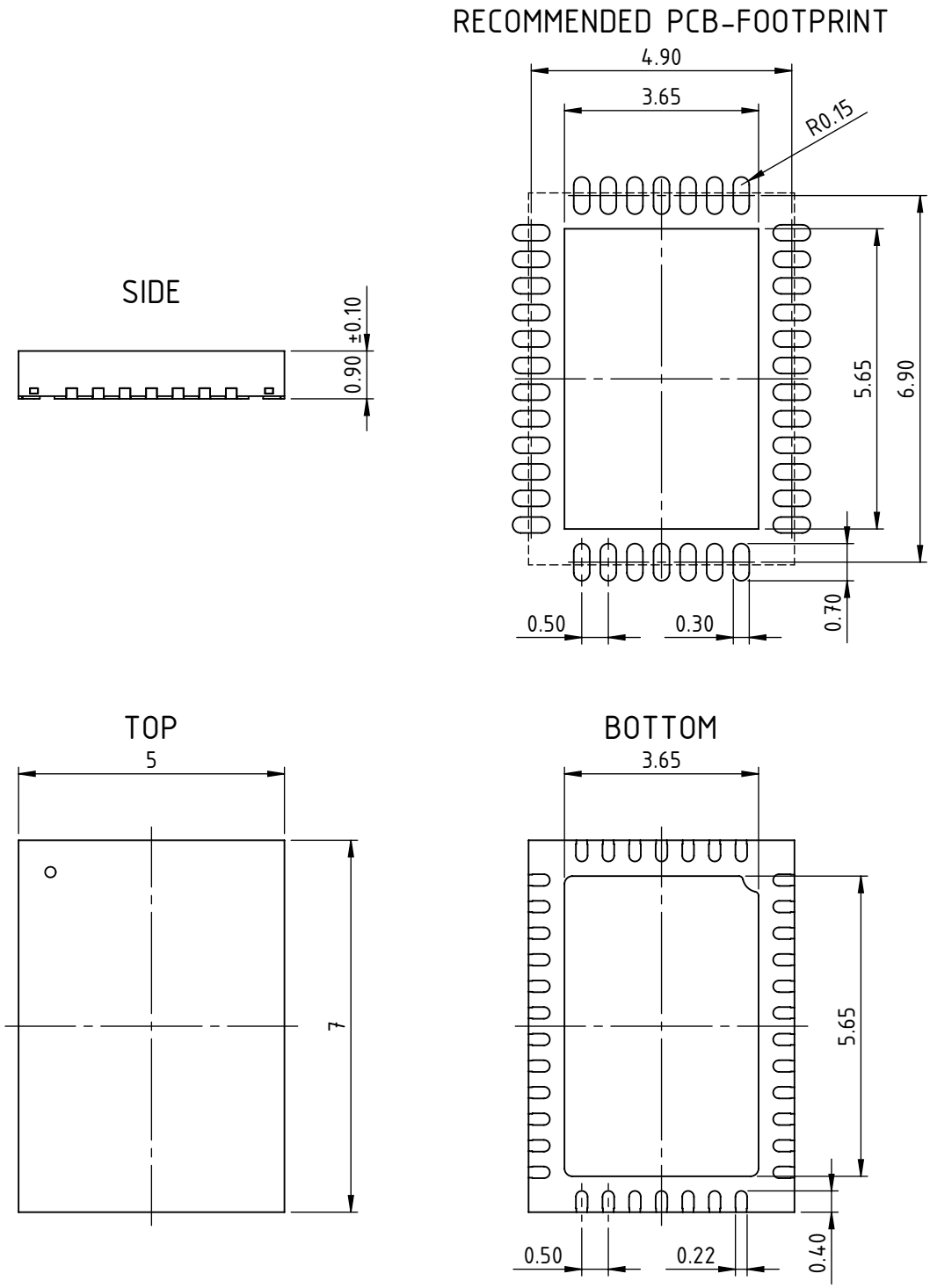
PACKAGE DIMENSIONS QFN38-5x7



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220

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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.3	6	V
G002	I(VDD)	Current in VDD		-10	50	mA
G003	V(VBL)	Voltage at VBL12, VBL34, VBL56, CIP1...6		-0.3	12	V
G004	I(VBL)	Current in VBL12, VBL34, VBL56	DC current	-10	1200	mA
G005	V(VNBL)	Voltage at VNBL12, VNBL34, VNBL56	VBL < 6 V VBL > 6 V	-0.3 VBL − 6	VBL + 0.3 VBL + 0.3	V V
G006	I(VNBL)	Current in VBL12, VBL34, VBL56	DC current	-10	10	mA
G007	V(CI)	Voltage at CI1...6		-0.3	6	V
G008	V()	Voltage at EN1...6, ELVDS, NER		-0.3	6	V
G009	V(LDA)	Voltage at LDA1...6		-0.3	12	V
G010	I(LDA)	Current in LDA1...6	DC current	-600	10	mA
G011	I()	Current in CI1...6, CIP1...6, EN1...6, ELVDS		-10	10	mA
G012	I(NER)	Current in NER		-10	20	mA
G013	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G014	Tj	Operating Junction Temperature		-40	125	°C
G015	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended range on request)		-25		85	°C
T02	Rthja	Thermal Resistance Chip/Ambient	Mounted onto the Evaluation Board HGP1D		25		K/W
T03	RthjTP	Thermal Resistance Chip/Thermal Pad			4		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0...5.5 V, Tj = -40...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device (x = 1...6)							
001	VDD	Permissible Supply Voltage		3		5.5	V
002	I(VDD)	Supply Current in VDD	CW operation; V(ELVDS) < 35% VDD, TTL V(ELVDS) > 65% VDD, LVDS	 2 4		 10 22	 mA mA
004	VBL	Permissible Supply Voltage VBL12, VBL34, VBL56		-0.3		12	V
007	V(LDAx)	Permissible Voltage at LDAx		3		12	V
008	V(NER)	Permissible Voltage at NER		-0.3		5.5	V
009	Vc(NER)	Clamp Voltage hi at NER	I(NER) = 1 mA	7	15	18	V
010	Vc(CIx)hi	Clamp Voltage hi at CIx	Vc(CIx) = V(CIx) − VDD, I(CI) = 1 mA, other pins open	0.8		3	V
011	Vc()hi	Clamp Voltage hi at ENx, ELVDS	Vc() = V() − VDD, I() = 1 mA, other pins open	0.8		3	V
012	Vc()lo	Clamp Voltage lo at VDD,VBL12, VBL34,VBL56, LDAx, CIx, CIPx, ENx, VNBL12, VNBL34,VNBL56, ELVDS, NER	I() = -10 mA, other pins open	-1.6		-0.3	V
Laser Control LDA1...6, CI1...6, CIP1...6, (x = 1...6)							
101	Icw(LDAx)	Permissible CW Current in LDAx (per channel)		-500			mA
102	Vs(LDAx)	Saturation Voltage at LDAx	I(LDAx) = -450 mA, V(CIx) = V(CIx)@I(LDKx) = -500 mA			1.5	V
103	I0(LDAx)	Leakage Current in LDAx	ENx = lo, V(LDAx) = 0 V, VBL = 12 V	-100			µA
104	tr()	LDAx Current Rise Time Fast	Iop(LDAx) = -500 mA, I(LDAx): 10% → 90% Iop, V(ELVDS) = 0 V or VDD			1	ns
105	tf()	LDAx Current Fall Time Fast	Iop(LDAx) = -500 mA, I(LDAx): 90% → 10% Iop, V(ELVDS) = 0 V or VDD			1	ns
106	tr()	LDAx Current Rise Time Slow	Iop(LDAx) = -500 mA, I(LDAx): 10% → 90% Iop, V(ELVDS) = 30% VDD or 70% VDD, VDD = 5 V	5	10	40	ns
107	tf()	LDAx Current Fall Time Slow	Iop(LDAx) = -500 mA, I(LDAx): 90% → 10% Iop, V(ELVDS) = 30% VDD or 70% VDD, VDD = 5 V	5	10	40	ns
108	tr()	LDAx Current Rise Time Slow	Iop(LDAx) = -500 mA, I(LDKx): 10% → 90% Iop, V(ELVDS) = 30% or 70% VDD, VDD = 3.3 V	10	30	90	ns
109	tf()	LDAx Current Fall Time Slow	Iop(LDAx) = -500 mA, I(LDKx): 90% → 10% Iop, V(ELVDS) = 30% or 70% VDD, VDD = 3.3 V	10	30	90	ns
110	tp()	Propagation Delay Fast V(ENx) → I(LDKx)	V(ELVDS) = 0 V or VDD, Differential LVDS Rise and Fall Time < 0.5 ns	3	6	16	ns
111	CR()	Current Matching all Channels		0.7		1.3	
112	V(CIx)	Permissible Voltage at CIx		-0.3		VDD	V
113	Vt(CIx)	Threshold Voltage at CIx	I(LDAx) > -5 mA	0.5		1.2	V
114	Vo(CIx)	Operating Voltage at CIx	I(LDAx) = -500 mA, V(LDAx) < VBL − 1.8 V		2	2.9	V
115	Ipd(CIx)	Pull-Down Current at CIx	V(CIx) = 0.5...5.5 V	1	2.5	5	µA
116	V(CIPx)	Permissible Voltage at CIPx		-0.3		VBL	V
117	Vt(CIPx)	Threshold Voltage at CIx	Vt(CIPx) = VBL - V(CIPx)	1.2		0.5	V
118	Vo(CIPx)	Operating Voltage at CIPx	Vo(CIPx) = VBL - V(CIPx), (I(LDAx) = -500 mA, V(LDAx) < VBL − 1.8 V		2	2.9	V
119	Rpu(CIPx)	Pullup Resistor	V(CIPx) < VBL - 2 V V(CIPx) > VBL - 0.4 V	7 60	11.6	20 800	kΩ kΩ
120	Vc(LDKx)	Clamp Voltage at LDAx	I(LDAx) = -100 mA, tclamp < 1 ms, tclamp/T < 1:100	-2		-0.3	V
121	tskc()	Channel to Channel Skew				160*	ps
122	tskp()	Part to Part Skew	best to worst			4*	ns

* Projected values by simulation

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0...5.5 V, Tj = -40...125 °C unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input EN1...6 (x = 1...6)							
201	Vt(TTL)hi	Input Threshold Voltage hi	V(ELVDS) < 35% VDD, TTL			2	V
202	Vt(TTL)lo	Input Threshold Voltage lo	V(ELVDS) < 35% VDD, TTL	0.8			V
203	Vhys(TTL)	Hysteresis	Vhys() = Vt()hi − Vt()lo; V(ELVDS) < 35% VDD, TTL	50			mV
204	R(EN)	Pull-Down Resistor at ENx	V(ELVDS) < 35% VDD, TTL	100	162	220	kΩ
205	V(EN)	Voltage at EN1, EN3, EN5	V(ELVDS) > 65% VDD, LVDS, ENx open	31	33	35	%VDD
206	V(EN)	Voltage at EN2, EN4, EN6	V(ELVDS) > 65% VDD, LVDS, ENx open	40	42	44	%VDD
207	Ri(EN)	Resistor at EN1, EN3, EN5	V(ELVDS) > 65% VDD, LVDS, ENx open	75	109	155	kΩ
208	Ri(EN)	Resistor at EN2, EN4, EN6	V(ELVDS) > 65% VDD, LVDS, ENx open	80	119	170	kΩ
209	Vdiff	Differential Voltage	Vdiff = |V(EN1,3,5) − V(EN2,4,6)|; V(ELVDS) > 65% VDD, LVDS	200			mV
210	V()	Input Voltage Range	V(ELVDS) > 65% VDD, LVDS	-0.2		VDD + 0.2	V
Input ELVDS							
301	V(ELVDS)	Voltage at ELVDS	ELVDS open	48	50	52	%VDD
302	Ri(ELVDS)	Resistor at ELVDS		35	50	70	kΩ
303	Vt(ELVDS)	Threshold Voltage TTL Fast to TTL Slow		16	20	24	%VDD
304	Vt(ELVDS)	Threshold Voltage TTL Slow to Error		36	40	44	%VDD
305	Vt(ELVDS)	Threshold Voltage Error to LVDS Slow		56	60	64	%VDD
306	Vt(ELVDS)	Threshold Voltage LVDS Slow to LVDS Fast		74	80	84	%VDD
307	Vhys()	Hysteresis		10	25	50	mV
Ouput NER							
401	Vsat(NER)	Saturation Voltage at NER	ELVDS open, I(NER) = 2 mA			0.6	V
402	I(NER)	Current in NER	ELVDS open, V(NER) > 0.6 V	3	9	20	mA
Overtemperature							
501	Toff	Overtemperature Shutdown	rising temperature	130		170	°C
502	Ton	Overtemperature Release	falling temperature	120		160	°C
503	Thys	Hysteresis	Toff − Ton	5			°C
Power On							
601	VON	Power On Voltage VDD	rising voltage			2.9	V
602	VOFF	Power Down Voltage VDD	falling voltage	1.5			V
603	Vhys	Hysteresis		50		500	mV
Switch Power Supply							
701	V(VNBL)	Voltage at VNBL	VDD = 5 V, VBL = 12 V, CW operation	6.8	7	7.2	V
702	Isc(VNBL)	Short circuit current	VDD = 5 V, VBL = 6 V, VNBL = 3 V	360	440	700	mA

CONFIGURATION INPUT ELVDS

Pin ELVDS select between 6 channel TTL mode or 3 channel LVDS mode and chooses slow or fast switching speed. The unconnected pin ELVDS is an error condition signaled at pin NER with the laser current disabled.

Pin ELVDS connected to GND selects the six channel fast TTL mode. Pin ELVDS connected to 30% VDD selects the six channel slow TTL mode. Pin ELVDS connected to 70% VDD selects the three channel slow LVDS mode. Pin ELVDS connected to VDD selects the three channel fast LVDS mode.

An easy way to set the slow operation mode for TTL and LVDS mode is to connect a voltage divider at pin ELVDS. Figure 1 shows the recommended voltage divider for slow TTL mode and Figure 2 shows the recommended voltage divider for slow LVDS mode.

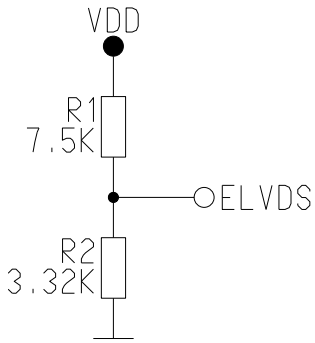

Figure 1: TTL Slow

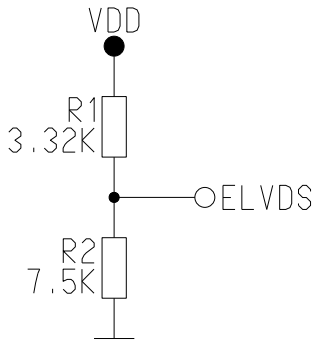

Figure 2: LVDS Slow

DIGITAL INPUTS EN1...6

EN1...6 are the digital switching inputs. With pin ELVDS set to *6 channel TTL mode*, each pin ENx enables the current source at the respective LDAx. With pin ELVDS set to *3 channel LVDS mode*, the odd ENx pins are the positive and the even ENx pins are the negative LVDS inputs:

EN1 and EN2 control LDA1 and LDA2.
EN3 and EN4 control LDA3 and LDA4.
EN5 and EN6 control LDA5 and LDA6.

For correct LVDS operation 100 Ω terminating resistors between the respective ENx pins, very close to the inputs, are strongly recommended. Input pins from unused channels have to be connected to GND (TTL operation) resp. even ENx pins to GND and odd ENx pins to VDD (LVDS operation).

ANALOG CURRENT CONTROL VOLTAGE INPUTS CI1...6

The voltage at pins CI1...6 sets the current in pins LDA1...6. Figures 3 and 4 show the temperature dependency of the current in a single LDAx output versus the voltage at CIx for a *typical* device. Figures 5 and 6 show the min., typ., and max. variations between devices at 27 °C temperature. The voltage at pins LDAx is VBL – 2.5 V.

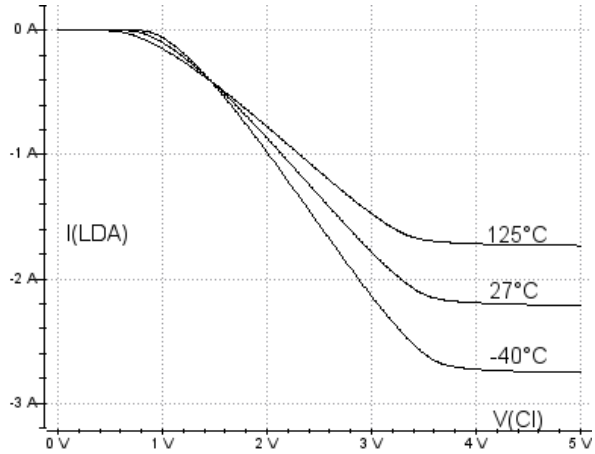

Figure 3: I(LDAx) vs. V(CIx) at VDD = 5 V

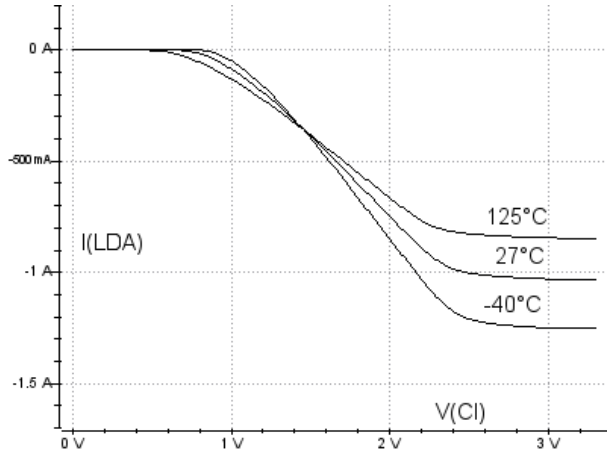

Figure 4: I(LDAx) vs. V(CIx) at VDD = 3.3 V

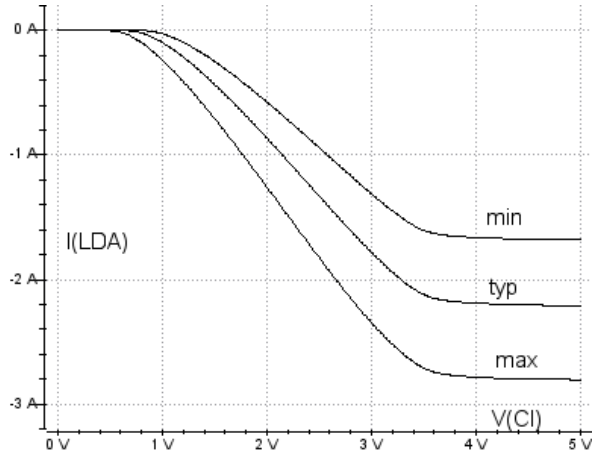

Figure 5: I(LDAx) vs. V(CIx) at VDD = 5 V

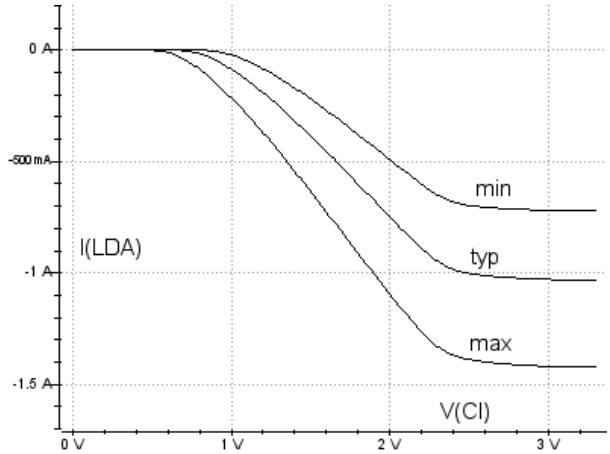

Figure 6: I(LDAx) vs. V(CIx) at VDD = 3.3 V

LASER OUTPUTS LDA1...6

LDA1...6 are the current outputs for the laser diode anode. For high speed operation, connect the laser diode as close as possible to this pins to minimize the inductance. To ensure a high switching speed, it is important to minimise the inductance of the whole current loop including the bypass capacitors.

It may still be necessary though to use an R/C snubber network for damping L/C oscillations.

Figure 7 shows the typical output characteristics of LDA. The left side of the diagram is the RDSon region where the current depends strongly on the voltage at LDA. The right side of the diagram is the current source region where the current depends only somewhat on the voltage at LDA. Only the current source region should be used.

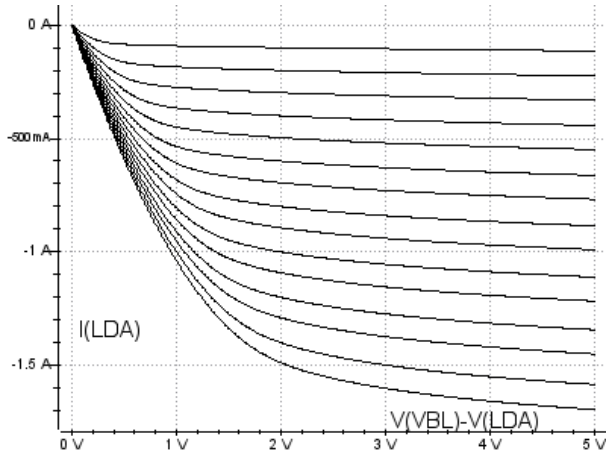

Figure 7: Typical output characteristics of LDA

PULSED OPERATION

The current for pulsed operation may be higher than for CW operation. Therefore the RMS current of the pulse train has to be considered.

$$I_{pulse_{max}} = I_{CW_{max}} \cdot \sqrt{\frac{repetition\ time(T)}{pulse\ time(t)}} \qquad (1)$$

With $I_{CW_{max}}$ from Electrical Characteristics No. 101 and pulses < 10 µs. So for a single channel operated with a 50% duty cycle, the max. laser current becomes

$$I_{pulse_{max}} = 500\,mA \cdot \sqrt{2} = 707\,mA$$

For pulses in the µs range and longer, the larger QFN38-5x7 package with additional bypass capacitors at the pins CIPx is recommended, yielding a better dynamic performance.

For shorter pulses in the ns range and fast rise/fall times the smaller QFN32-5x5 package is to be used.

LASER AND SWITCH SUPPLIES VBL and VNBL

The independent power supplies for the lasers are separated into 3 groups of 2 channels:

VBL12 is the laser supply for channel 1 and 2.
VBL34 is the laser supply for channel 3 and 4.
VBL56 is the laser supply for channel 5 and 6.

The power supply pins for the fast laser switch are VBL and VNBL. The power supply voltage from VBL to VNBL is a mirror of the voltage from VDD to GND and internally generated:

VNBL12 relates to VBL12.
VNBL34 relates to VBL34.
VNBL56 relates to VBL56.

An external capacitor between VBL and VNBL is used to stabilize this power supply. For laser supplies VBL up to 5.5 V the corresponding VNBL can be connected directly to GND and the capacitor can be omitted. An example for separated power supplies and VBL56 up to 5.5 V can be found on page 18: "6 channel TTL fast with 3 separated power supplies".

ERROR OUTPUT NER

The open drain pin NER is a low-active error output. Signalled errors are ELVDS open or at 50% VDD, VDD undervoltage and thermal shutdown.

THERMAL SHUTDOWN

iC-HGP is protected by an integrated thermal shutdown feature. When the shutdown temperature is reached all channels are disabled. Falling temperature after this shutdown will unconditionally enable all channels again. Necessary precaution to prevent damage of the laser may be to also disable any external control circuits for the laser output power or current control during thermal shutdown. The error signal at pin NER can be used to e.g. disable the control circuit.

APPLICATION EXAMPLES

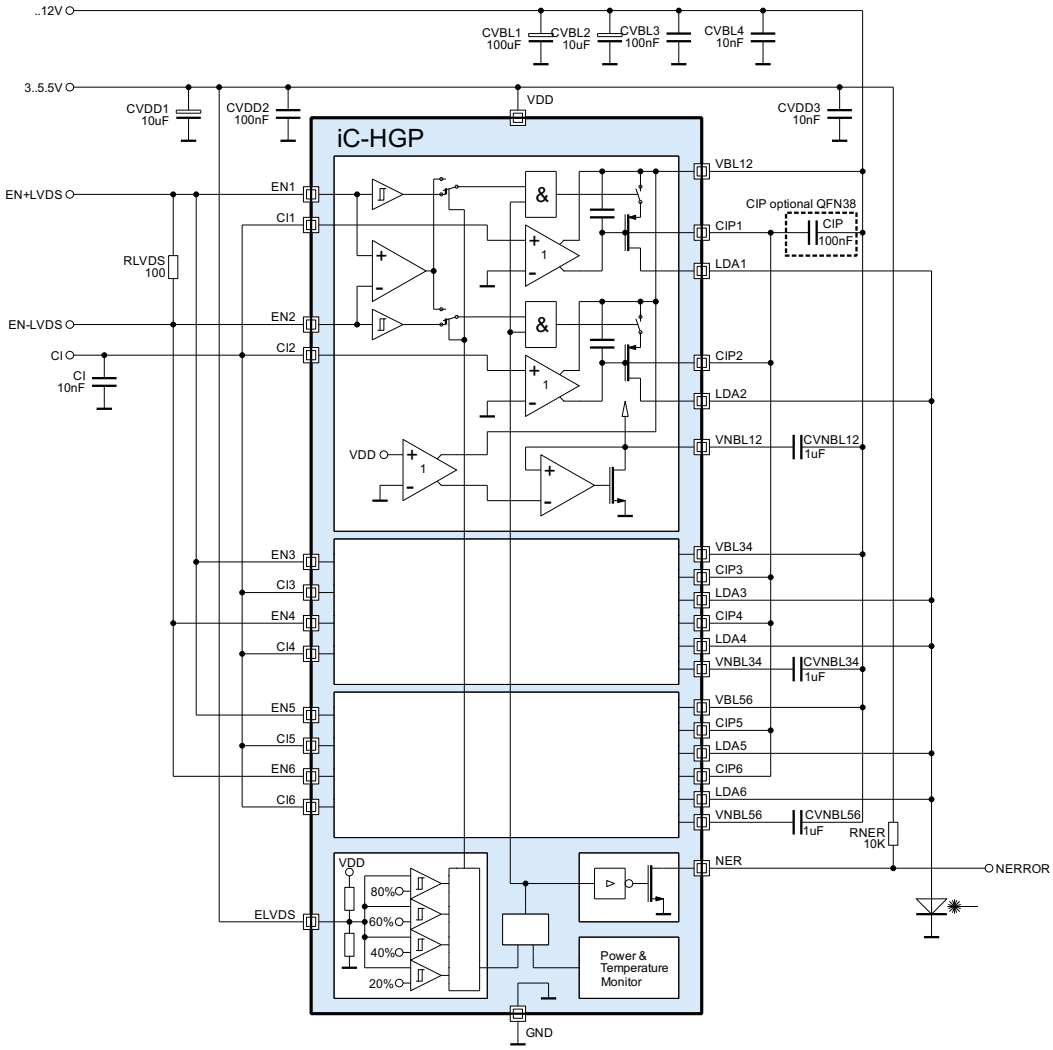

Figure 8: 1 channel LVDS fast

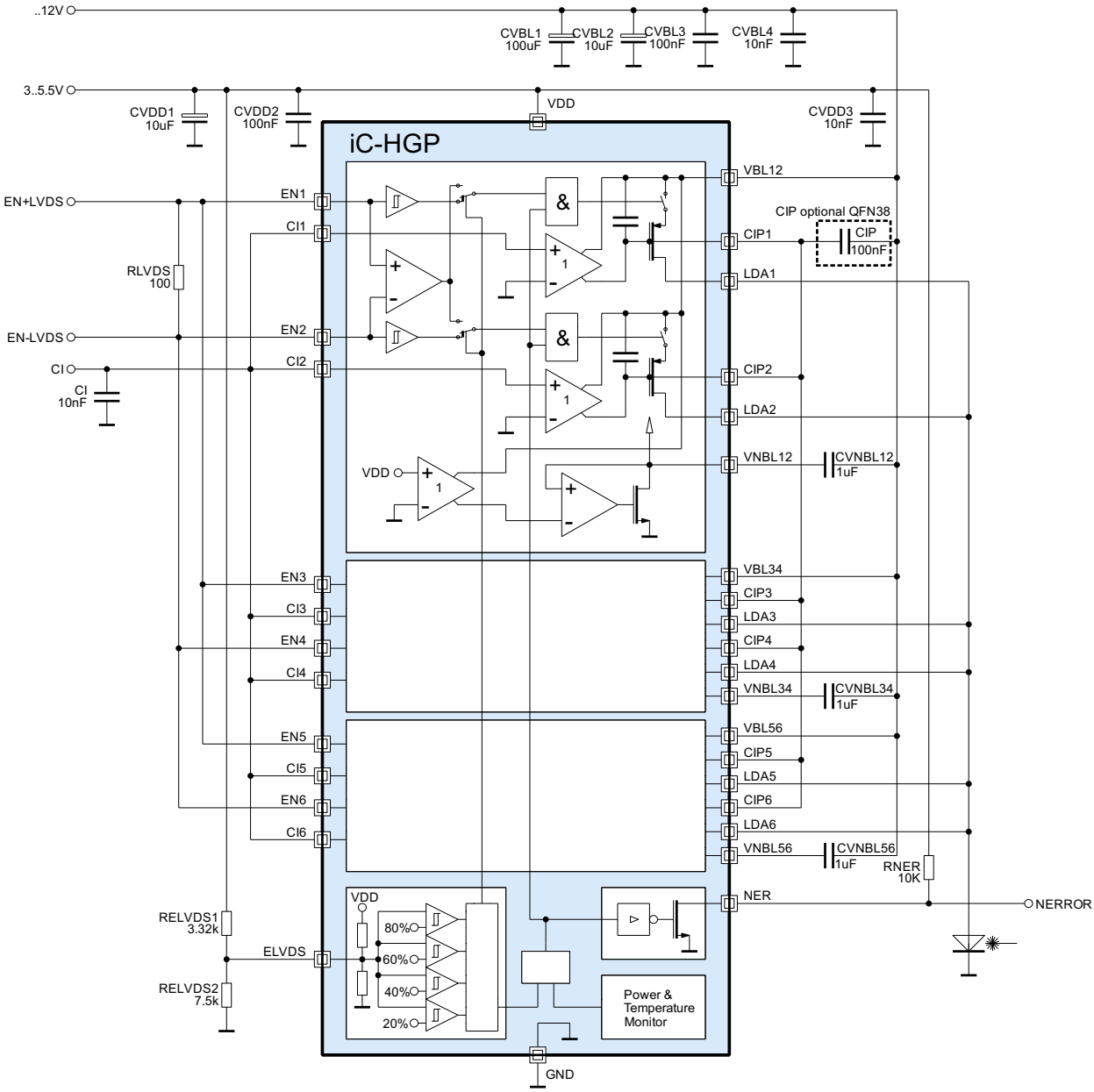

Figure 9: 1 channel LVDS slow

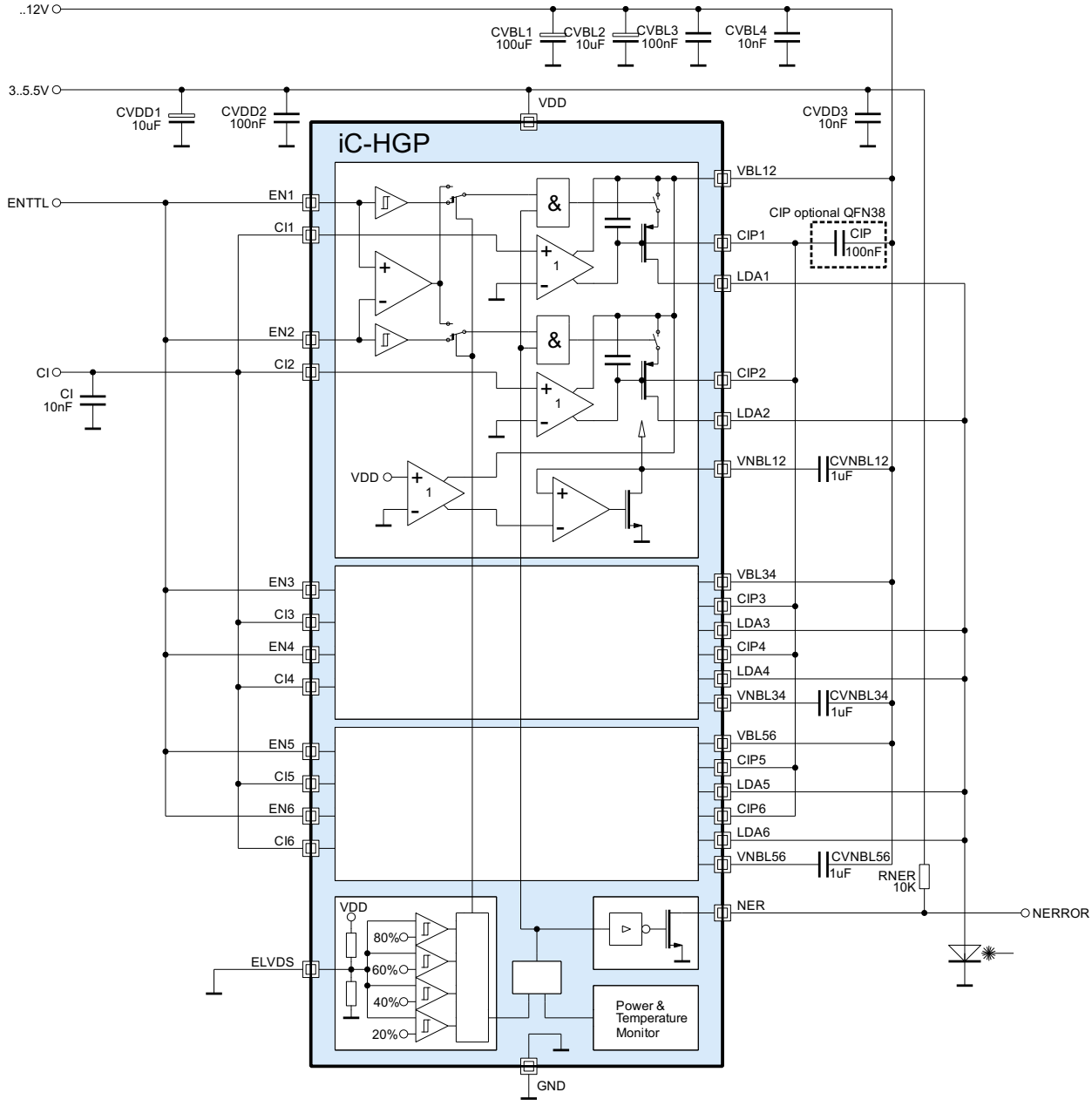

Figure 10: 1 channel TTL fast

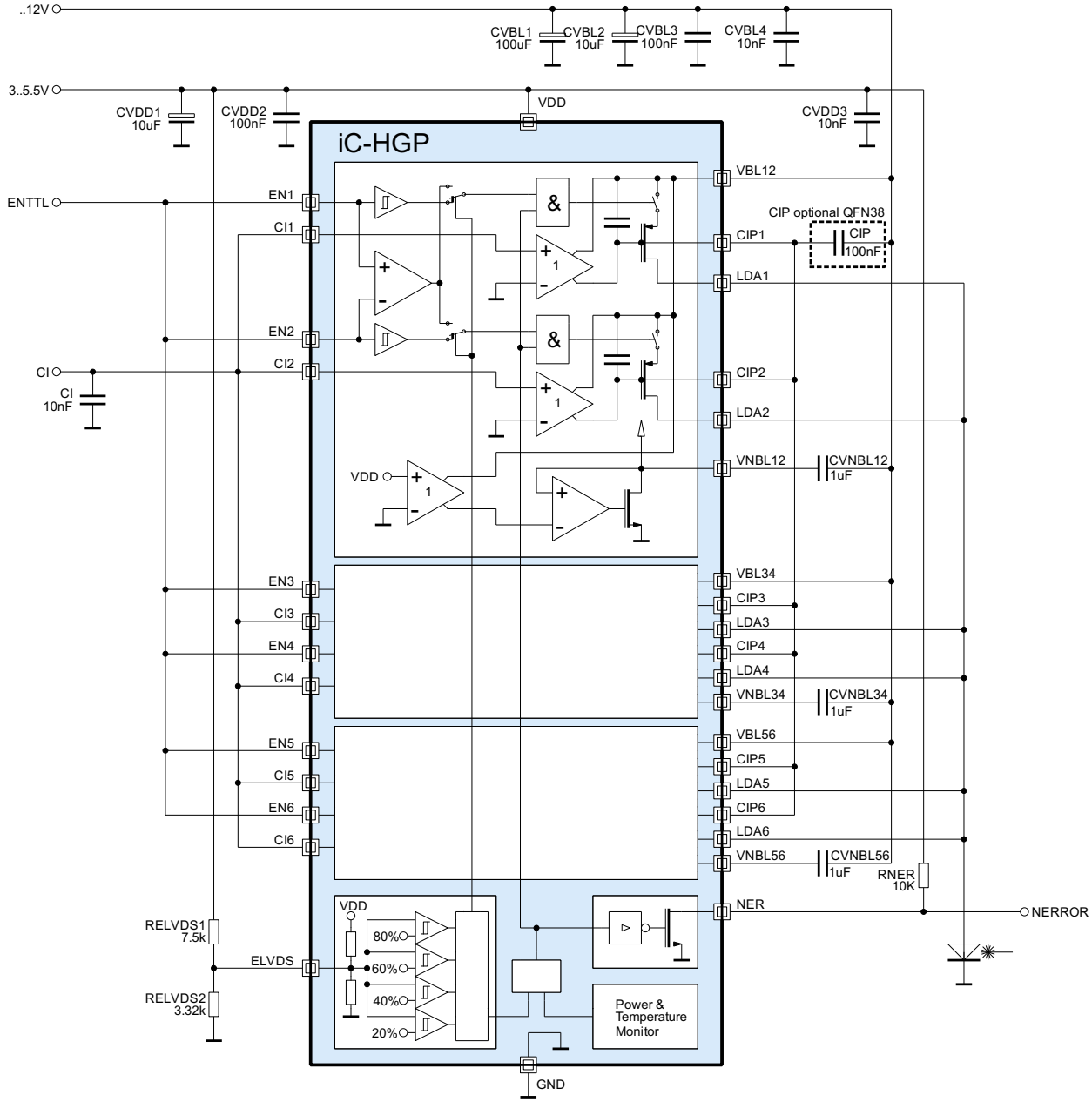

Figure 11: 1 channel TTL slow

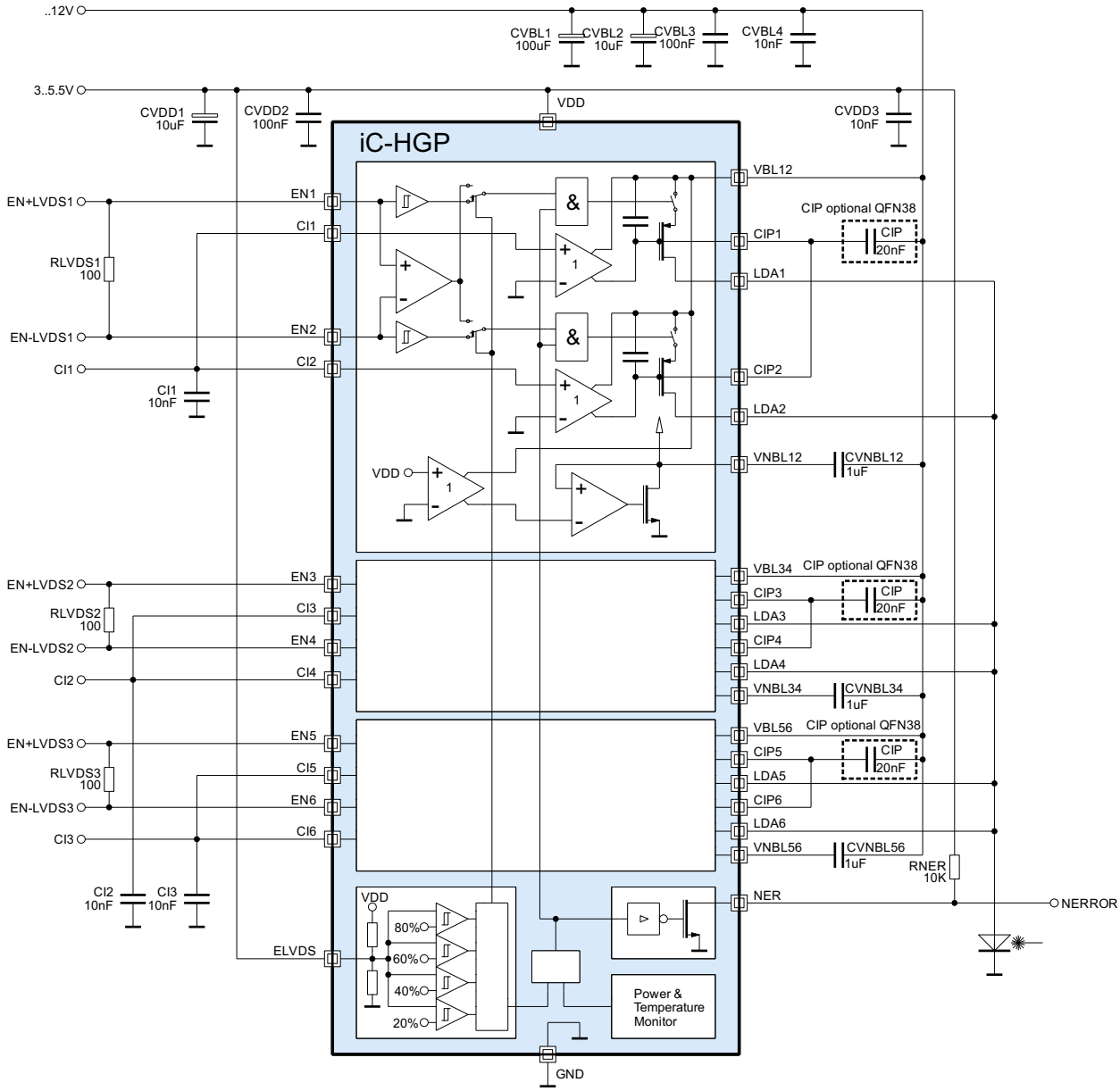

Figure 12: 3 channel LVDS fast

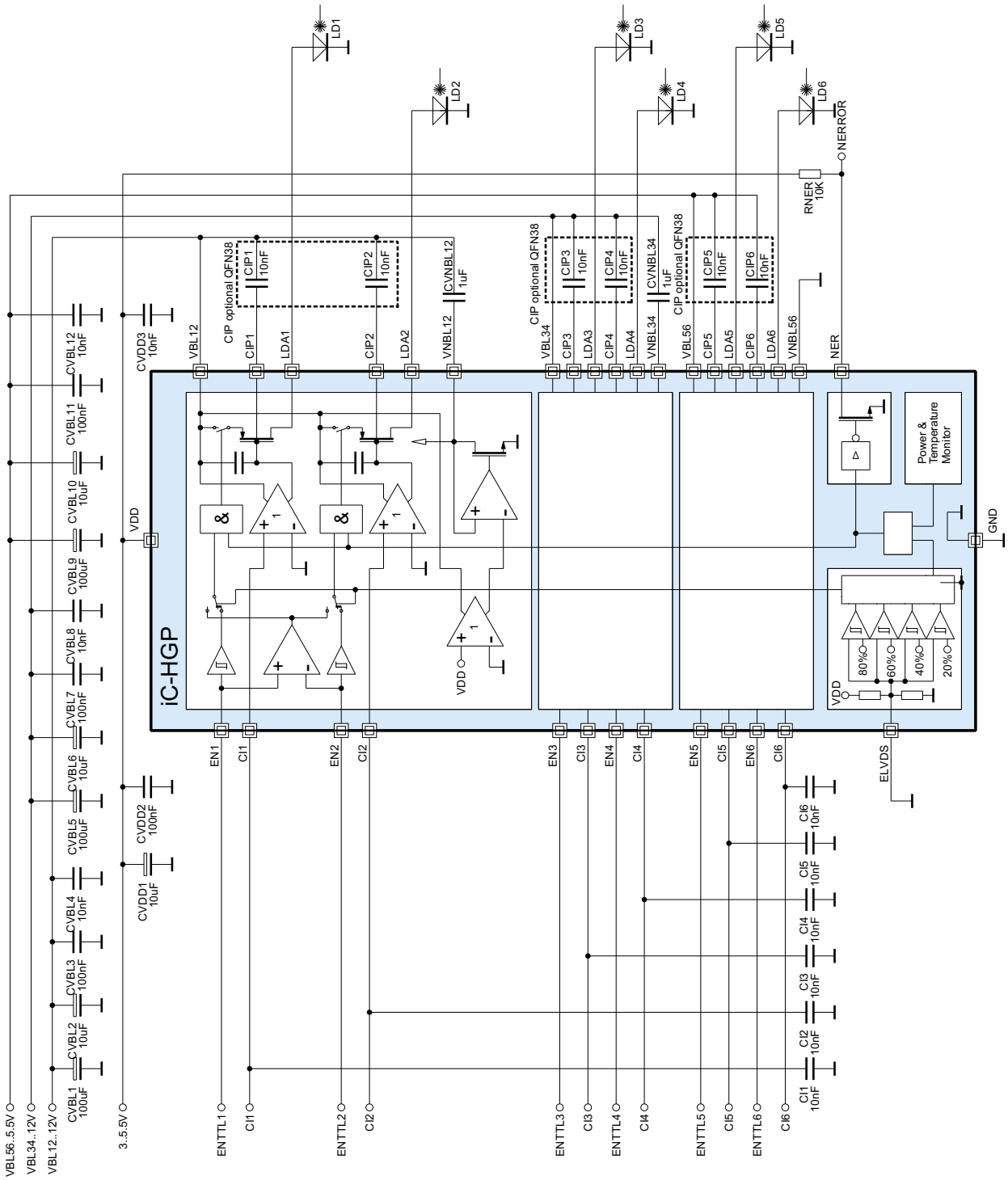

Figure 13: 6 channel TTL fast with 3 separate power supplies VBL12 and VBL34 up to 12 V, VBL56 up to 5.5 V

EVALUATION BOARDS

iC-HGP comes with evaluation boards for test purpose.

Figures 14 and 15 show the schematic and the component side of the evaluation board for the QFN32 package.

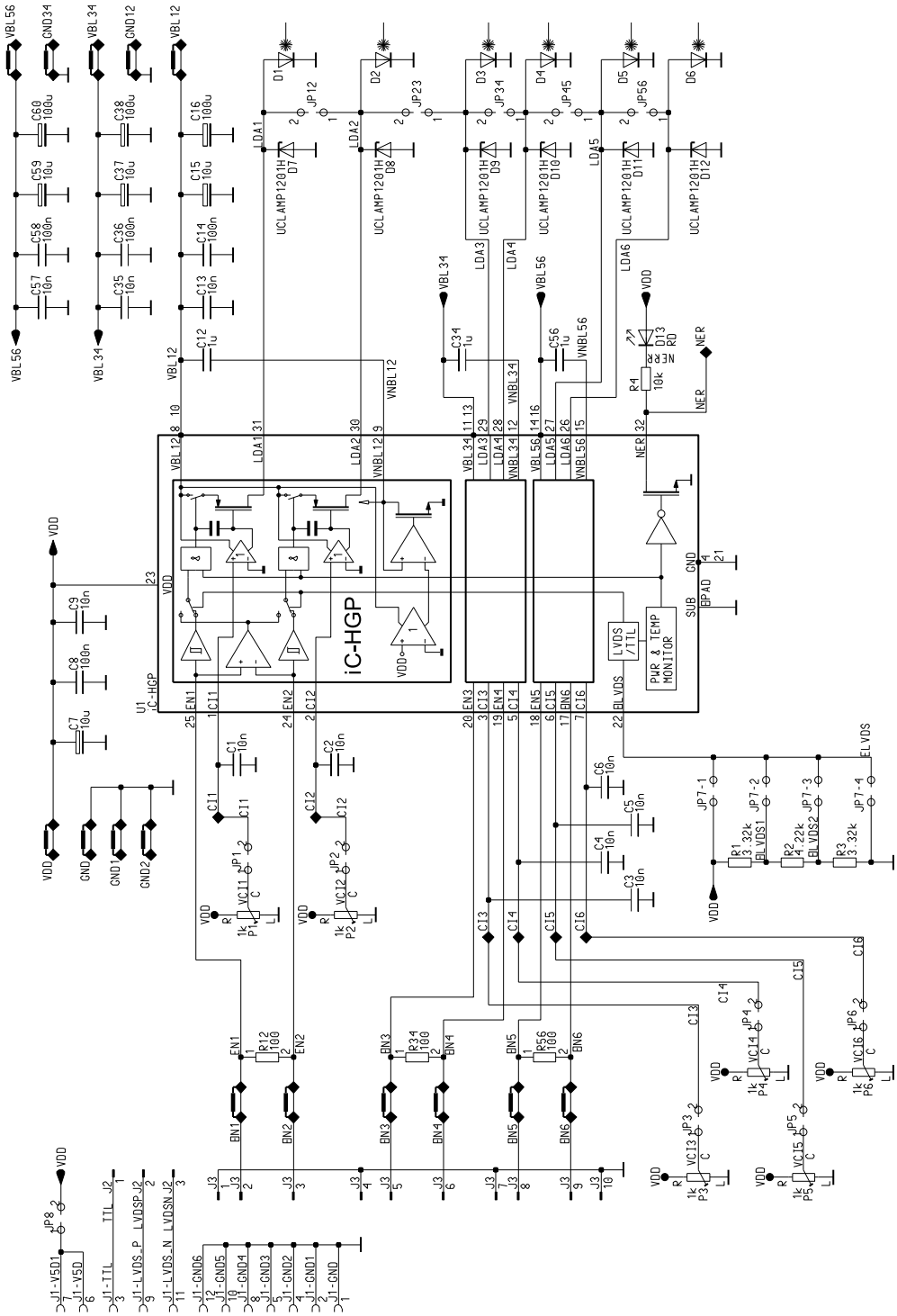

Figure 14: Schematic of the evaluation board

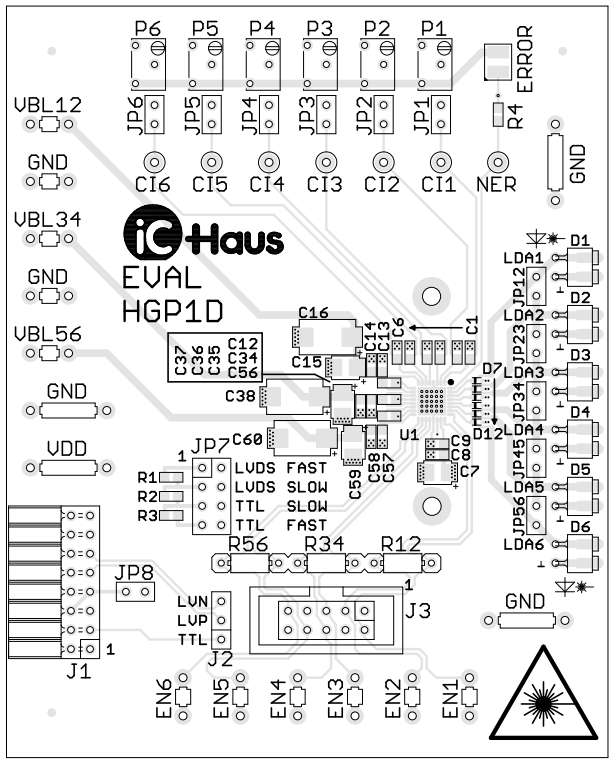

Figure 15: Evaluation board (component side)

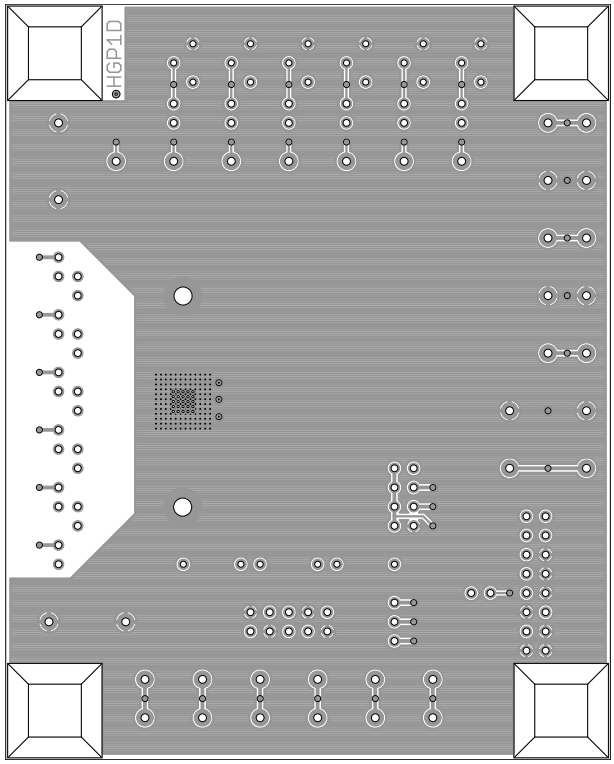

Figure 16: Evaluation board (solder side) with mounting option for heat sink

Figures 17 and 18 show the schematic and the component side of the evaluation board for the QFN38 package.

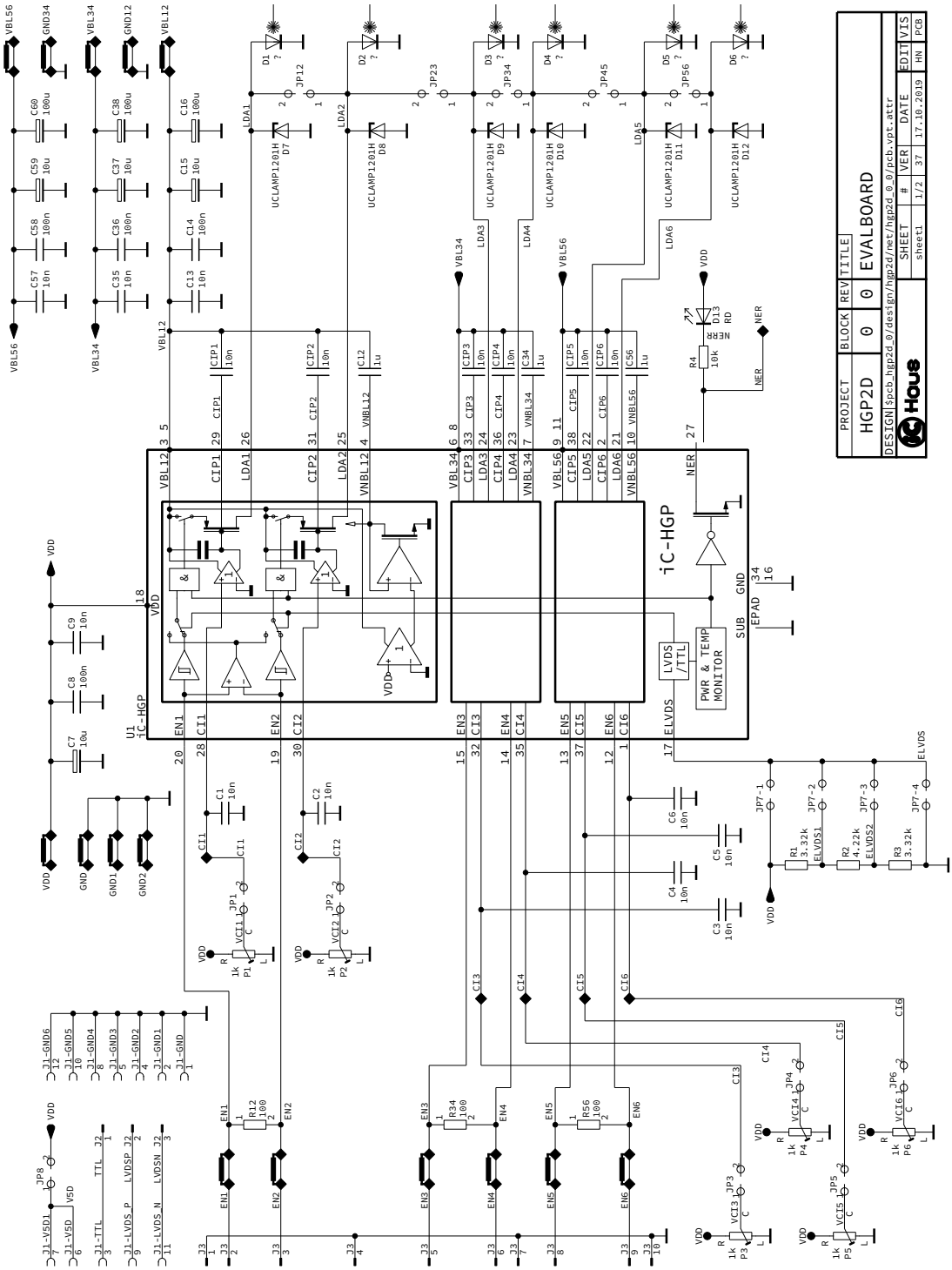

Figure 17: Schematic of the evaluation board

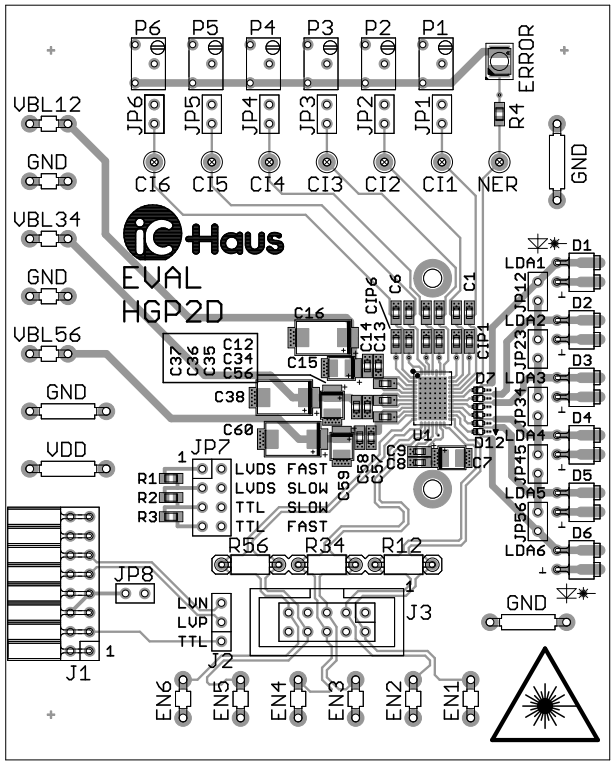

Figure 18: Evaluation board (component side)

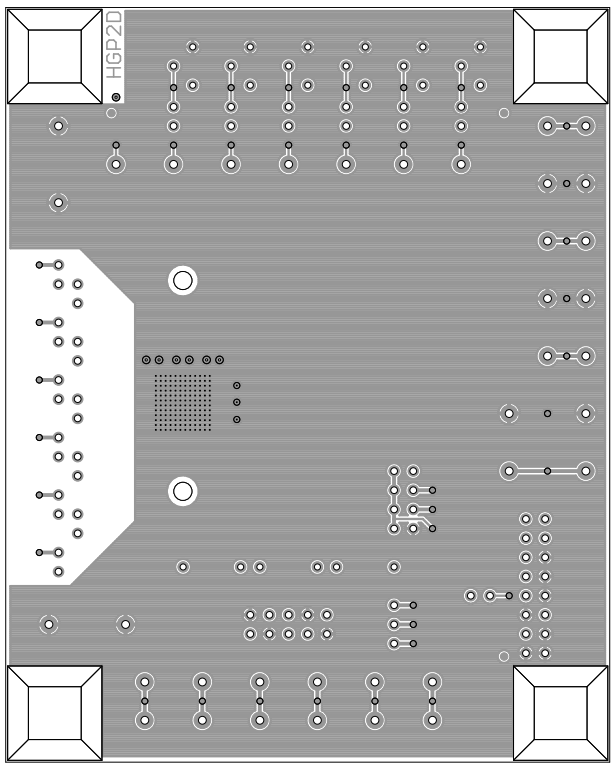

Figure 19: Evaluation board (solder side) with mounting option for heat sink

REVISION HISTORY

Rel.	Rel. Date†	Chapter	Modification	Page
A1	2017-09-05		Initial Release	

Rel.	Rel. Date†	Chapter	Modification	Page
A2	2018-11-20	EVALUATION BOARD	Polarity markers for D1 to D6 added on the component side of the evaluation board (Figure 15).	18

Rel.	Rel. Date†	Chapter	Modification	Page
B1	2020-10-27	BLOCK DIAGRAM	Updated schematic	1
		PACKAGES	QFN38-5x7 package added	1
		PACKAGING INFORMATION	QFN38-5x7 package added	5-6
		ELECTRICAL CHARACTERISTICS	Items No. 012, 116, 118: CIPx added	8
		APPLICATION EXAMPLES	Updated schematics	13-18
		EVALUATION BOARDS	HGP2D added	21-22
		PULSED OPERATION	Hint on package options added.	12

† Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-HGP	QFN32 5 mm x 5 mm	iC-HGP QFN32-5x5
	QFN38 5 mm x 7 mm	iC-HGP QFN32-5x7
	General Purpose Evaluation Board	iC-HGP EVAL HGP1D
	General Purpose Evaluation Board	iC-HGP EVAL HGP2D

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