www.ablic.com

AUTOMOTIVE, 125°C OPERATION, 6 V, VOLTAGE DETECTOR WITH FAST DETECTION RESPONSE AND MANUAL RESET FUNCTION

Rev.1.1_00

This IC, developed using CMOS technology, is a high-accuracy voltage detector. The detection voltage and release voltage are fixed internally with an accuracy of ±1.5%.
Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared, so the output is stable even if the SENSE pin voltage (V_{SENSE}) falls to 0 V.
The release signal can be delayed by setting a capacitor externally, and the release delay time accuracy is ±15% (C_D = 3.3 nF).
This IC also has a manual reset function. The manual reset function changes the comparator input voltage of the internal circuit, and the detector is forcibly put into the detection status. This enables a diagnosis of anomalies in the detector, such as erroneous release.
The output form is Nch open-drain output.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

■ Features

- Detection voltage: 0.6 V to 4.9 V (0.05 V step)
- Detection voltage accuracy: ±1.5%
- Hysteresis width selectable from "Available" / "Unavailable": "Available": 3.0%, 5.0%, 10.0%
  "Unavailable": 0%
- Detection response time: 10.0 μs typ.
- Manual reset function: MR pin input logic: Active "L"
- Release delay time accuracy: ±15% (C_D = 3.3 nF)
- Current consumption: 1.2 μA typ.
- Output form: Nch open-drain output
- Operation voltage range: 2.5 V to 6.0 V
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 in process*1

***1.** Contact our sales representatives for details.

■ Applications

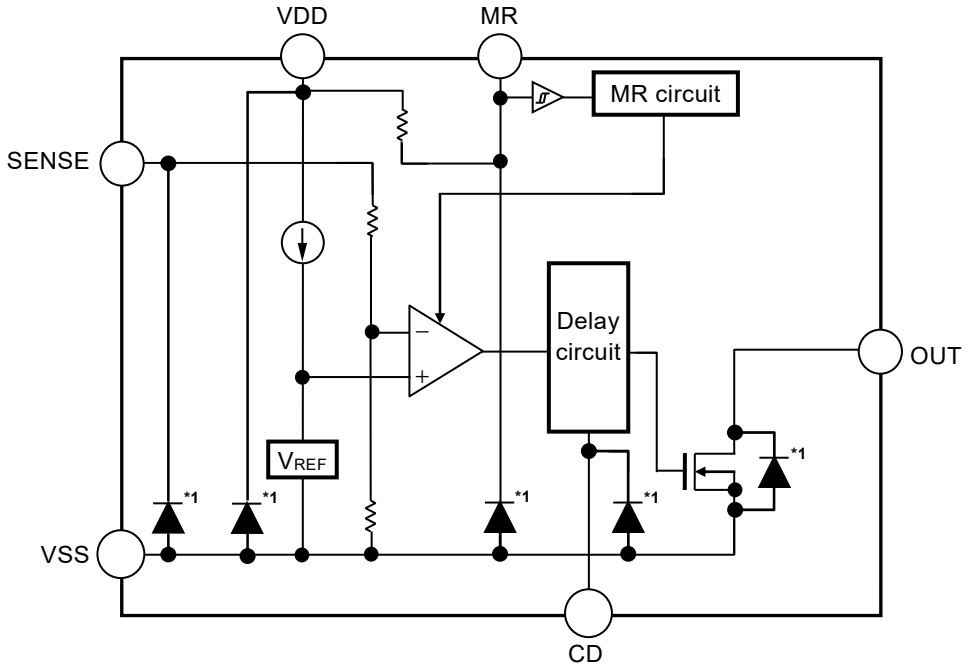
- Voltage detection of power supply for automotive electric component
- Voltage monitoring of automotive ECUs, ADAS and other systems that require failure detection
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

■ Packages

- SOT-23-6
- HSNT-8(1616)B

■ Block Diagrams

1. S-19122 Series A type

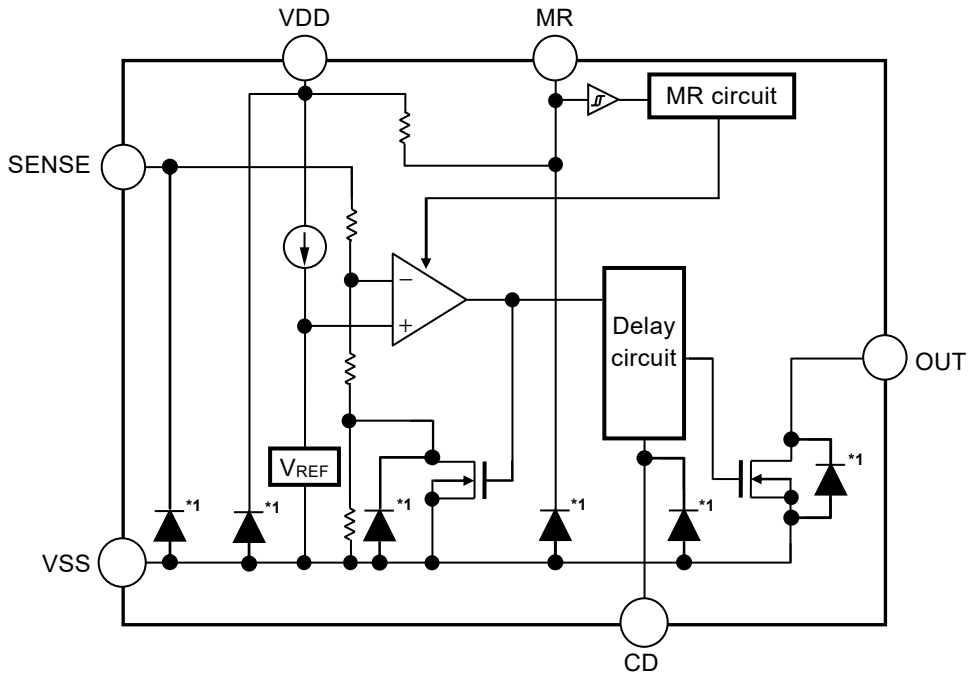


***1.** Parasitic diode

Figure 1

Product Type	Hysteresis Width	MR Pin Input Logic	OUT Pin Output Form	OUT Pin Output Logic
A type	0%	Active "L"	Nch open-drain output	Active "L"

2. S-19122 Series B / C / D type



***1.** Parasitic diode

Figure 2

Product Type	Hysteresis Width	MR Pin Input Logic	OUT Pin Output Form	OUT Pin Output Logic
B type	3%	Active "L"	Nch open-drain output	Active "L"
C type	5%	Active "L"	Nch open-drain output	Active "L"
D type	10%	Active "L"	Nch open-drain output	Active "L"

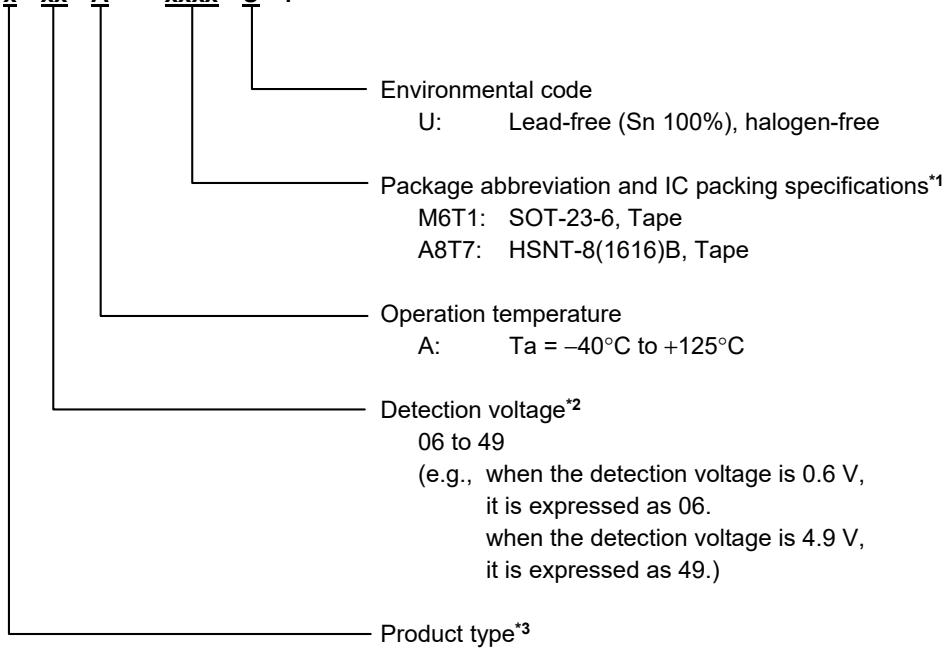
■ AEC-Q100 in Process

Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name

S-19122 x xx A - xxxx U 7



***1.** Refer to the tape drawing.
***2.** If you request the product which has 0.05 V step, contact our sales representatives.
***3.** Refer to "**2. Function list of product types**".

2. Function list of product types

Table 1

Product Type	Hysteresis Width	MR Pin Input Logic	OUT Pin Output Form	OUT Pin Output Logic
A type	0%	Active "L"	Nch open-drain output	Active "L"
B type	3%	Active "L"	Nch open-drain output	Active "L"
C type	5%	Active "L"	Nch open-drain output	Active "L"
D type	10%	Active "L"	Nch open-drain output	Active "L"

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD	–
HSNT-8(1616)B	PY008-B-P-SD	PY008-B-C-SD	PY008-B-R-SD	PY008-B-L-SD

■ Pin Configurations

1. SOT-23-6

Top view

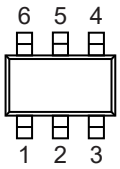


Figure 3

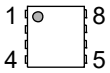
Table 3

Pin No.	Symbol	Description
1	SENSE	Detection voltage input pin
2	VDD	Voltage input pin
3	MR	Manual Reset pin
4	OUT	Voltage detection output pin
5	VSS	GND pin
6	CD*1	Connection pin for release delay time adjustment capacitor

***1.** Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance.

2. HSNT-8(1616)B

Top view



Bottom view

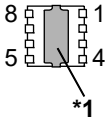


Figure 4

Table 4

Pin No.	Symbol	Description
1	MR	Manual Reset pin
2	VDD	Voltage input pin
3	NC*2	No connection
4	SENSE	Detection voltage input pin
5	CD*3	Connection pin for release delay time adjustment capacitor
6	VSS	GND pin
7	OUT	Voltage detection output pin
8	NC*2	No connection

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.

***2.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

***3.** Connect a capacitor between the CD pin and the VSS pin. The release delay time can be adjusted according to the capacitance.

■ Absolute Maximum Ratings

Table 5

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{DD}	V_{SS} – 0.3 to V_{SS} + 7.0	V
SENSE pin voltage	V_{SENSE}	V_{SS} – 0.3 to V_{SS} + 7.0	V
CD pin input voltage	V_{CD}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
MR pin input voltage	V_{MR}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
Output voltage	V_{OUT}	V_{SS} – 0.3 to V_{SS} + 7.0	V
Output current	I_{OUT}	25	mA
Junction temperature	T_j	–40 to +150	°C
Operation ambient temperature	T_{opr}	–40 to +125	°C
Storage temperature	T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SOT-23-6	Board A	–	159	–	°C/W
			Board B	–	124	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		HSNT-8(1616)B	Board A	–	214	–	°C/W
			Board B	–	172	–	°C/W
			Board C	–	52	–	°C/W
			Board D	–	55	–	°C/W
			Board E	–	43	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 7

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	V_{DET}	V_{DD} = 5.0 V, 0.6 V ≤ $V_{DET(S)}$ ≤ 4.9 V	$V_{DET(S)}$ × 0.985	$V_{DET(S)}$	$V_{DET(S)}$ × 1.015	V	1
Hysteresis width*2	V_{HYS}	A type (V_{HYS} = 0%)	–	V_{DET} × 0.00	–	V	1
		B type (V_{HYS} = 3.0%)	V_{DET} × 0.02	V_{DET} × 0.03	V_{DET} × 0.04	V	1
		C type (V_{HYS} = 5.0%)	V_{DET} × 0.04	V_{DET} × 0.05	V_{DET} × 0.06	V	1
		D type (V_{HYS} = 10.0%)	V_{DET} × 0.09	V_{DET} × 0.10	V_{DET} × 0.11	V	1
Current consumption	I_{SS1}	V_{DD} = 5.0 V, V_{SENSE} = $V_{DET(S)}$ + 1 V	–	1.2	2.3	μA	5
Operation voltage	V_{DD}	–	2.5	–	6.0	V	1
Output current	I_{OUT}	OUT pin Nch driver, V_{DD} = 2.5 V, V_{DS}*3 = 0.5 V, V_{SENSE} = $V_{DET(S)}$ – 0.5 V	2.50	–	–	mA	2
Leakage current	I_{LEAK}	OUT pin Nch driver, V_{DD} = 6.0 V, V_{OUT} = 6.0 V, V_{SENSE} = 6.0 V	–	–	0.10	μA	2
Detection response time*4	t_{RESET}	–	–	10.0	40.0	μs	3
Release delay time*5	t_{DELAY}	C_D = 3.3 nF	8.5	10.0	11.5	ms	3
SENSE pin resistance	R_{SENSE}	–	6.0	–	85.0	MΩ	5
MR pin input voltage "H"	V_{MRH}	–	2.0	–	–	V	4
MR pin input voltage "L"	V_{MRL}	–	–	–	0.6	V	4
MR pin resistance	R_{MR}	–	0.91	2.20	5.71	MΩ	4
CD pin discharge ON resistance	R_{CDD}	V_{DD} = 2.5 V, V_{CD} = 0.7 V	0.15	–	0.90	kΩ	–

***1.** V_{DET}: Actual detection voltage value, $V_{DET(S)}$: Set detection voltage value

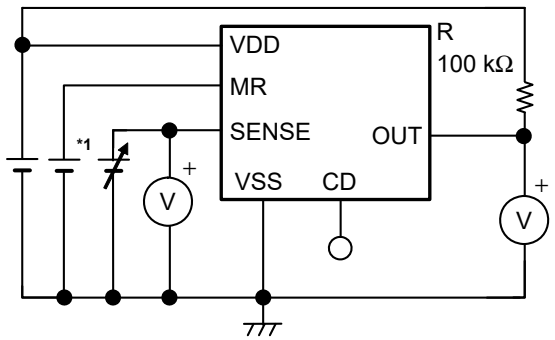
***2.** The Release voltage (V_{REL}) is as follows.
A type (hysteresis width "Unavailable"): $V_{REL} = V_{DET}$
B / C / D type (hysteresis width "Available"): $V_{REL} = V_{DET} + V_{HYS}$

***3.** V_{DS}: Drain-to-source voltage of the output transistor

***4.** The time period from when the pulse voltage of $V_{DET(S)}$ + 0.5 V → $V_{DET(S)}$ – 0.5 V is applied to the SENSE pin after V_{SENSE} reaches the release voltage once, until V_{OUT} reaches 50% of V_{DD}.

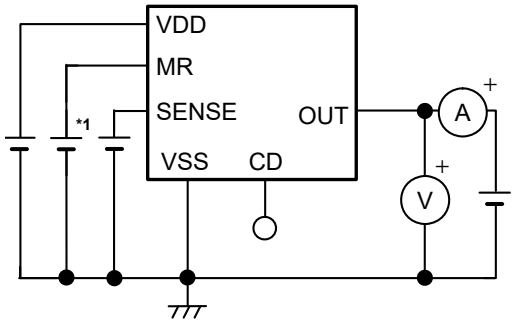
***5.** $V_{REL(S)}$: Set release voltage value
The time period from when the pulse voltage of $V_{REL(S)}$ – 0.5 V → $V_{REL(S)}$ × 1.03 V is applied to the SENSE pin to when V_{OUT} reaches 50% of V_{DD}.

■ Test Circuits



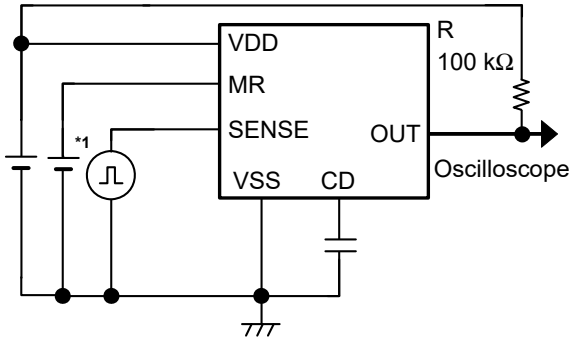
***1.** Set to V_{DD}

Figure 5 Test Circuit 1



***1.** Set to V_{DD}

Figure 6 Test Circuit 2



***1.** Set to V_{DD}

Figure 7 Test Circuit 3

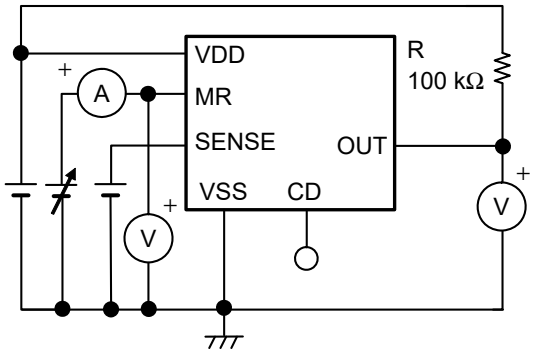
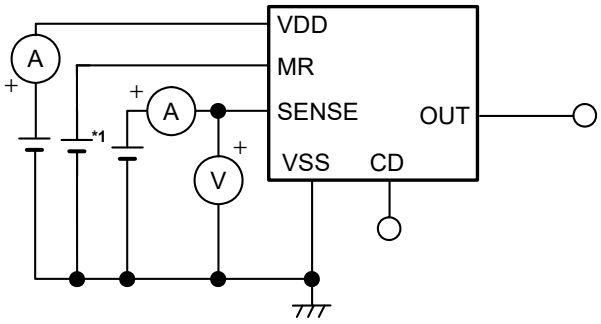


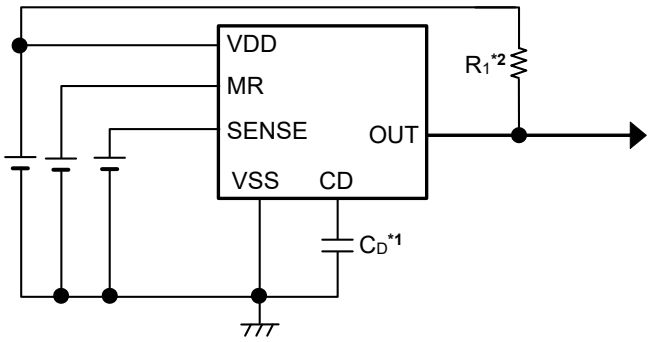
Figure 8 Test Circuit 4



***1.** Set to V_{DD}

Figure 9 Test Circuit 5

■ Standard Circuit



***1.** C_D is a release delay time adjustment capacitor. The C_D should be connected directly to the CD pin and the VSS pin.
***2.** R_1 is the external pull-up resistors for the output pin.

Figure 10

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

■ Condition of Application

Release delay time adjustment capacitor (C_D): A ceramic capacitor with capacitance of 0.33 nF or more is recommended.

■ Selection of Release Delay Time Adjustment Capacitor (C_D)

In this IC, the release delay time adjustment capacitor (C_D) is necessary between the CD pin and the VSS pin to adjust the release delay time (t_{DELAY}) of the detector. Refer to "**3. Delay circuit**" in "**■ Operation**" for details.

Caution Perform thorough evaluation including the temperature characteristics with an actual application to select C_D.

■ Explanation of Terms

1. Detection voltage (V_{DET})

The detection voltage is a SENSE pin voltage at which the output voltage in **Figure 13** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum and the maximum is called the detection voltage range (Refer to "**Figure 11 Detection Voltage**").

Example: In V_{DET} = 4.0 V product, the detection voltage is at any point in the range of 3.940 V ≤ V_{DET} ≤ 4.060 V.
This means that some V_{DET} = 4.0 V product has V_{DET} = 3.940 V and some has V_{DET} = 4.060 V.

2. Release voltage (V_{REL})

The release voltage is a SENSE pin voltage at which the output voltage in **Figure 13** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum and the maximum is called the release voltage range (Refer to "**Figure 12 Release Voltage**").
The release voltage becomes the value differs from the detection voltage within the range shown below.

- B type: 2% to 4% (3% typ.)
- C type: 4% to 6% (5% typ.)
- D type: 9% to 11% (10% typ.)

Example: For D type, V_{DET} = 4.0 V product, the release voltage is at any point in the range of 4.294 V ≤ V_{REL} ≤ 4.507 V despite V_{REL} = 4.400 V typ.
This means that some D type, V_{DET} = 4.0 V product has V_{REL} = 4.294 V and some has V_{REL} = 4.507 V.

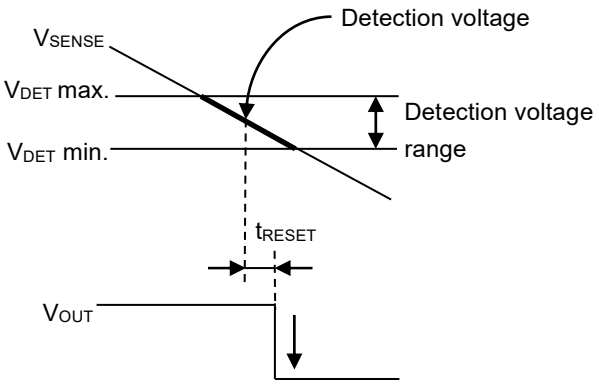


Figure 11 Detection Voltage

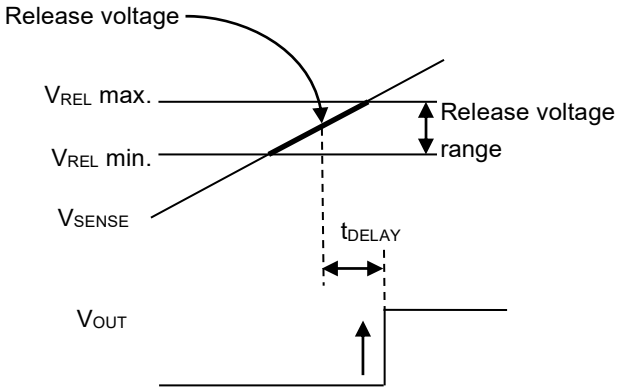


Figure 12 Release Voltage

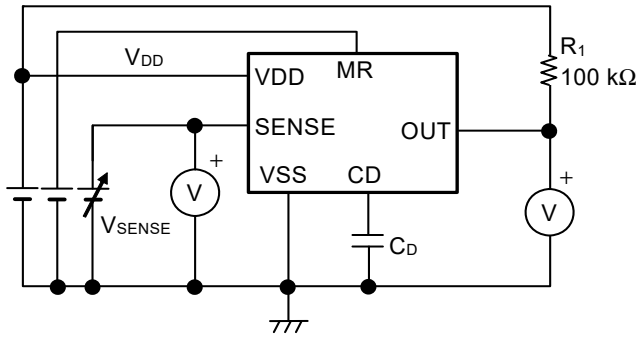


Figure 13 Test Circuit of Detection Voltage and Release Voltage

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage (V_{DET}) and the release voltage (V_{REL}). Voltage difference between V_{REL} and V_{DET} is the hysteresis width (V_{HYS}*1) of the OUT pin. Setting the hysteresis width between V_{DET} and V_{REL}, prevents malfunction caused by noise on the input voltage.

***1.** Refer to "**1. 2 S-19122 Series B / C / D type**" in "■ **Operation**" for details.

4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector.

■ Operation

1. Basic operation

Figure 14 and **Figure 16** show that the OUT pin being pulled up by resistors (R_1) is an example of basic operation.

1. 1 S-19122 Series A type

(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage (V_{REL}) or higher, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up.

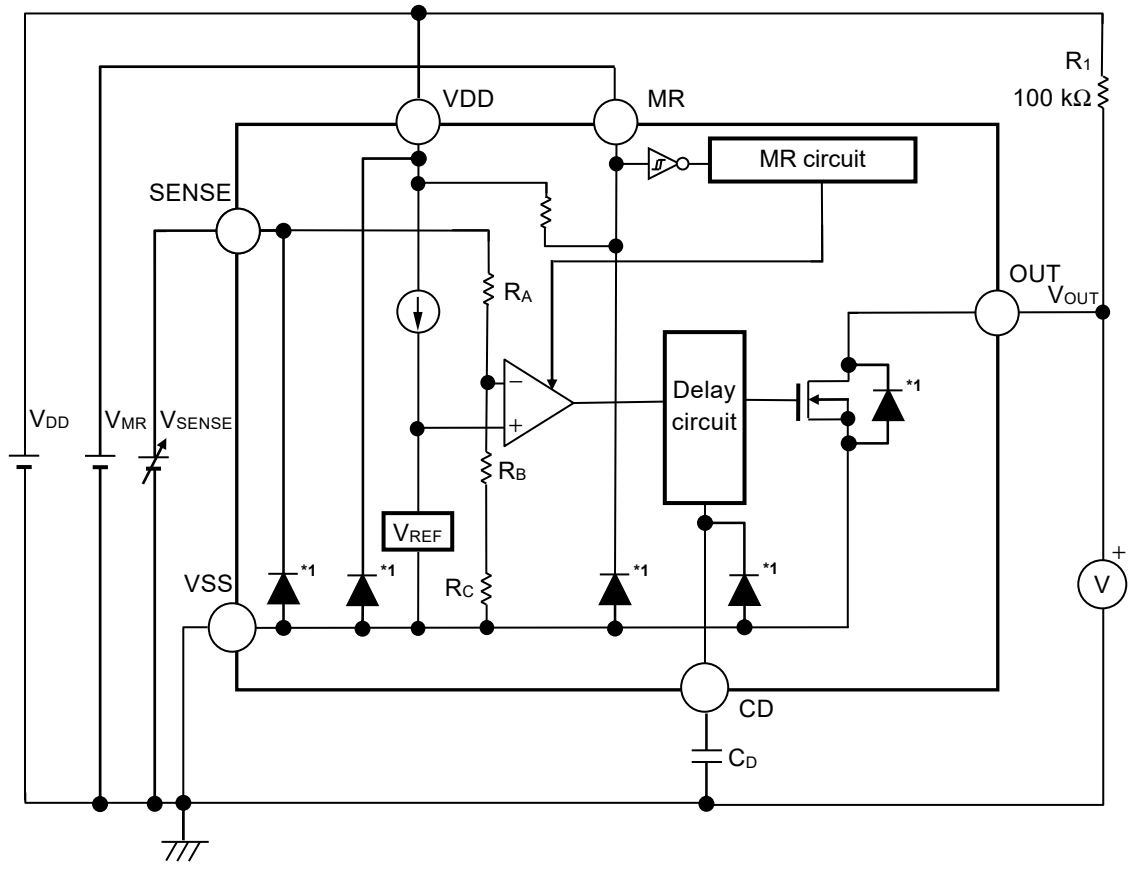
At this time, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) When V_{SENSE} decreases to the detection voltage (V_{DET}) or lower (point A in **Figure 15**), the Nch transistor is turned on. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection response time (t_{RESET}).

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

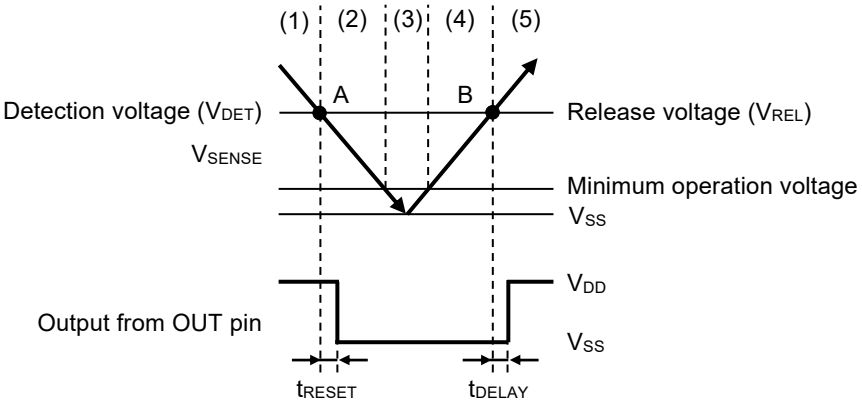
(4) Even if V_{SENSE} increases, V_{SS} is output when V_{SENSE} is lower than V_{REL}.

(5) When V_{SENSE} increases to V_{REL} or higher (point B in **Figure 15**), the Nch transistor is turned off. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}) when the output is pulled up.



***1.** Parasitic diode

Figure 14 Operation of S-19122 Series A type



Remark The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 15 Timing Chart of S-19122 Series A Type

1. 2 S-19122 Series B / C / D type

(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage (V_{REL}) or higher, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up.

Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

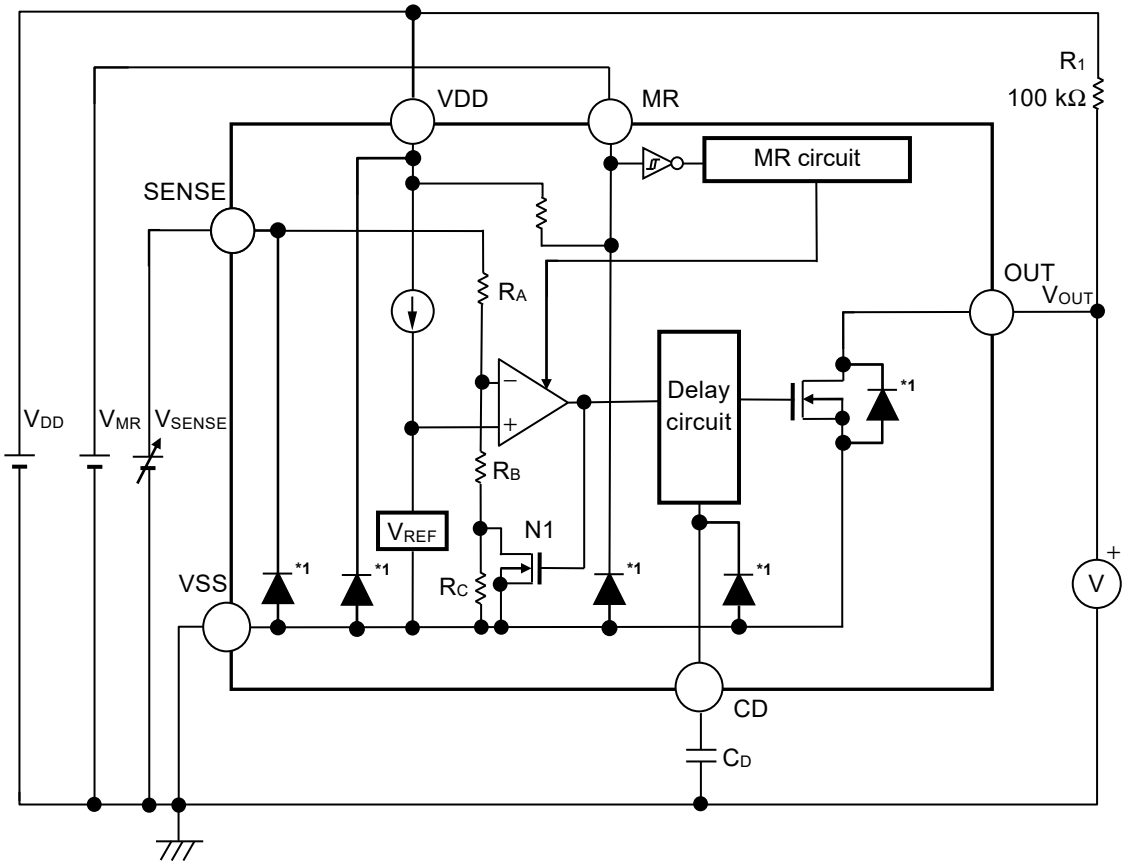
(2) Even if V_{SENSE} decreases to V_{REL} or lower, V_{DD} is output when V_{SENSE} is higher than the detection voltage (V_{DET}). When V_{SENSE} decreases to V_{DET} or lower (point A in **Figure 17**), the Nch transistor is turned on. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection response time (t_{RESET}).

At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

(4) Even if V_{SENSE} exceeds V_{DET}, V_{SS} is output when V_{SENSE} is lower than V_{REL}.

(5) When V_{SENSE} increases to V_{REL} or higher (point B in **Figure 17**), the Nch transistor is turned off. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{DELAY}) when the output is pulled up.



***1.** Parasitic diode

Figure 16 Operation of S-19122 Series B / C / D type

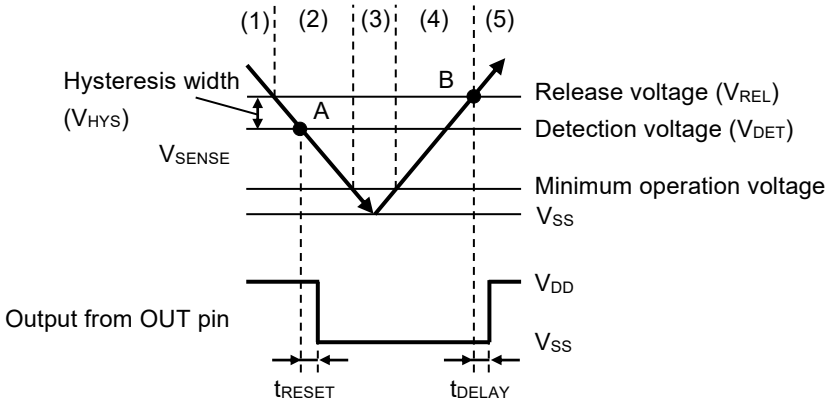


Figure 17 Timing Chart of S-19122 Series B / C / D type

2. SENSE pin

The SENSE pin is the input pin for the detection voltage. The power supply VDD pin and SENSE pin, for voltage detection, are divided. Therefore, as long as a voltage is supplied to the VDD pin, the reset signal will be held even if the input voltage to the SENSE pin drops below the minimum operation voltage.

2. 1 Error when detection voltage is set externally

The detection voltage can be set externally by connecting a node that was resistance-divided by the resistor (R_A) and the resistor (R_B) to the SENSE pin as shown in **Figure 18**.
For conventional products without the SENSE pin, external resistor cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if external resistor is large, problems such as oscillation or larger error in the hysteresis width may occur.
In this IC, R_A and R_B in **Figure 18** are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance (R_{SENSE}) that will occur.
Although R_{SENSE}*1 in this IC is large to make the error small, R_A and R_B should be selected such that the error is within the allowable limits.

***1.** 6.0 MΩ min.

2. 2 Selection of R_A and R_B

In **Figure 18**, the relation between the external setting detection voltage (V_{DX}) and the actual detection voltage (V_{DET}) is ideally calculated by the equation below.

$$V_{DX} = V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) \cdots\cdots(1)$$

However, in reality there is an error in the current flowing through R_{SENSE}.
When considering this error, the relation between V_{DX} and V_{DET} is calculated as follows.

$$\begin{aligned} V_{DX} &= V_{DET} \times \left(1 + \frac{R_A}{R_B \,||\, R_{SENSE}}\right) \\ &= V_{DET} \times \left(1 + \frac{R_A}{\dfrac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right) \\ &= V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times V_{DET} \cdots\cdots(2) \end{aligned}$$

By using equations (1) and (2), the error is calculated as $V_{DET} \times \frac{R_A}{R_{SENSE}}$.
The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100\ [\%] = \frac{R_A \,||\, R_B}{R_{SENSE}} \times 100\ [\%] \cdots(3)$$

As seen in equation (3), the smaller the resistance values of R_A and R_B compared to R_{SENSE}, the smaller the error rate becomes.

Also, the relation between the external setting hysteresis width (V_{HX}) and the hysteresis width (V_{HYS}) is calculated by equation below. Error due to R_{SENSE} also occurs to the relation in a similar way to the detection voltage.

$$V_{HX} = V_{HYS} \times \left(1 + \frac{R_A}{R_B}\right) \cdots\cdots(4)$$

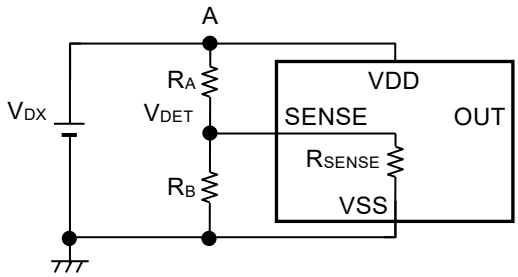


Figure 18 Detection Voltage External Setting Circuit

Caution If R_A and R_B are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.

3. Delay circuit

The delay circuit has a function that adjusts the release delay time (t_{DELAY}) from when the SENSE pin voltage (V_{SENSE}) reaches the release voltage ($V_{REL} = V_{DET} + V_{HYS}$) or higher to when the output from OUT pin inverts.
t_{DELAY} is determined by the delay coefficient, the release delay time adjustment capacitor (C_D) and the release delay time when the CD pin is open (t_{DELAY0}). They are calculated by the equation below.

t_{DELAY} [ms] = Delay coefficient × C_D [nF] + t_{DELAY0} [ms]

Table 8

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +125°C	2.64	2.90	3.24
Ta = +25°C	2.67	3.00	3.18
Ta = –40°C	2.72	3.00	3.34

Table 9

Operation Temperature	Release Delay Time when CD Pin is Open (t_{DELAY0})		
	Min.	Typ.	Max.
Ta = +125°C	0.05	0.09	0.24
Ta = +25°C	0.05	0.10	0.22
Ta = –40°C	0.06	0.11	0.27

The release delay time ($t_{DELAYMR}$) during operation of the manual reset function is determined by the delay coefficient, the release delay time adjustment capacitor (C_D), and the release delay time ($t_{DELAYMR0}$) when the CD pin is open during operation of the manual reset function. They are calculated by the equation below.

$t_{DELAYMR}$ [ms] = Delay coefficient × C_D [nF] + $t_{DELAYMR0}$ [ms]

Table 10

Operation Temperature	Release Delay Time ($t_{DELAYMR0}$) When the CD Pin is Open During Operation of the Manual Reset Function		
	Min.	Typ.	Max.
Ta = +125°C	0.04	0.19	0.41
Ta = +25°C	0.05	0.26	0.62
Ta = –40°C	0.06	0.35	0.70

Caution 1. Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.
2. There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value (approximately 160 nA). The leakage current may cause error in delay time. When the leakage current is larger than the built-in constant current, no detect or release takes place.
3. The above equations will not guarantee successful operation. Determine the capacitance of C_D through thorough evaluation including temperature characteristics in the actual usage conditions.

4. Manual reset function

This IC has a manual reset function that can forcibly switch to the detection status.
This IC can activate the manual reset function by applying "L" to the MR pin from the outside.
The manual reset function changes the input voltage of the comparator when an external input signal is received from the MR pin. The manual reset function changes the comparator input voltage of the internal circuit, and the detector is forcibly put into the detection status.
Use of the manual reset function when SENSE pin voltage is held within the release voltage range makes it possible to monitor the OUT pin output logic signal to confirm that the comparator circuit, delay circuit and output transistor are operating normally.

4. 1 MR pin

The MR pin input voltage (V_{MR}) forces the OUT pin voltage (V_{OUT}) to "L".
If the manual reset function is disabled, set the MR pin input voltage (V_{MR}) to "H" or to open.
When the MR pin is open (floating status), the MR pin resistor (R_{MR}) causes the MR pin to be internally pulled up to the VDD pin raising it to V_{DD} level. Also, take care when 0.6 V to V_{DD} min. − 0.3 V voltage is applied to the MR pin as this increases current consumption.

The structure of the MR pin is shown in **Figure 19**.
Note that when the MR pin is set to "L" level, current relative to MR pin resistance (R_{MR} = 2.2 MΩ typ.) in **Table 7** in "■ **Electrical Characteristics**" and VDD pin voltage (V_{DD}) will flow to the MR pin.

Table 11

MR Pin	Internal Circuit	OUT Pin Output Logic	Current Consumption
"H" or open: OFF	Normal operation	Depends on specific status*1	I_{SS1}
"L": ON	Forced detection	"L"	$I_{SS1} + V_{DD} / R_{MR}$

***1.** For details, refer to "**4. 2 Manual reset operation**".

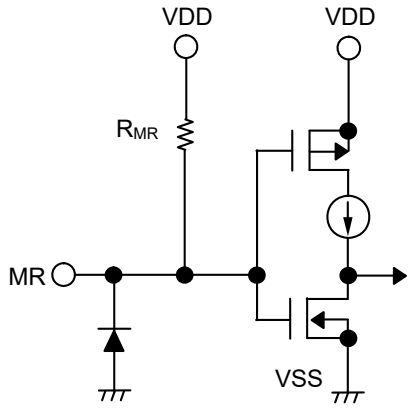


Figure 19

4. 2 Manual reset operation

Figure 20 shows a timing chart for the manual reset function.

Operation of the manual reset function when the SENSE pin voltage (V_{SENSE}) is higher than the release voltage (V_{REL}) is shown below.

(1) When a voltage lower than MR pin input voltage "L" (V_{MRL}) is applied to the MR pin, the output from the OUT pin becomes "L" and the detector switches from release status to detection status after the detection response time ($t_{RESETMR}$) = 50.0 µs max. during operation of the manual reset function has elapsed. Apply a voltage of V_{MRL} or less for at least 50.0 µs.
(2) When a voltage higher than MR pin input voltage "H" (V_{MRH}) is applied to the MR pin, the output from the OUT pin becomes "H" and the detector switches from detection status to release status after the release delay time ($t_{DELAYMR}$) during operation of the manual reset function has elapsed. Be sure to maintain V_{MRH} during $t_{DELAYMR}$. Refer to "**3. Delay circuit**" in "■ **Operation**" for details on $t_{DELAYMR}$.

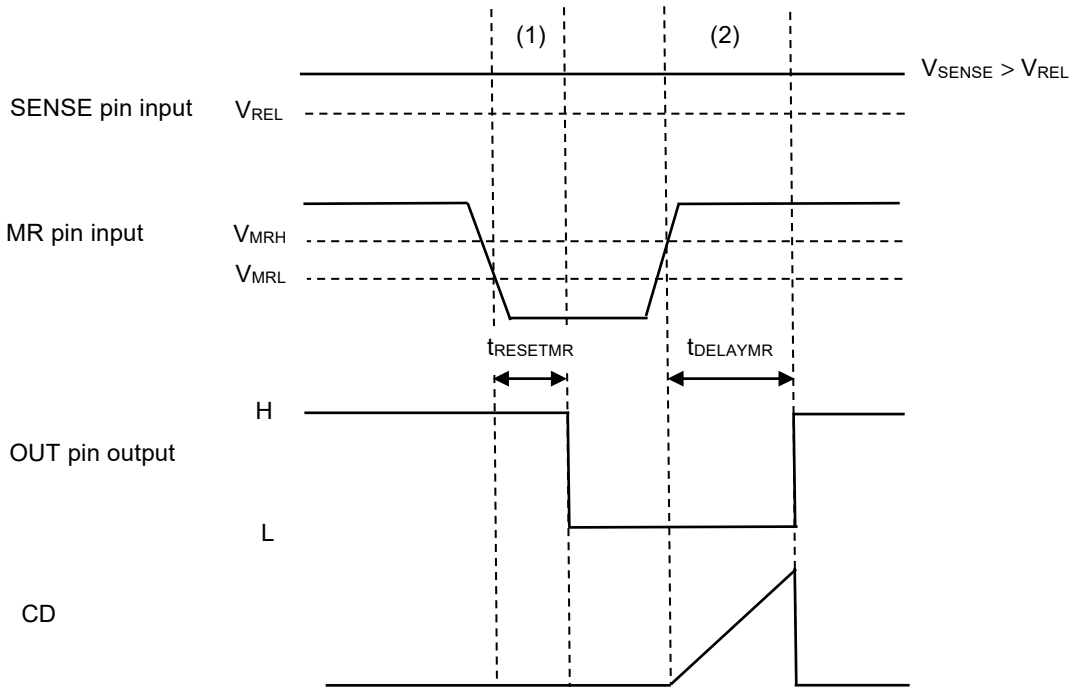


Figure 20

4. 3 When connecting a resistor (R_A) between the supply voltage (V_{DD}) and the VDD / SENSE pins

When the VDD and SENSE pins of the IC are shorted and the MR pin input voltage (V_{MR}) is at an intermediate potential ($V_{MRL} < V_{MR} < V_{MRH}$), the current consumption increases by 35.7 μA max. This current flows through R_A and causes a voltage drop.
When this voltage drop causes the VDD pin voltage (V_{IN}) to fall below the detection voltage (V_{DET}), the detector switches to the detection status, and may not be able to switch to the release status unless the supply voltage (V_{DD}) is increased.
When $V_{IN} > V_{MR}$, current also flows through the MR pin input resistor (R_{MR}). For example, when V_{IN} = 6 V, V_{MR} = 1 V, and R_{MR} = 0.91 MΩ min., a current of 5.5 μA flows from the VDD pin to the MR pin. Therefore, set R_A to satisfy the following equation.

$R_A \leq (V_{DD} - (V_{DET})) / (35.7\ \mu A + \text{MR pin current})$

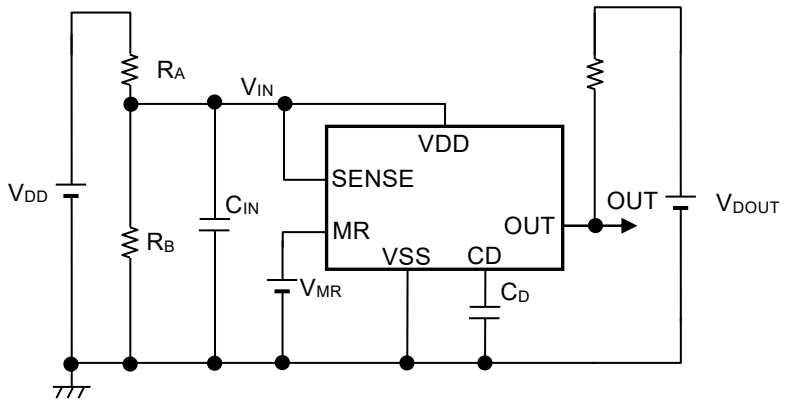


Figure 21

■ Usage Precautions

1. Feed-through current at the time of detection and release

In this IC, a feed-through current flows instantaneously at the time of detection and release. Therefore, if the input impedance is increased, oscillation may occur due to the voltage drop caused by the feed-through current.
When this IC is used in the configuration shown in **Figure 22**, the input impedance is recommended to be 1 kΩ or less.
Perform a sufficient evaluation including the temperature characteristics under the actual operating conditions.

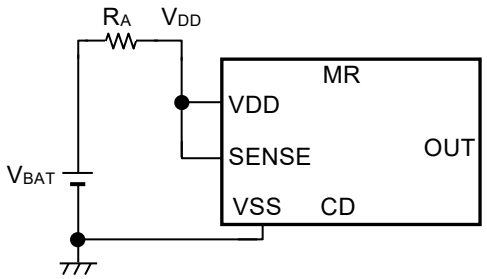


Figure 22

2. Power on sequence

Turn on the power in one of the following two procedures.

(1) Order of VDD pin and SENSE pin (Refer to **Figure 23**)
(2) VDD pin and SENSE pin at the same time

When $V_{SENSE} \geq V_{REL}$ applies, output voltage (V_{OUT}) becomes "H", and the detector enters release status.

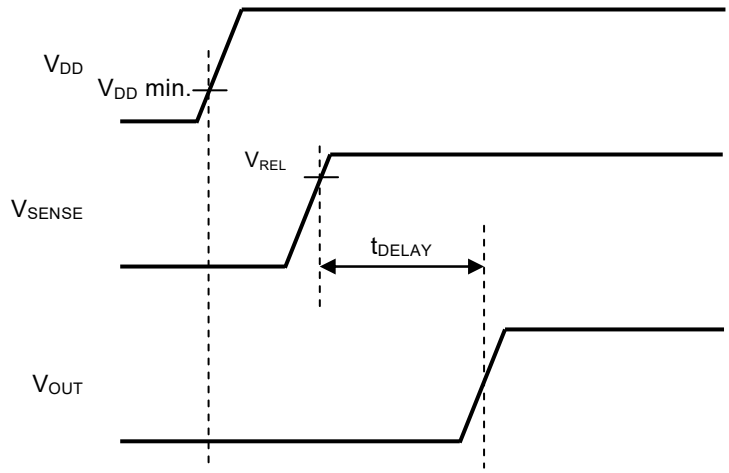


Figure 23

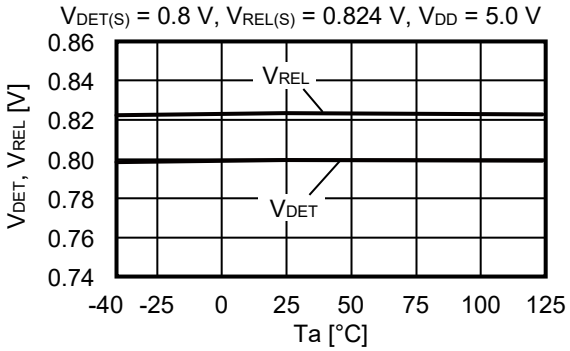
Caution When the SENSE pin is turned on before the VDD pin, a release may mistakenly occur even if V_{SENSE} is less than V_{REL}.

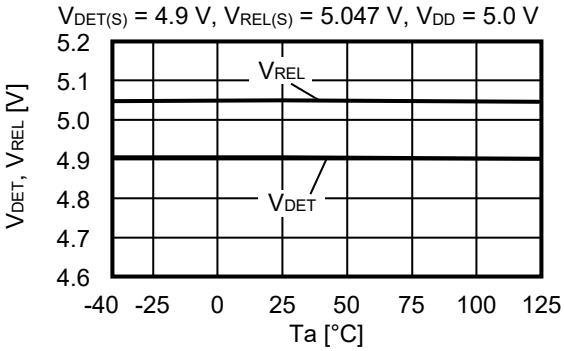
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Because the SENSE pin has a high impedance, malfunctions may occur due to noise.
  Be careful of wiring adjoining SENSE pin wiring in actual applications.
- When using the manual reset function, be sure to hold MR pin input voltage "L" (V_{MRL}) for 50.0 μs or longer. Be careful if the V_{MRL} is held for less than 50.0 μs, because the internal logic may not be established and a malfunction could occur.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

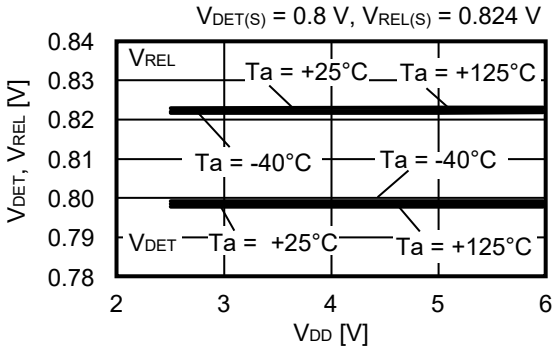
■ Characteristics (Typical Data)

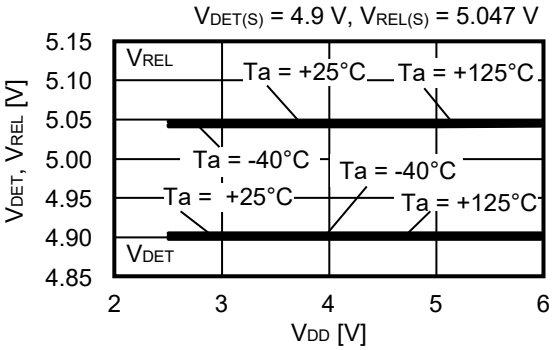
1. Detection voltage (V_{DET}), Release voltage (V_{REL}) vs. Temperature (Ta)



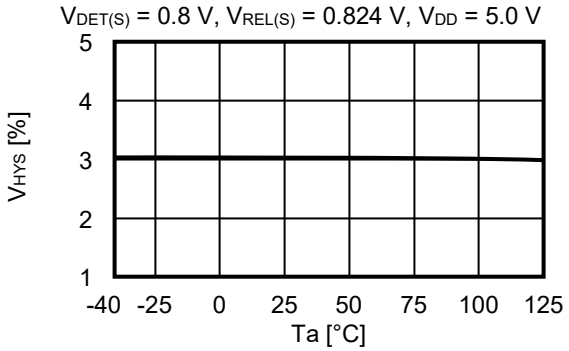


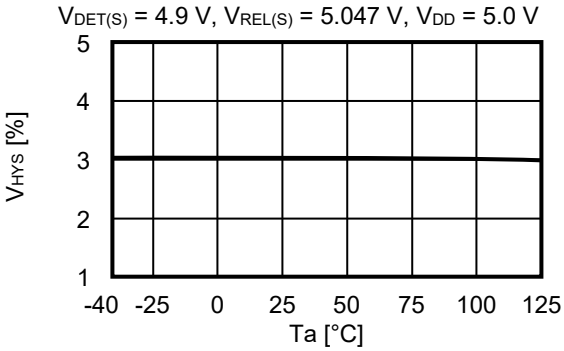
2. Detection voltage (V_{DET}), Release voltage (V_{REL}) vs. Power supply voltage (V_{DD})



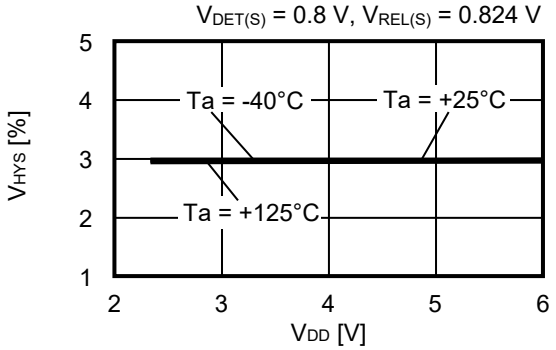


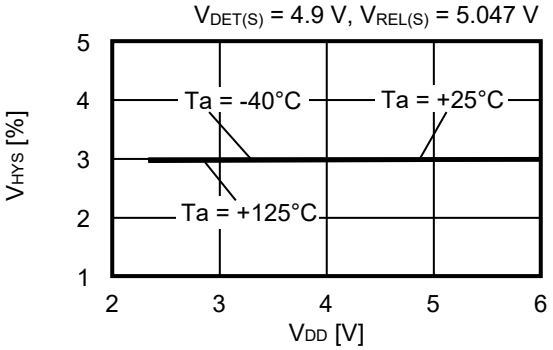
3. Hysteresis width (V_{HYS}) vs. Temperature (Ta)





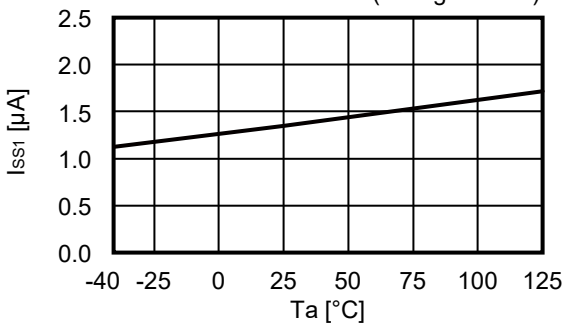
4. Hysteresis width (V_{HYS}) vs. Power supply voltage (V_{DD})



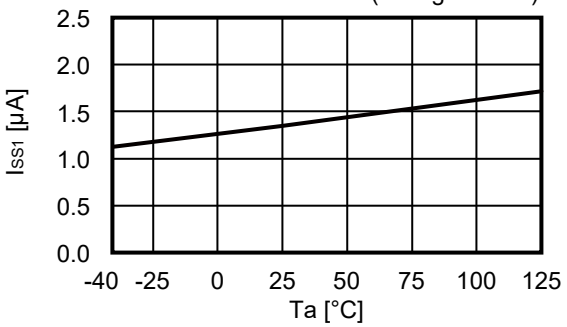


5. Current consumption (I_{SS1}) vs. Temperature (Ta)

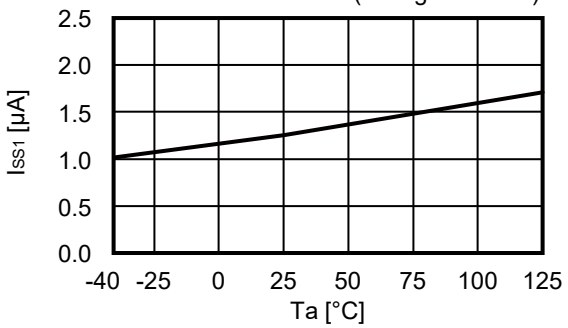
$V_{DET(S)}$ = 0.8 V, V_{DD} = 5.0 V,
V_{SENSE} = 1.8 V, V_{MR} = V_{DD}
(during release)



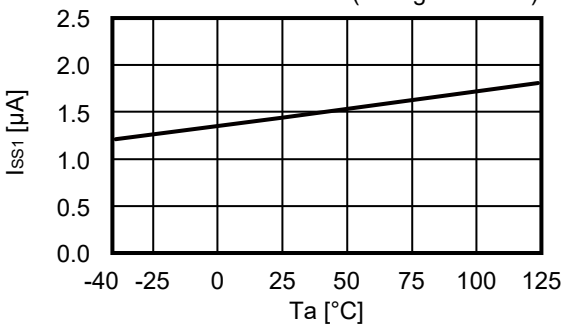
$V_{DET(S)}$ = 4.9 V, V_{DD} = 5.0 V,
V_{SENSE} = 5.9 V, V_{MR} = V_{DD}
(during release)



$V_{DET(S)}$ = 0.8 V, V_{DD} = 5.0 V,
V_{SENSE} = 0.0 V, V_{MR} = V_{DD}
(during detection)

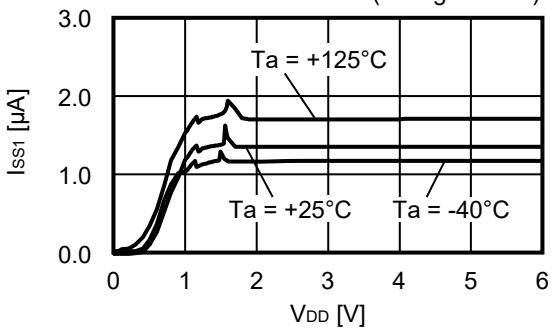


$V_{DET(S)}$ = 4.9 V, V_{DD} = 5.0 V,
V_{SENSE} = 3.9 V, V_{MR} = V_{DD}
(during detection)

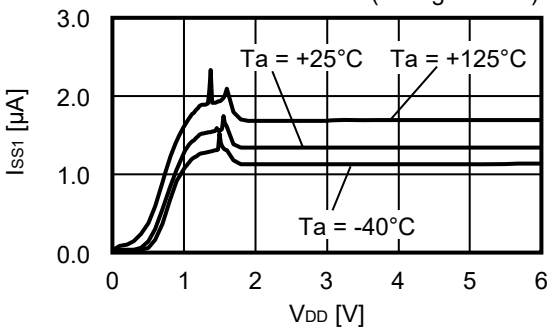


6. Current consumption (I_{SS1}) vs. Power supply voltage (V_{DD})

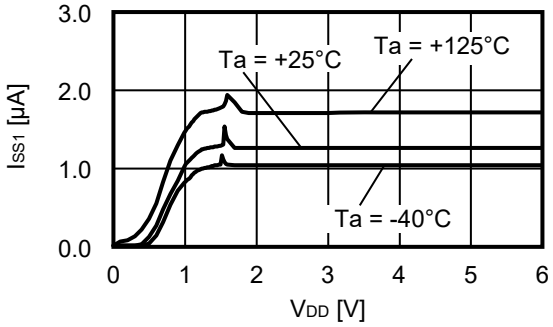
$V_{DET(S)}$ = 0.8 V,
V_{DD} = 0 V → 6.0 V, V_{SENSE} = 1.8 V
(during release)



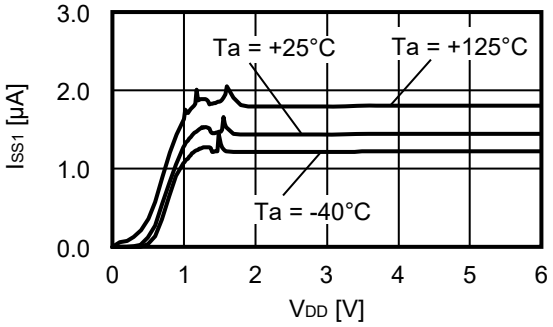
$V_{DET(S)}$ = 4.9 V,
V_{DD} = 0 V → 6.0 V, V_{SENSE} = 5.9 V
(during release)



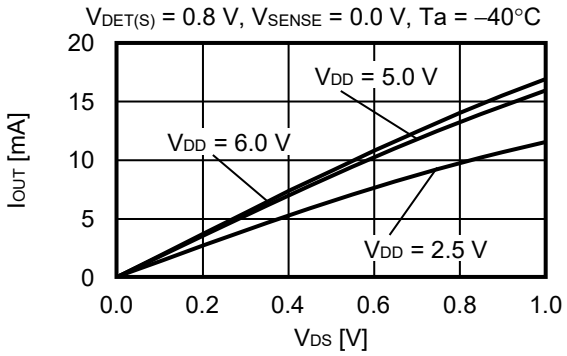
$V_{DET(S)}$ = 0.8 V,
V_{DD} = 0 V → 6.0 V, V_{SENSE} = 0.0 V
(during detection)

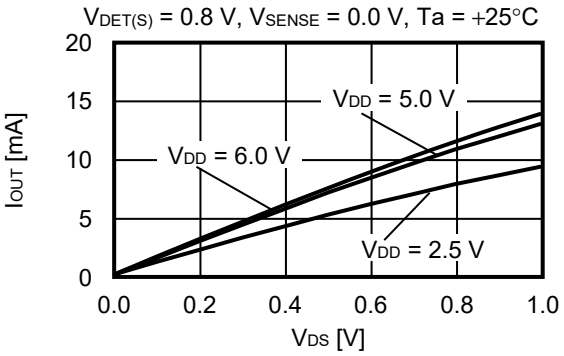


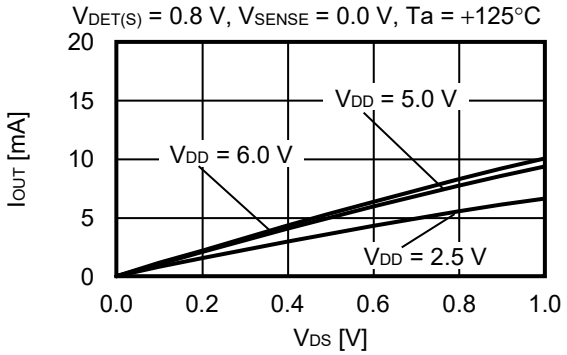
$V_{DET(S)}$ = 4.9 V,
V_{DD} = 0 V → 6.0 V, V_{SENSE} = 3.9 V
(during detection)



7. Nch transistor output current (I_{OUT}) vs. V_{DS}

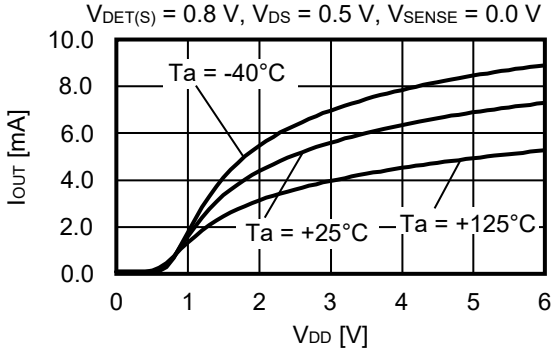






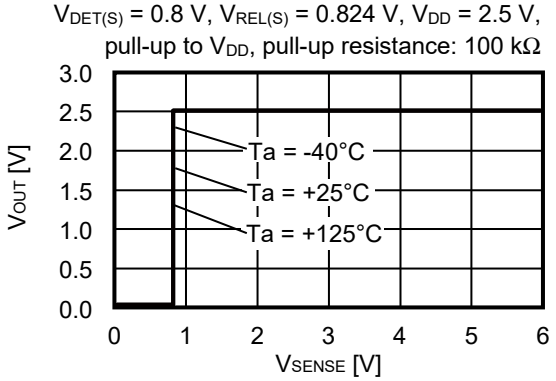
Remark V_{DS}: Drain-to-source voltage of the output transistor

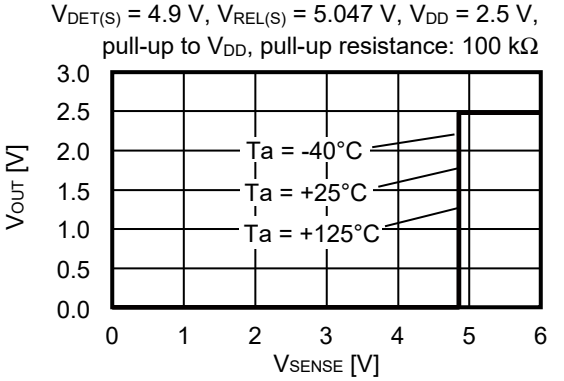
8. Nch transistor output current (I_{OUT}) vs. Power supply voltage (V_{DD})



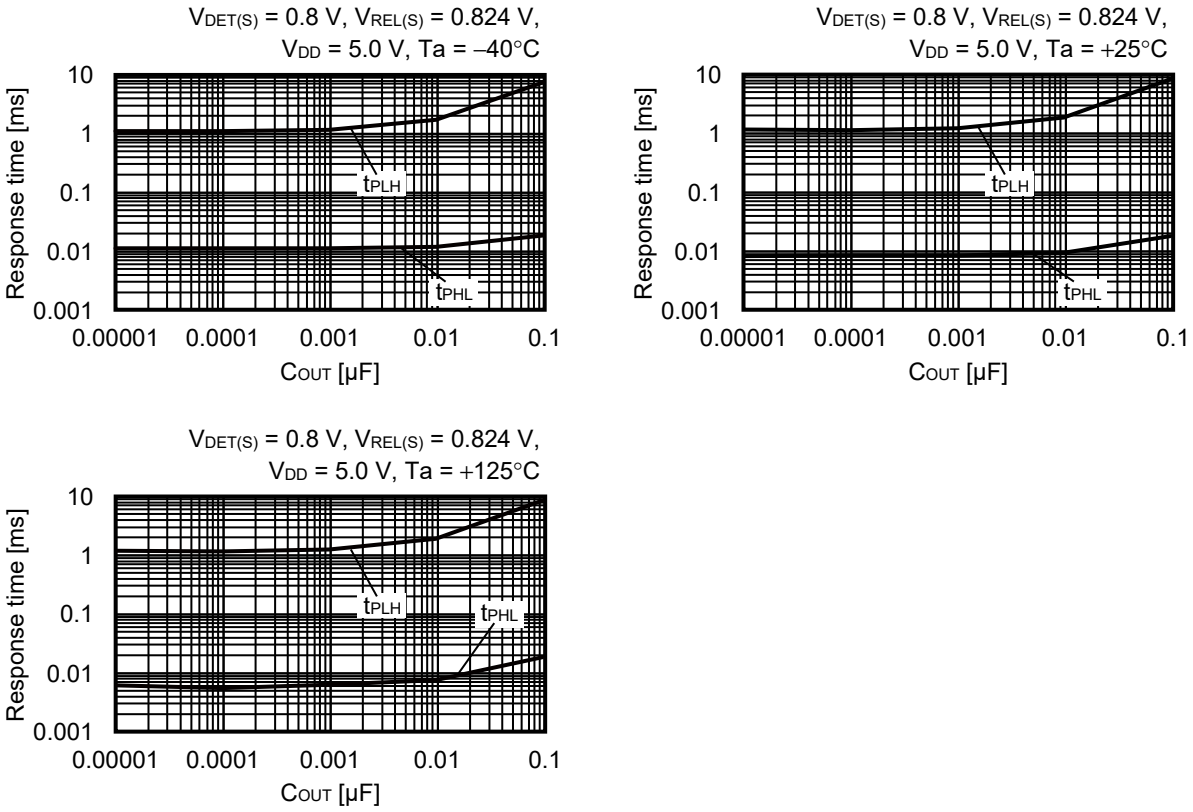
Remark V_{DS}: Drain-to-source voltage of the output transistor

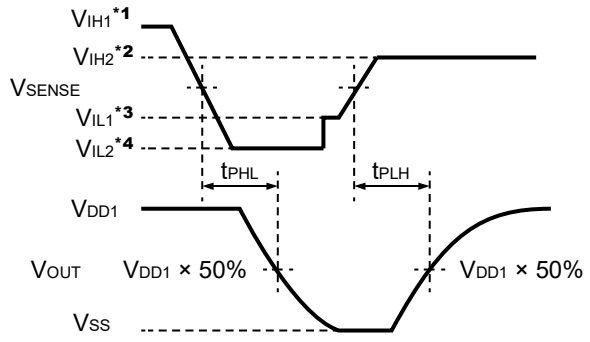
9. Output voltage (V_{OUT}) vs. SENSE pin voltage (V_{SENSE})





10. Dynamic response vs. Output pin capacitance (C_{OUT}) (CD = 0.33 nF)





***1.** $V_{IH1} = V_{DET(S)} + 0.5$ V
***2.** $V_{IH2} = V_{REL(S)} \times 1.03$ V
***3.** $V_{IL1} = V_{REL(S)} - 0.5$ V
***4.** $V_{IL2} = V_{DET(S)} - 0.5$ V

Figure 24 Test Condition of Response Time

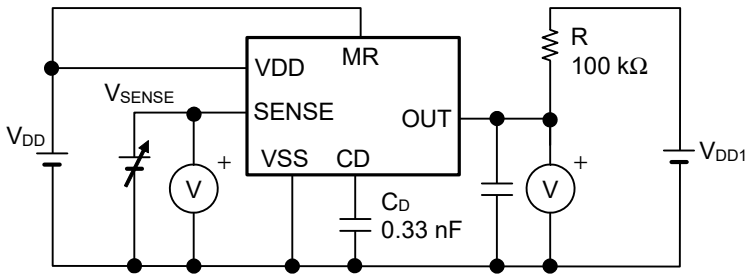
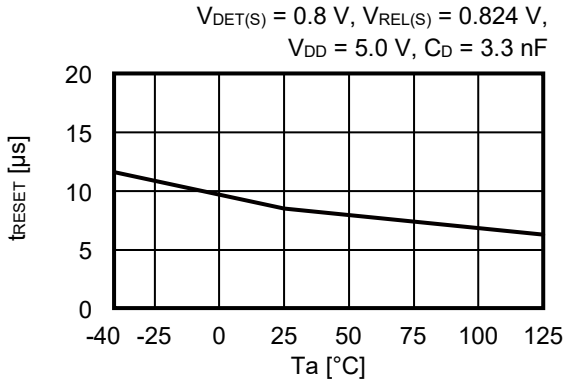


Figure 25 Test Circuit of Response Time

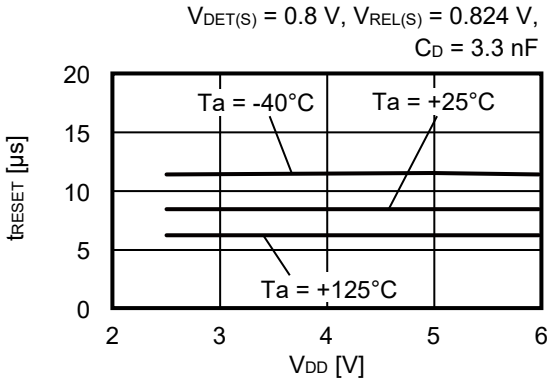
Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

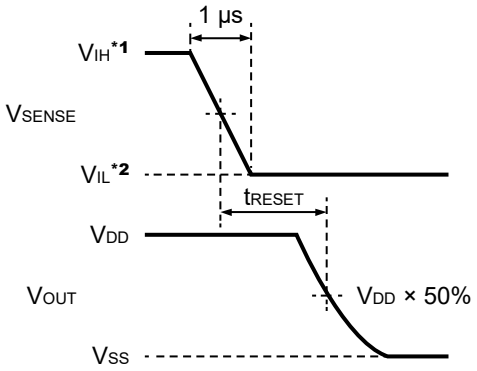
■ Reference Data

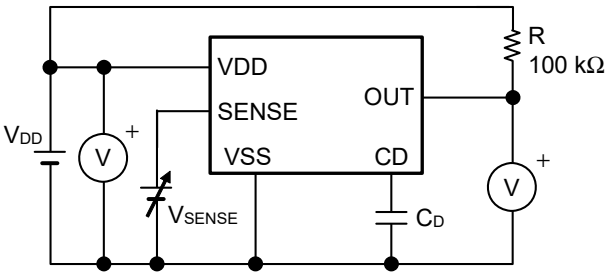
1. Detection response time (t_{RESET}) vs. Temperature (Ta)



2. Detection response time (t_{RESET}) vs. Power supply voltage (V_{DD})







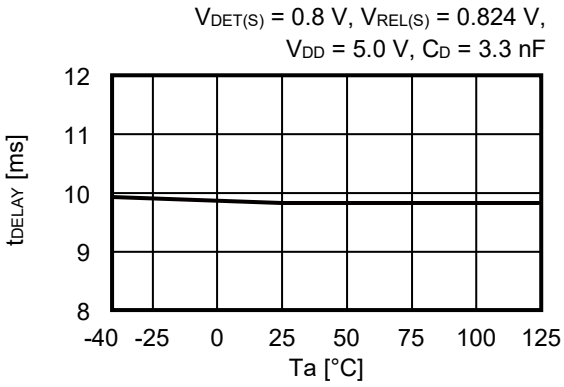
***1.** $V_{IH} = V_{DET(S)} + 0.5$ V
***2.** $V_{IL} = V_{DET(S)} - 0.5$ V

Figure 26 Test Condition of Detection Response Time

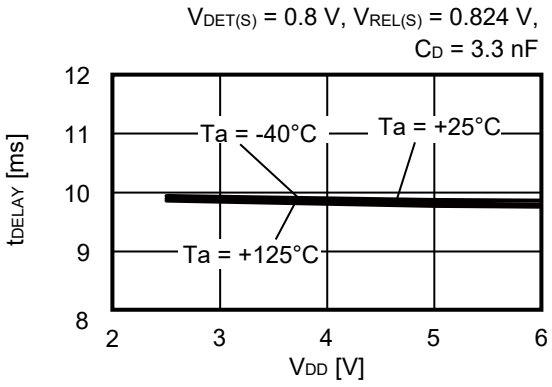
Figure 27 Test Circuit of Detection Response Time

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

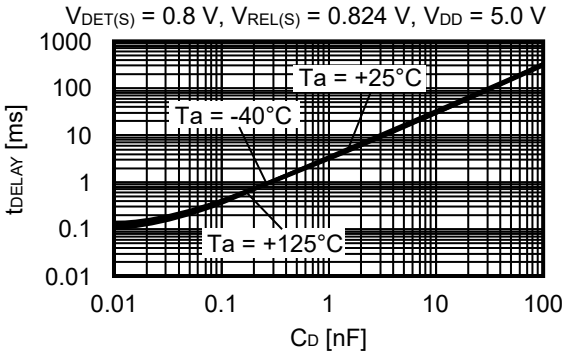
3. Release delay time (t_{DELAY}) vs. Temperature (Ta)

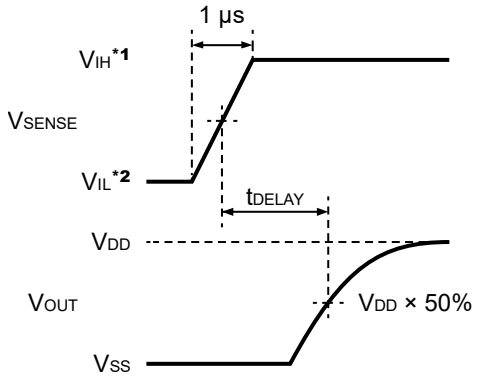


4. Release delay time (t_{DELAY}) vs. Power supply voltage (V_{DD})



5. Release delay time (t_{DELAY}) vs. CD pin capacitance (C_D) (Without output pin capacitance)





***1.** $V_{IH} = V_{REL(S)} \times 1.03$ V
***2.** $V_{IL} = V_{REL(S)} - 0.5$ V

Figure 28 Test Condition of Release Delay Time

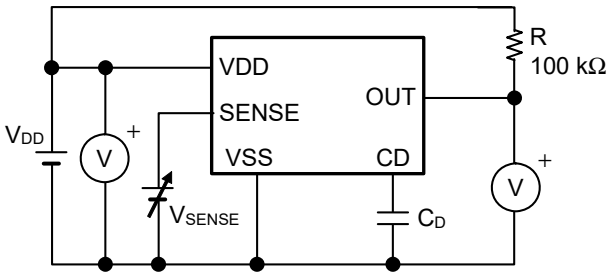
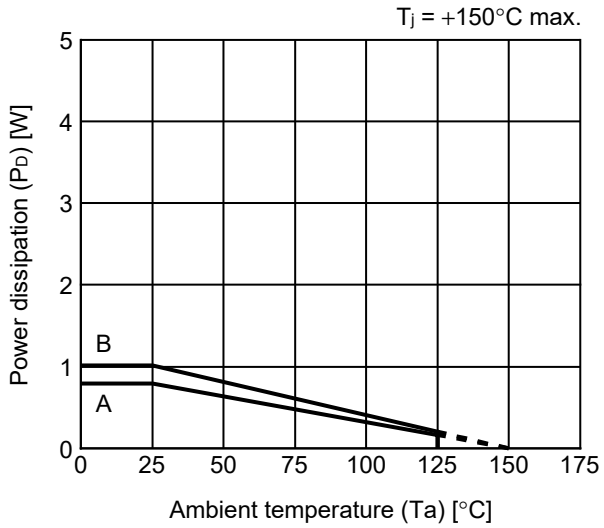


Figure 29 Test Circuit of Release Delay Time

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics with an actual application to set the constants.

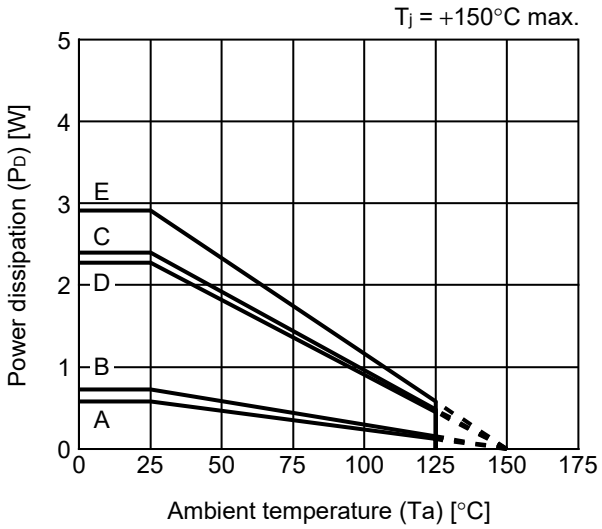
■ Power Dissipation

SOT-23-6



Board	Power Dissipation (P_D)
A	0.79 W
B	1.01 W
C	–
D	–
E	–

HSNT-8(1616)B

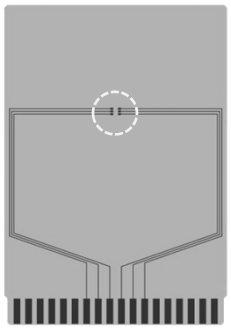


Board	Power Dissipation (P_D)
A	0.58 W
B	0.73 W
C	2.40 W
D	2.27 W
E	2.91 W

SOT-23-3/3S/5/6 Test Board

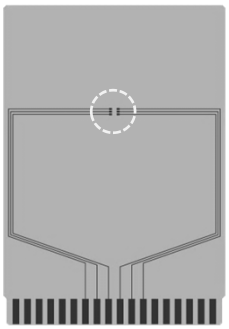
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



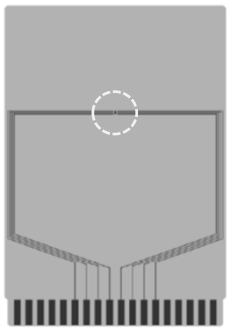
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SOT23x-A-Board-SD-2.0

HSNT-8(1616)B Test Board

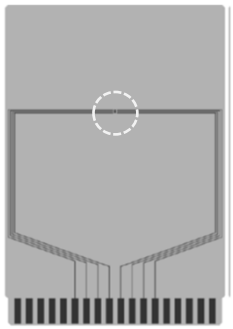
IC Mount Are

(1) Board A



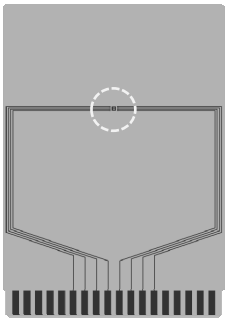
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



enlarged view

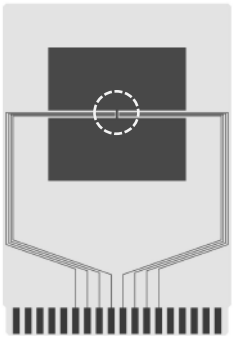
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-C-Board-SD-1.0

HSNT-8(1616)B Test Board

IC Mount Are

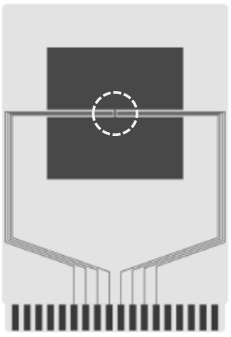
(4) Board D



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

enlarged view

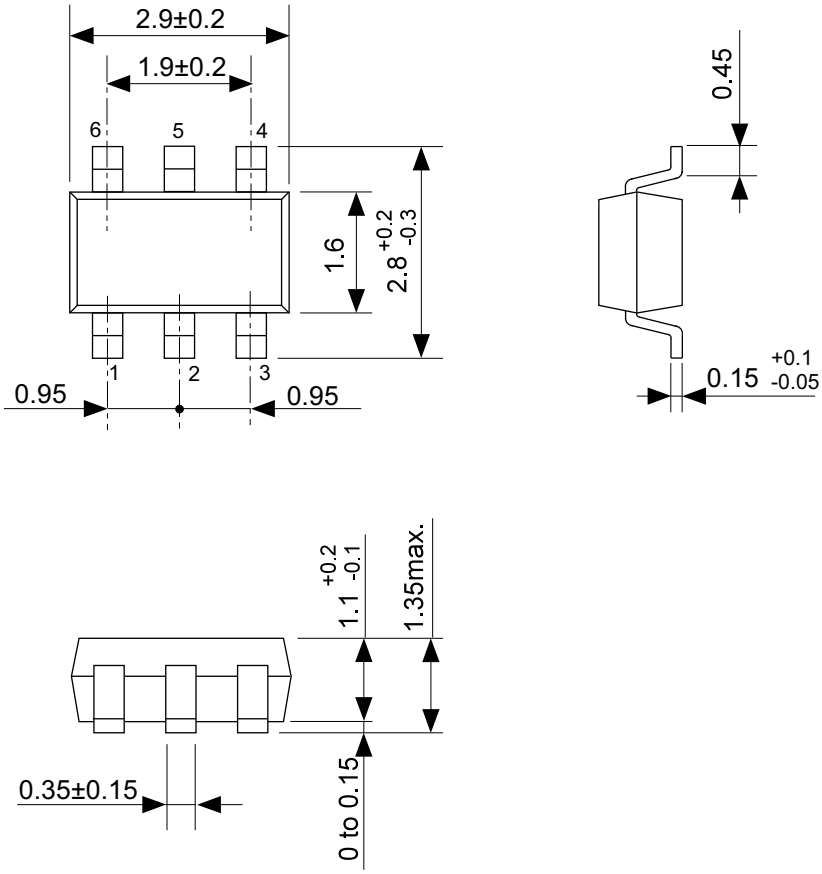
(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

enlarged view

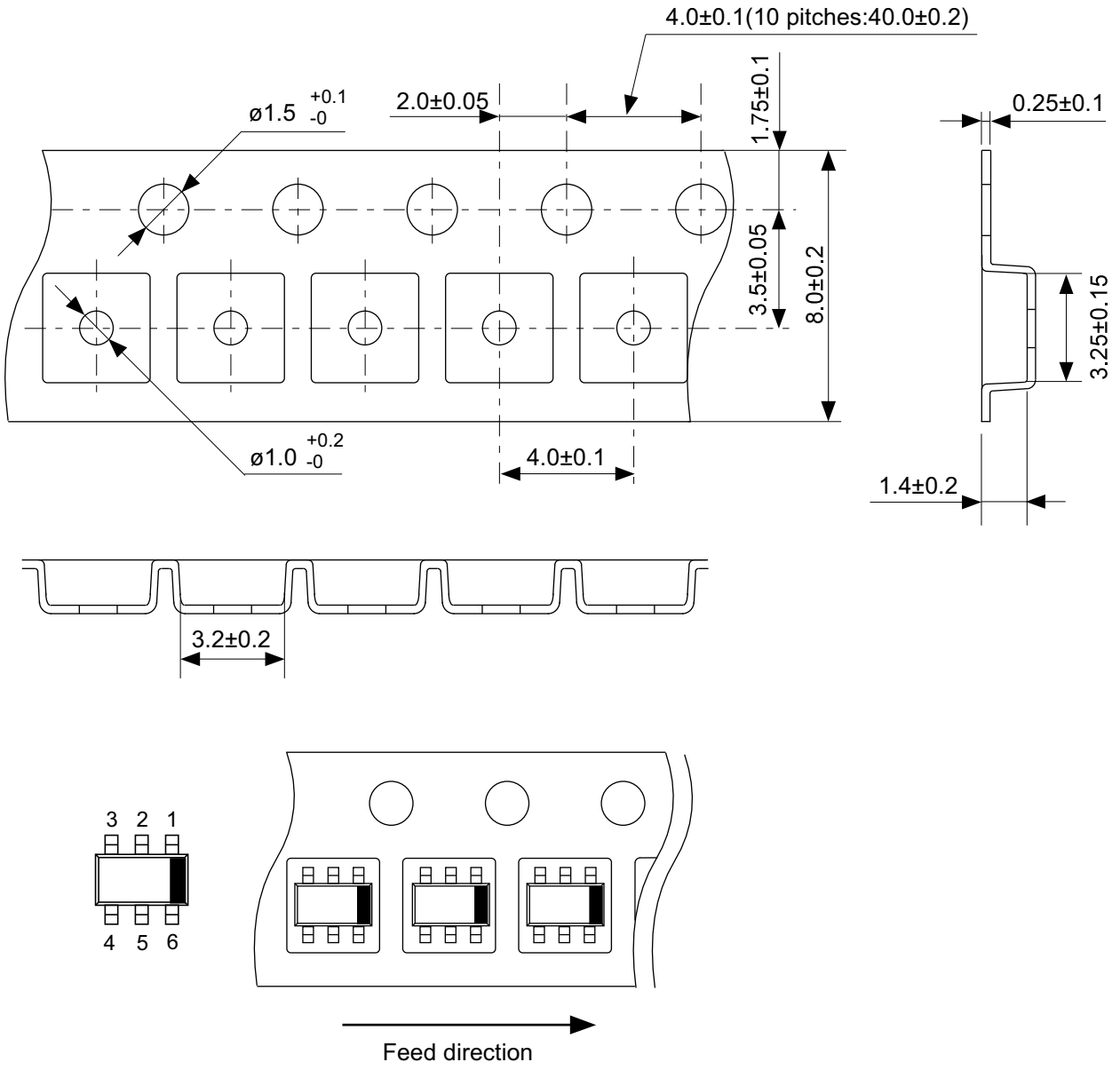
No. HSNT8-C-Board-SD-1.0



No. MP006-A-P-SD-2.1

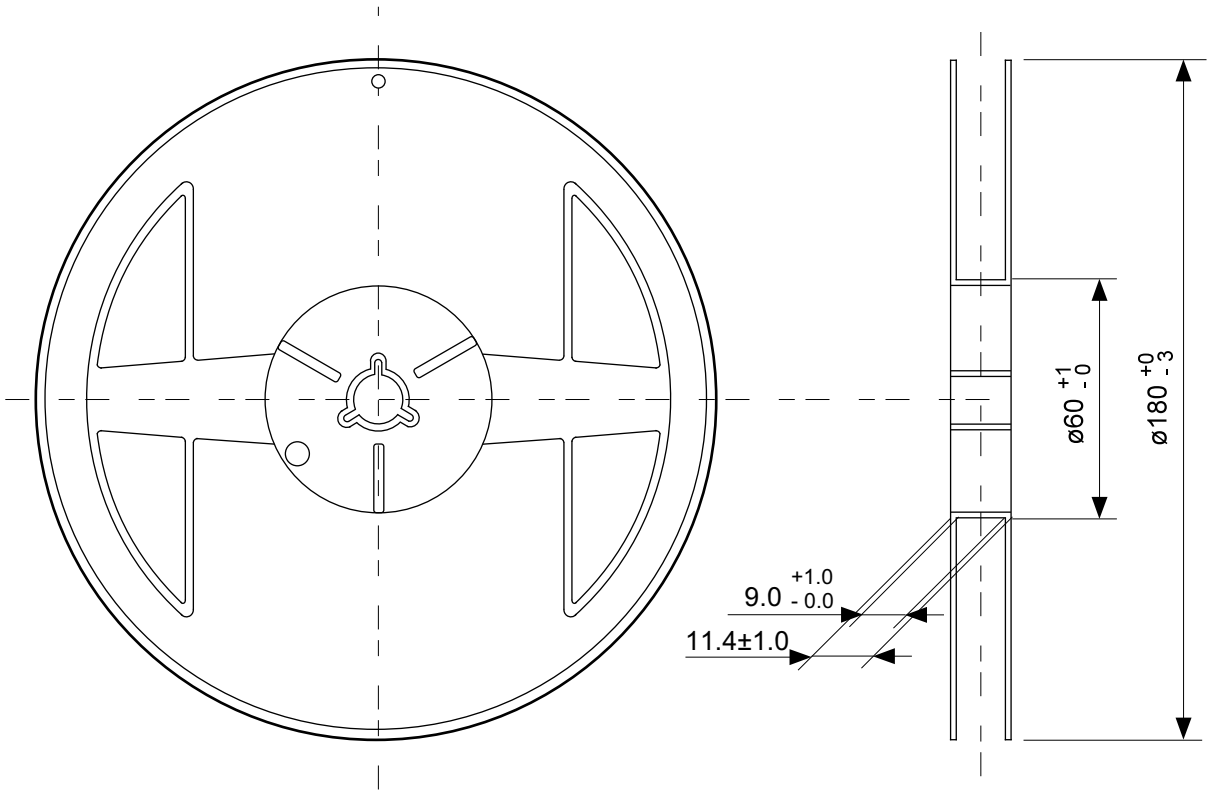
TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.1
ANGLE	
UNIT	mm

ABLIC Inc.

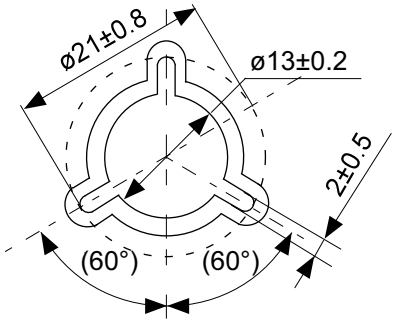


No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
ANGLE	
UNIT	mm
ABLIC Inc.	

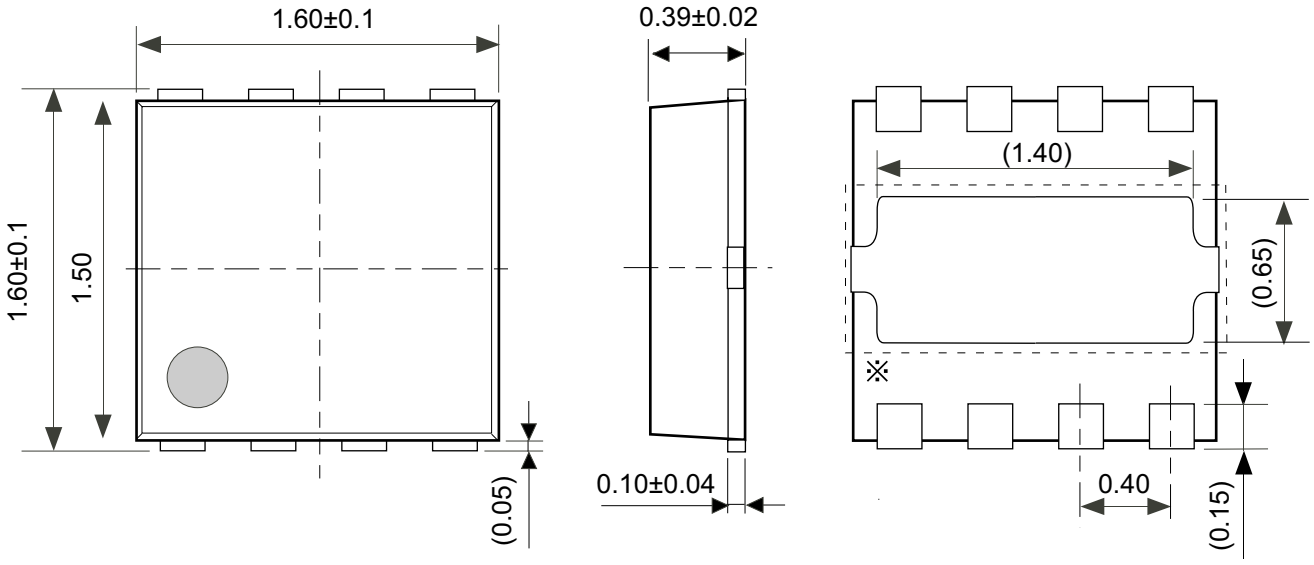


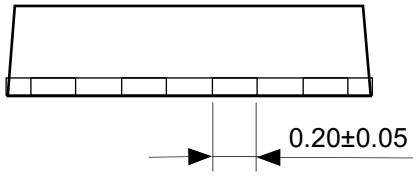
Enlarged drawing in the central part



No. MP006-A-R-SD-3.0

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-3.0		
ANGLE		QTY	3,000
UNIT	mm		
ABLIC Inc.			

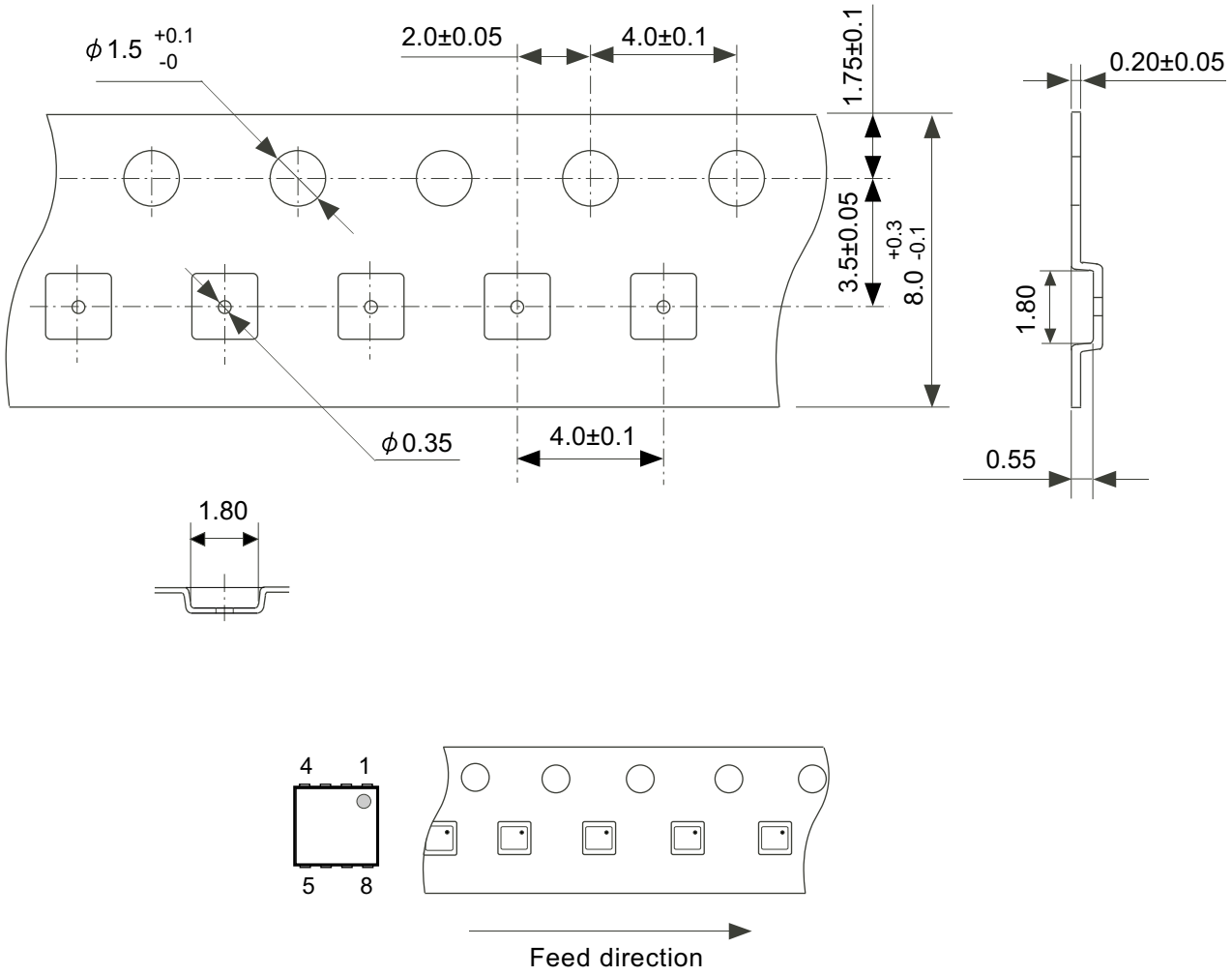




※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

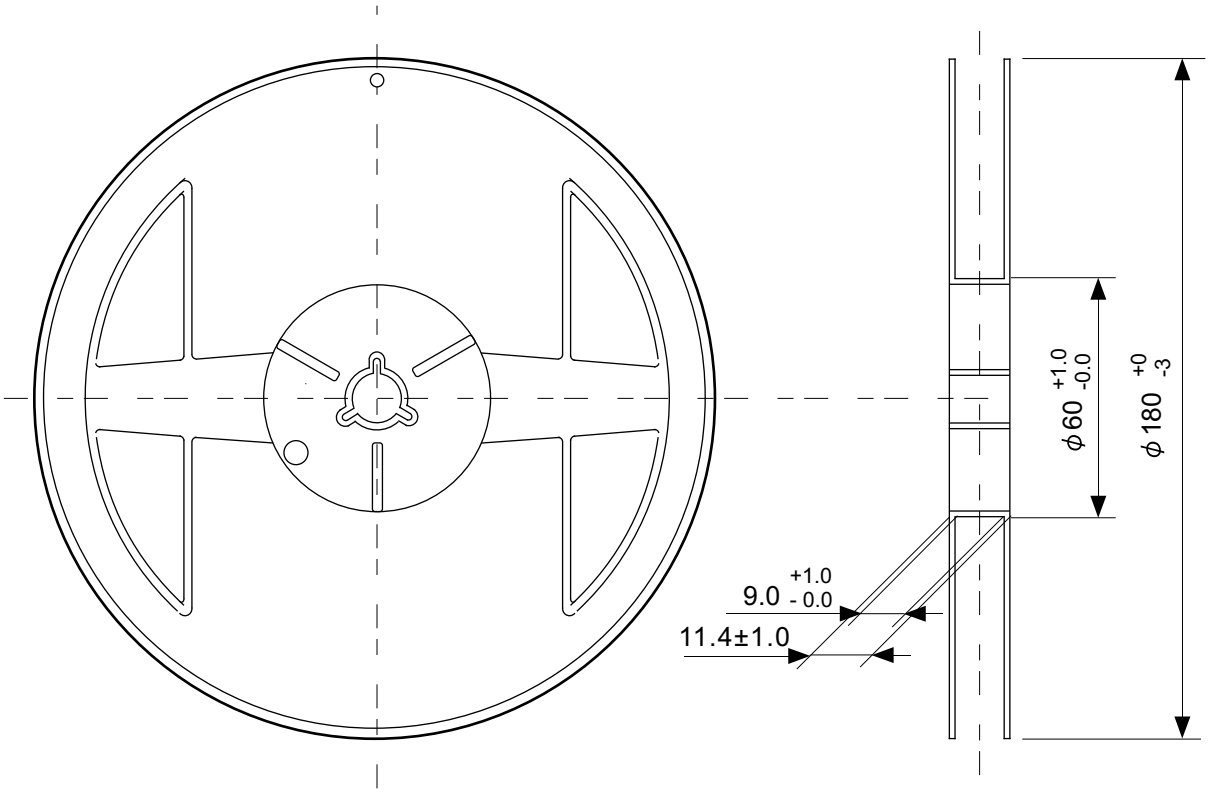
No. PY008-B-P-SD-1.0

TITLE	HSNT-8-C-PKG Dimensions
No.	PY008-B-P-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

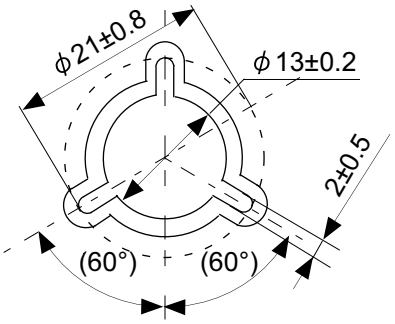


No. PY008-B-C-SD-1.0

TITLE	HSNT-8-C-Carrier Tape
No.	PY008-B-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



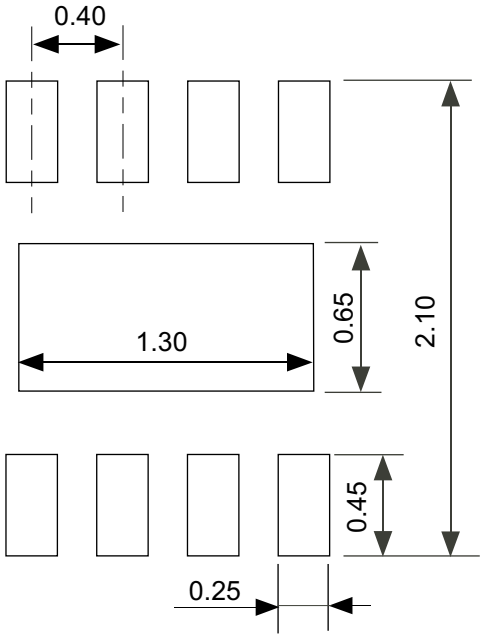
Enlarged drawing in the central part



No. PY008-B-R-SD-1.0

TITLE	HSNT-8-C-Reel		
No.	PY008-B-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

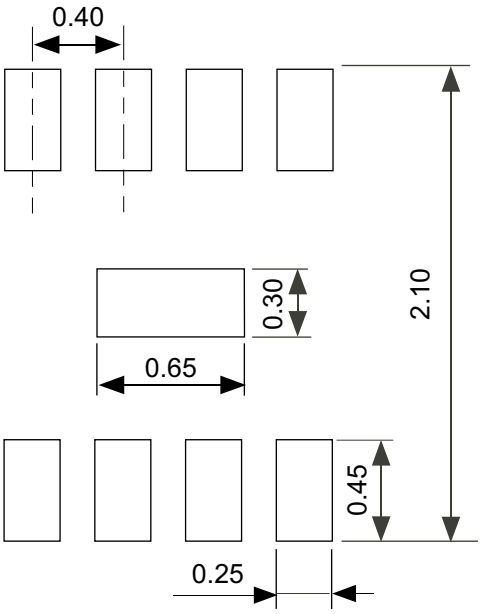
Land Pattern



Cauion It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意 放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 20%.
③ Mask thickness: t0.10 mm

注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は20%です。
③マスク厚み：t0.10 mm

No. PY008-B-L-SD-1.0

TITLE	HSNT-8-C -Land Recommendation
No.	PY008-B-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07